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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

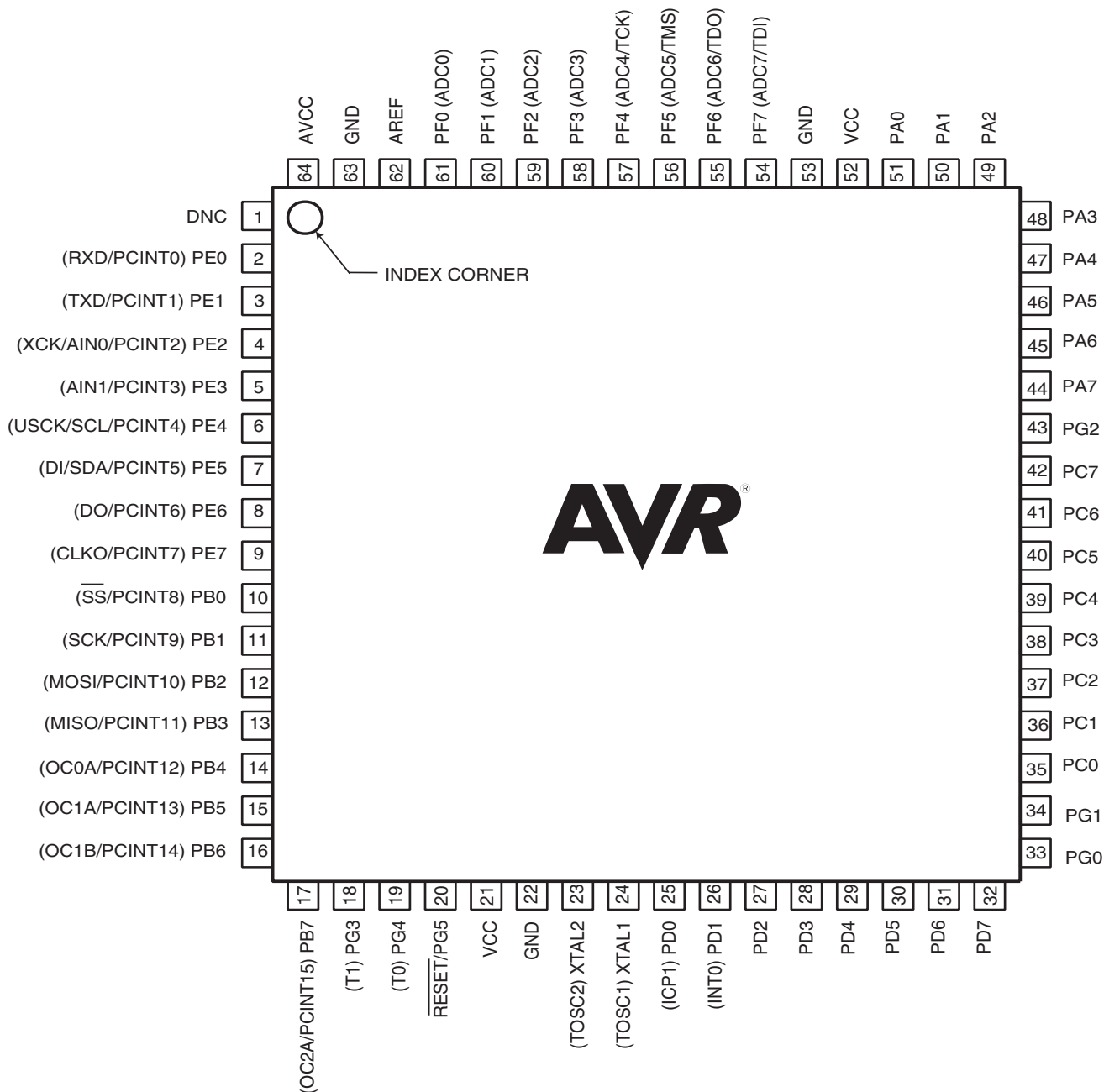
#### Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	69
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atmega3250pa-aur">https://www.e-xfl.com/product-detail/microchip-technology/atmega3250pa-aur</a>

# 1. Pin configurations

## 1.1 Pinout - TQFP and QFN/MLF

Figure 1-1. 64A (TQFP) and 64M1 (QFN/MLF) pinout Atmel  
ATmega165A/ATmega165PA/ATmega325A/ATmega325PA/ATmega645A/ATmega645P.



Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

## 2.2 Comparison between Atmel

### ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P

Table 2-1. Differences between: ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P.

Device	Flash	EEPROM	RAM	MHz
ATmega165A	16Kbyte	512Bytes	1Kbyte	16
ATmega165PA	16Kbyte	512Bytes	1Kbyte	16
ATmega325A	32Kbyte	1Kbyte	2Kbyte	20
ATmega325PA	32Kbyte	1Kbyte	2Kbyte	20
ATmega3250A	32Kbytes	1Kbyte	2Kbyte	20
ATmega3250PA	32Kbyte	1Kbyte	2Kbyte	20
ATmega645A	64Kbyte	2Kbyte	4Kbyte	16
ATmega645P	64Kbyte	2Kbyte	4Kbyte	16
ATmega6450A	64Kbyte	2Kbyte	4Kbyte	20
ATmega6450P	64Kbyte	2Kbyte	4Kbyte	20

## 2.3 Pin descriptions

### 2.3.1 VCC

Digital supply voltage.

### 2.3.2 GND

Ground.

### 2.3.3 Port A (PA7:PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on ["Alternate functions of Port B" on page 73](#).

### 2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on ["Alternate functions of Port B" on page 73](#).

### 2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins

that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the Atmel ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on ["Alternate functions of Port D" on page 75](#).

### 2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on ["Alternate functions of Port D" on page 75](#).

### 2.3.7 Port E (PE7:PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on ["Alternate functions of Port E" on page 76](#).

### 2.3.8 Port F (PF7:PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface, see ["Alternate functions of Port F" on page 78](#).

### 2.3.9 Port G (PG5:PG0)

Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P as listed on [page 80](#).

### 2.3.10 Port H (PH7:PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega3250A/3250PA/6450A/6450P as listed on [page 81](#).

### 2.3.11 Port J (PJ6:PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the Atmel ATmega3250A/3250PA/6450A/6450P as listed on [page 83](#).

### 2.3.12 RESET

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in [Table 28-13 on page 304](#). Shorter pulses are not guaranteed to generate a reset.

### 2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

### 2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

### 2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to  $V_{CC}$ , even if the ADC is not used. If the ADC is used, it should be connected to  $V_{CC}$  through a low-pass filter.

### 2.3.16 AREF

This is the analog reference pin for the A/D Converter.

### 3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on <http://www.atmel.com/avr>.

### 4. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

### 5. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBR", "SBRC", "SBR", and "CBR".

### 6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the Atmel QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: [www.atmel.com/qtouchlibrary](http://www.atmel.com/qtouchlibrary). For implementation details and other information, refer to the [Atmel QTouch Library User Guide](#) - also available for download from the Atmel website.

## 7. Register Summary

Note: Registers with bold type only available in ATmega3250A/3250PA/6450A/6450P.

(0xFF)	Reserved									
(0xFE)	Reserved									
(0xFD)	Reserved									
(0xFC)	Reserved									
(0xFB)	Reserved									
(0xFA)	Reserved									
(0xF9)	Reserved									
(0xF8)	Reserved									
(0xF7)	Reserved									
(0xF6)	Reserved									
(0xF5)	Reserved									
(0xF4)	Reserved									
(0xF3)	Reserved									
(0xF2)	Reserved									
(0xF1)	Reserved									
(0xF0)	Reserved									
(0xEF)	Reserved									
(0xEE)	Reserved									
(0xED)	Reserved									
(0xEC)	Reserved									
(0xEB)	Reserved	-	-	-	-	-	-	-	-	
(0xEA)	Reserved	-	-	-	-	-	-	-	-	
(0xE9)	Reserved	-	-	-	-	-	-	-	-	
(0xE8)	Reserved	-	-	-	-	-	-	-	-	
(0xE7)	Reserved									
(0xE6)	Reserved									
(0xE5)	Reserved									
(0xE4)	Reserved									
(0xE3)	Reserved	-	-	-	-	-	-	-	-	
(0xE2)	Reserved	-	-	-	-	-	-	-	-	
(0xE1)	Reserved	-	-	-	-	-	-	-	-	
(0xE0)	Reserved	-	-	-	-	-	-	-	-	
(0xDF)	Reserved	-	-	-	-	-	-	-	-	
(0xDE)	Reserved	-	-	-	-	-	-	-	-	
(0xDD)	<b>PORTJ</b>	-	<b>PORTJ6</b>	<b>PORTJ5</b>	<b>PORTJ4</b>	<b>PORTJ3</b>	<b>PORTJ2</b>	<b>PORTJ1</b>	<b>PORTJ0</b>	88
(0xDC)	<b>DDRJ</b>	-	<b>DDJ6</b>	<b>DDJ5</b>	<b>DDJ4</b>	<b>DDJ3</b>	<b>DDJ2</b>	<b>DDJ1</b>	<b>DDJ0</b>	88
(0xDB)	<b>PINJ</b>	-	<b>PINJ6</b>	<b>PINJ5</b>	<b>PINJ4</b>	<b>PINJ3</b>	<b>PINJ2</b>	<b>PINJ1</b>	<b>PINJ0</b>	88
(0xDA)	<b>PORTH</b>	<b>PORTH7</b>	<b>PORTH6</b>	<b>PORTH5</b>	<b>PORTH4</b>	<b>PORTH3</b>	<b>PORTH2</b>	<b>PORTH1</b>	<b>PORTH0</b>	87
(0xD9)	<b>DDRH</b>	<b>DDH7</b>	<b>DDH6</b>	<b>DDH5</b>	<b>DDH4</b>	<b>DDH3</b>	<b>DDH2</b>	<b>DDH1</b>	<b>DDH0</b>	87
(0xD8)	<b>PINH</b>	<b>PINH7</b>	<b>PINH6</b>	<b>PINH5</b>	<b>PINH4</b>	<b>PINH3</b>	<b>PINH2</b>	<b>PINH1</b>	<b>PINH0</b>	88
(0xD7)	Reserved	-	-	-	-	-	-	-	-	
(0xD6)	Reserved	-	-	-	-	-	-	-	-	
(0xD5)	Reserved	-	-	-	-	-	-	-	-	
(0xD4)	Reserved	-	-	-	-	-	-	-	-	
(0xD3)	Reserved	-	-	-	-	-	-	-	-	
(0xD2)	Reserved	-	-	-	-	-	-	-	-	
(0xD1)	Reserved	-	-	-	-	-	-	-	-	
(0xD0)	Reserved	-	-	-	-	-	-	-	-	
(0xCF)	Reserved	-	-	-	-	-	-	-	-	
(0xCE)	Reserved	-	-	-	-	-	-	-	-	
(0xCD)	Reserved	-	-	-	-	-	-	-	-	
(0xCC)	Reserved	-	-	-	-	-	-	-	-	
(0xCB)	Reserved	-	-	-	-	-	-	-	-	
(0xCA)	Reserved	-	-	-	-	-	-	-	-	
(0xC9)	Reserved	-	-	-	-	-	-	-	-	
(0xC8)	Reserved	-	-	-	-	-	-	-	-	
(0xC7)	Reserved	-	-	-	-	-	-	-	-	
(0xC6)	UDR0	USART0 Data Register								178
(0xC5)	UBRR0H	USART0 Baud Rate Register High								182

(0xC4)	UBRR0L	USART0 Baud Rate Register Low								182
(0xC3)	Reserved	-	-	-	-	-	-	-	-	
(0xC2)	UCSR0C	-	UMSEL0	UPM01	UPM00	USBS0	UCSZ01	UCSZ00	UCPOL0	180
(0xC1)	UCSR0B	RXCIE0	TXCIE0	UDRIE0	RXEN0	TXEN0	UCSZ02	RXB80	TXB80	179
(0xC0)	UCSR0A	RXC0	TXC0	UDRE0	FE0	DOR0	UPE0	U2X0	MPCM0	178
(0xBF)	Reserved	-	-	-	-	-	-	-	-	
(0xBE)	Reserved	-	-	-	-	-	-	-	-	
(0xBD)	Reserved	-	-	-	-	-	-	-	-	
(0xBC)	Reserved	-	-	-	-	-	-	-	-	
(0xBB)	Reserved	-	-	-	-	-	-	-	-	
(0xBA)	USIDR	USI Data Register								190
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	190
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	191
(0xB7)	Reserved	-	-	-	-	-	-	-	-	
(0xB6)	ASSR	-	-	-	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB	146
(0xB5)	Reserved	-	-	-	-	-	-	-	-	
(0xB4)	Reserved	-	-	-	-	-	-	-	-	
(0xB3)	OCR2A	Timer/Counter 2 Output Compare Register A								145
(0xB2)	TCNT2	Timer/Counter2								144
(0xB1)	Reserved	-	-	-	-	-	-	-	-	
(0xB0)	TCCR2A	FOC2A	WGM20	COM2A1	COM2A0	WGM21	CS22	CS21	CS20	143
(0xAF)	Reserved	-	-	-	-	-	-	-	-	
(0xAE)	Reserved	-	-	-	-	-	-	-	-	
(0xAD)	Reserved	-	-	-	-	-	-	-	-	
(0xAC)	Reserved	-	-	-	-	-	-	-	-	
(0xAB)	Reserved	-	-	-	-	-	-	-	-	
(0xAA)	Reserved	-	-	-	-	-	-	-	-	
(0xA9)	Reserved	-	-	-	-	-	-	-	-	
(0xA8)	Reserved	-	-	-	-	-	-	-	-	
(0xA7)	Reserved	-	-	-	-	-	-	-	-	
(0xA6)	Reserved	-	-	-	-	-	-	-	-	
(0xA5)	Reserved	-	-	-	-	-	-	-	-	
(0xA4)	Reserved	-	-	-	-	-	-	-	-	
(0xA3)	Reserved	-	-	-	-	-	-	-	-	
(0xA2)	Reserved	-	-	-	-	-	-	-	-	
(0xA1)	Reserved	-	-	-	-	-	-	-	-	
(0xA0)	Reserved	-	-	-	-	-	-	-	-	
(0x9F)	Reserved	-	-	-	-	-	-	-	-	
(0x9E)	Reserved	-	-	-	-	-	-	-	-	
(0x9D)	Reserved	-	-	-	-	-	-	-	-	
(0x9C)	Reserved	-	-	-	-	-	-	-	-	
(0x9B)	Reserved	-	-	-	-	-	-	-	-	
(0x9A)	Reserved	-	-	-	-	-	-	-	-	
(0x99)	Reserved	-	-	-	-	-	-	-	-	
(0x98)	Reserved	-	-	-	-	-	-	-	-	
(0x97)	Reserved	-	-	-	-	-	-	-	-	
(0x96)	Reserved	-	-	-	-	-	-	-	-	
(0x95)	Reserved	-	-	-	-	-	-	-	-	
(0x94)	Reserved	-	-	-	-	-	-	-	-	
(0x93)	Reserved	-	-	-	-	-	-	-	-	
(0x92)	Reserved	-	-	-	-	-	-	-	-	
(0x91)	Reserved	-	-	-	-	-	-	-	-	
(0x90)	Reserved	-	-	-	-	-	-	-	-	
(0x8F)	Reserved	-	-	-	-	-	-	-	-	
(0x8E)	Reserved	-	-	-	-	-	-	-	-	
(0x8D)	Reserved	-	-	-	-	-	-	-	-	
(0x8C)	Reserved	-	-	-	-	-	-	-	-	
(0x8B)	OCR1BH	Timer/Counter1 Output Compare Register B High								126
(0x8A)	OCR1BL	Timer/Counter1 Output Compare Register B Low								126
(0x89)	OCR1AH	Timer/Counter1 Output Compare Register A High								126
(0x88)	OCR1AL	Timer/Counter1 Output Compare Register A Low								126
(0x87)	ICR1H	Timer/Counter1 Input Capture Register High								126
(0x86)	ICR1L	Timer/Counter1 Input Capture Register Low								126
(0x85)	TCNT1H	Timer/Counter1 High								126
(0x84)	TCNT1L	Timer/Counter1 Low								126



0x22 (0x42)	EEARH	–	–	–	–	–	–	–	–	25
0x21 (0x41)	EEARL	EEPROM Address Register Low								25
0x20 (0x40)	EEDR	EEPROM Data Register								26
0x1F (0x3F)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	26
0x1E (0x3E)	GPOR0	General Purpose I/O Register								27
0x1D (0x3D)	EIMSK	PCIE	PCIE2	PCIE1	PCIE0	–	–	–	INT0	61
0x1C (0x3C)	EIFR	PCIF3	PCIF2	PCIF1	PCIF0	–	–	–	INTF0	62
0x1B (0x3B)	Reserved	–	–	–	–	–	–	–	–	
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	TIFR2	–	–	–	–	–	–	OCF2A	TOV2	145
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	127
0x15 (0x35)	TIFR0	–	–	–	–	–	–	OCF0A	TOV0	130
0x14 (0x34)	PORTG	–	–	–	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	87
0x13 (0x33)	DDRG	–	–	–	DDG4	DDG3	DDG2	DDG1	DDG0	87
0x12 (0x32)	PING	–	–	PING5	PING4	PING3	PING2	PING1	PING0	87
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	87
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	87
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	87
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	86
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	86
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	87
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	86
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	86
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	86
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	86
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	86
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	86
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	85
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	85
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	85
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	85
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	85
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	85

- Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
  2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
  3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
  4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
<b>BIT AND BIT-TEST INSTRUCTIONS</b>					
SBI	P, b	Set Bit in I/O Register	I/O(P, b) ← 1	None	2
CBI	P, b	Clear Bit in I/O Register	I/O(P, b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z, C, N, V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z, C, N, V	1
ROL	Rd	Rotate Left Through Carry	Rd(0) ← C, Rd(n+1) ← Rd(n), C ← Rd(7)	Z, C, N, V	1
ROR	Rd	Rotate Right Through Carry	Rd(7) ← C, Rd(n) ← Rd(n+1), C ← Rd(0)	Z, C, N, V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z, C, N, V	1
SWAP	Rd	Swap Nibbles	Rd(3..0) ← Rd(7..4), Rd(7..4) ← Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
<b>DATA TRANSFER INSTRUCTIONS</b>					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q, Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q, Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
<b>MCU CONTROL INSTRUCTIONS</b>					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

## 9. Ordering Information

### 9.1 ATmega165A

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
16	1.8 - 5.5V	ATmega165A-AU ATmega165A-AUR <sup>(4)</sup> ATmega165A-MU ATmega165A-MUR <sup>(4)</sup> ATmega165A-MCH ATmega165A-MCHR <sup>(4)</sup>	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega165A-AN ATmega165A-ANR <sup>(4)</sup> ATmega165A-MN ATmega165A-MNR <sup>(4)</sup>	64A 64A 64M1 64M1	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel
  5. See characterization specifications at 105°C.

Package Type	
<b>64A</b>	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M1</b>	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
<b>64MC</b>	64-lead (2-row Staggered), 7 x 7 x 1.0 mm body, 4.0 x 4.0mm Exposed Pad, Quad Flat No-Lead Package (QFN)

## 9.2 ATmega165PA

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
16	1.8 - 5.5V	ATmega165PA-AU ATmega165PA-AUR <sup>(4)</sup> ATmega165PA-MU ATmega165PA-MUR <sup>(4)</sup> ATmega165PA-MCH ATmega165PA-MCHR <sup>(4)</sup>	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega165PA-AN ATmega165PA-ANR <sup>(4)</sup> ATmega165PA-MN ATmega165PA-MNR <sup>(4)</sup>	64A 64A 64M1 64M1	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel.
  5. See characterization specifications at 105°C.

Package Type	
<b>64A</b>	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M1</b>	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
<b>64MC</b>	64-lead (2-row Staggered), 7 x 7 x 1.0mm body, 4.0 x 4.0 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

## 9.4 ATmega325PA

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
20	1.8 - 5.5V	ATmega325PA-AU ATmega325PA-AUR <sup>(4)</sup> ATmega325PA-MU ATmega325PA-MUR <sup>(4)</sup>	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega325PA-AN ATmega325PA-ANR <sup>(4)</sup> ATmega325PA-MN ATmega325PA-MNR <sup>(4)</sup>	64A 64A 64M1 64M1	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel
  5. See characterization specifications at 105°C.

Package Type	
<b>64A</b>	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M1</b>	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

## 9.5 ATmega3250A

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
20	1.8 - 5.5V	ATmega3250A-AU ATmega3250A-AUR <sup>(4)</sup>	100A 100A	Industrial (-40°C to 85°C)
		ATmega3250A-AN ATmega3250A-ANR <sup>(4)</sup>	100A 100A	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel
  5. See characterization specifications at 105°C.

Package Type	
<b>100A</b>	100-lead, 14 x 14 x 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

## 9.6 ATmega3250PA

Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
20	1.8 - 5.5V	ATmega3250PA-AU ATmega3250PA-AUR <sup>(4)</sup>	100A 100A	Industrial (-40°C to 85°C)
		ATmega3250PA-AN ATmega3250PA-ANR <sup>(4)</sup>	100A 100A	Extended (-40°C to 105°C) <sup>(5)</sup>

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel
  5. See characterization specifications at 105°C.

Package Type	
<b>100A</b>	100-lead, 14 x 14 x 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)



## 9.8 ATmega645P

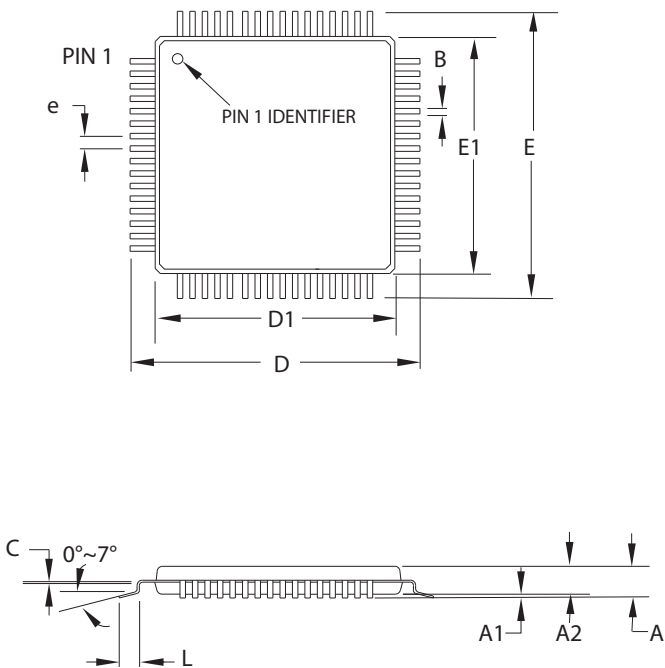
Speed (MHz) <sup>(3)</sup>	Power Supply	Ordering Code <sup>(2)</sup>	Package <sup>(1)</sup>	Operation Range
20	1.8 - 5.5V	ATmega645P-AU ATmega645P-AUR <sup>(4)</sup> ATmega645P-MU ATmega645P-MUR <sup>(4)</sup>	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

- Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
  2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
  3. For Speed vs.  $V_{CC}$ , see [Figure 28-1 on page 302](#).
  4. Tape & Reel

Package Type	
<b>64A</b>	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
<b>64M1</b>	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

# 10. Packaging Information

## 10.1 64A




COMMON DIMENSIONS  
(Unit of measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30–	0.45		
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

- Notes:
- 1.This package conforms to JEDEC reference MS-026, Variation AEB.
  - 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
  - 3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	2325 Orchard Parkway San Jose, CA 95131	TITLE 64A, 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	DRAWING NO.	REV.
			64A	C

## 11. Errata

### 11.1 ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P Rev. G

No known errata.

### 11.2 ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P Rev. A to F

Not sampled.

## 12.5 8285B – 03/11

1. Updated the datasheet according to the Atmel new Brand Style Guide
2. Updated ["Signature bytes"](#) , [Table 27.3 on page 267](#).
3. Updated the power supply voltage (1.5 - 5.5V) for all devices in ["Ordering Information" on page 18](#).
4. Added ["Ordering Information"](#) for Extended Temperature (-40°C to 105°C)

## 12.6 8285A – 09/10

1. Initial revision (Based on the ATmega165P/325P/3250P/645/6450/V).
2. Changes done compared to ATmega165P/325P/3250P/645/6450/V datasheet:
  - New EIMSK and EIFR register overview
  - New graphics in ["Typical characteristics – TA = -40°C to 85°C" on page 314](#).
  - Ordering Information includes Tape & Reel
  - New ["Ordering Information" on page 18](#).
  - QTouch Library Support Features

