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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	16MHz
Connectivity	SPI, UART/USART, USI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	54
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega645p-aur

1. Pin configurations

1.1 Pinout - TQFP and QFN/MLF

Figure 1-1. 64A (TQFP)and 64M1 (QFN/MLF) pinout Atmel ATmega165A/ATmega165PA/ATmega325A/ATmega325PA/ATmega645A/ATmega645P.
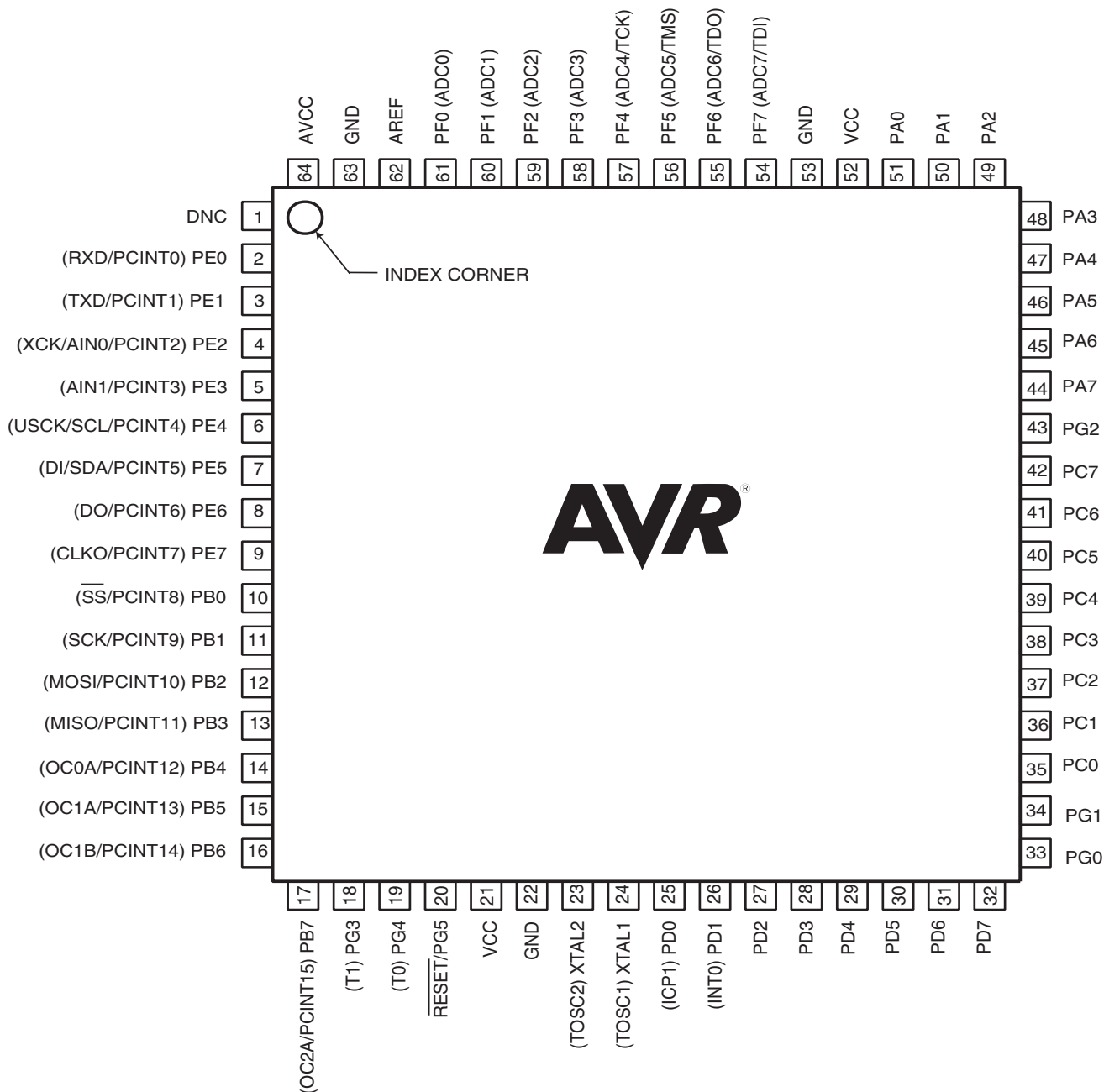

Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

1.2   Pinout - 100A (TQFP)

Figure 1-2.   Pinout Atmel ATmega3250A/ATmega3250PA/ATmega6450A/ATmega6450P.

TQFP
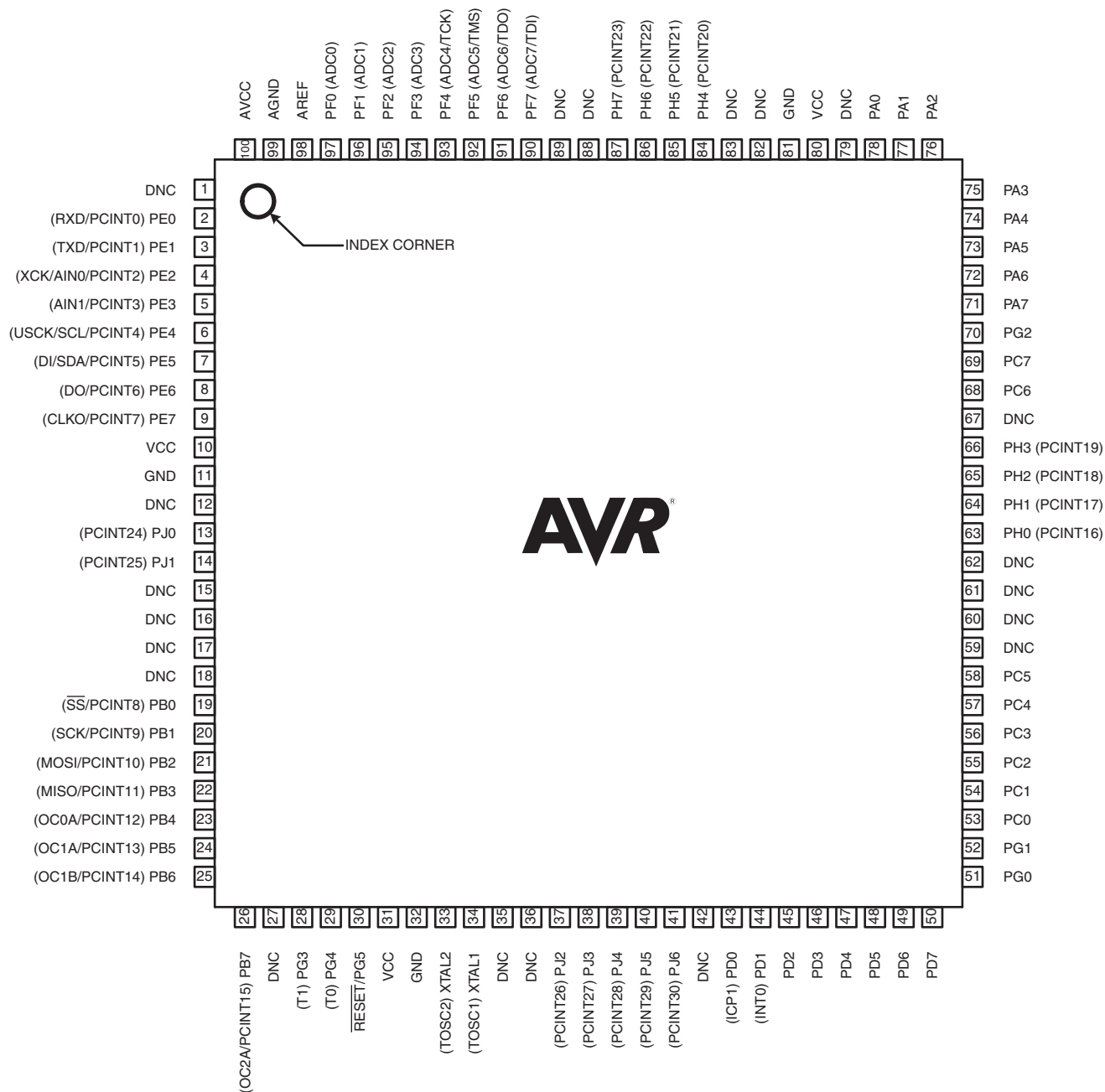
2. Overview

The Atmel ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, this microcontroller achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.
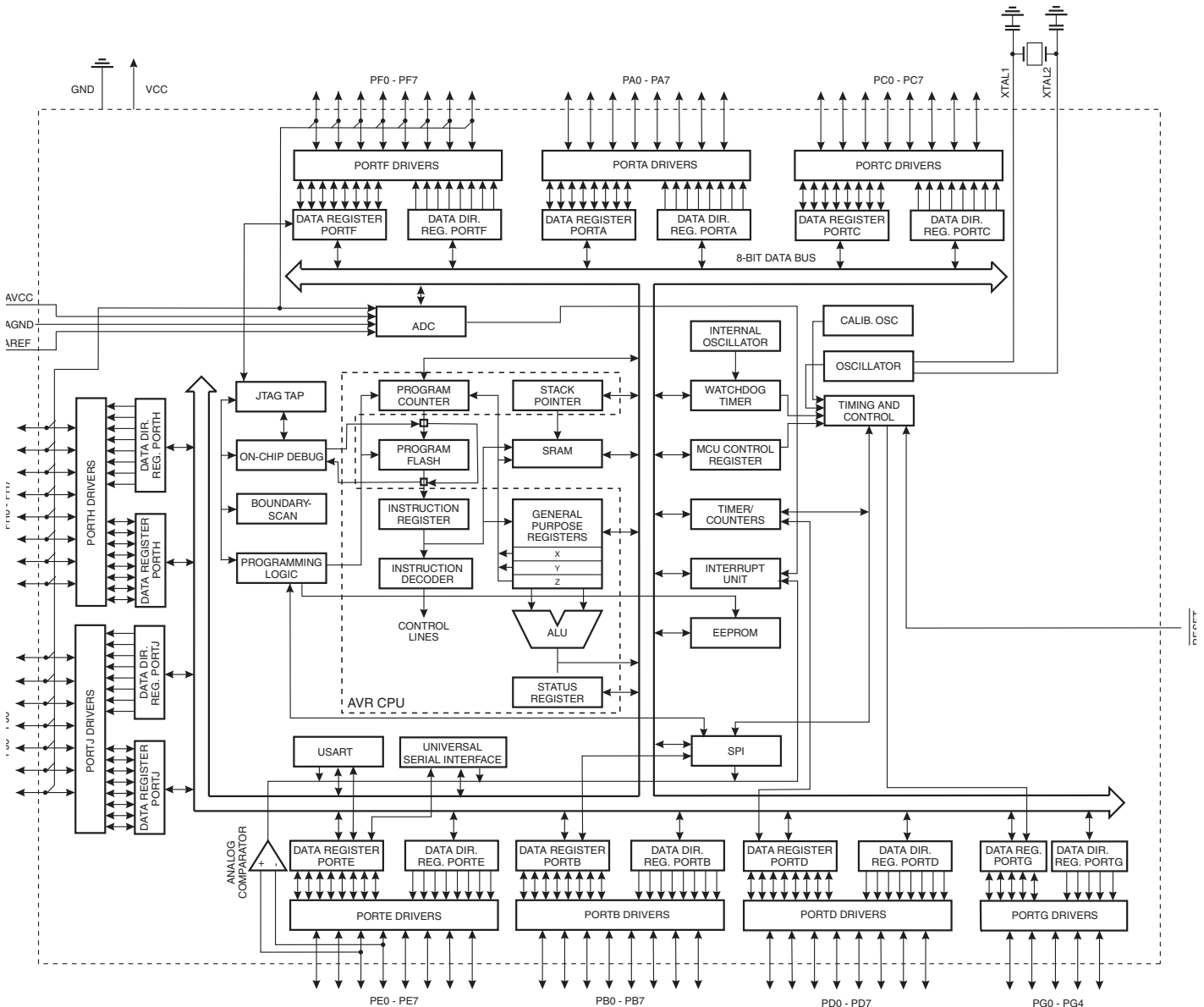
The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P provides the following features: 16K/32K/64K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K bytes EEPROM, 1K/2K/4K byte SRAM, 54/69 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, an 8-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the XTAL/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

Atmel offers the QTouch® library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel devise is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.3.11 Port J (PJ6:PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the Atmel ATmega3250A/3250PA/6450A/6450P as listed on page 83.

2.3.12 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 28-13 on page 304. Shorter pulses are not guaranteed to generate a reset.

2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.16 AREF

This is the analog reference pin for the A/D Converter.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

5. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".

6. Capacitive touch sensing

The Atmel QTouch Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR microcontrollers. The QTouch Library includes support for the Atmel QTouch and QMatrix acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API's to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	125
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	124
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	122
(0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D	197
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	215
(0x7D)	Reserved	–	–	–	–	–	–	–	–	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	211
(0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	214
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	213
(0x79)	ADCH	ADC Data Register High									214
(0x78)	ADCL	ADC Data Register Low									214
(0x77)	Reserved	–	–	–	–	–	–	–	–	
(0x76)	Reserved	–	–	–	–	–	–	–	–	
(0x75)	Reserved	–	–	–	–	–	–	–	–	
(0x74)	Reserved	–	–	–	–	–	–	–	–	
(0x73)	**PCMSK3**	–	**PCINT30**	**PCINT29**	**PCINT28**	**PCINT27**	**PCINT26**	**PCINT25**	**PCINT24**	63
(0x72)	Reserved	–	–	–	–	–	–	–	–	
(0x71)	Reserved	–	–	–	–	–	–	–	–	
(0x70)	TIMSK2	–	–	–	–	–	–	OCIE2A	TOIE2	145
(0x6F)	TIMSK1	–	-	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	127
(0x6E)	TIMSK0	–	–	–	–	–	–	OCIE0A	TOIE0	101
(0x6D)	**PCMSK2**	**PCINT23**	**PCINT22**	**PCINT21**	**PCINT20**	**PCINT19**	**PCINT18**	**PCINT17**	**PCINT16**	63
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	63
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	63
(0x6A)	Reserved	–	–	–	–	–	–	–	–	
(0x69)	EICRA	–	–	–	–	–	–	ISC01	ISC00	61
(0x68)	Reserved	–	–	–	–	–	–	–	–	
(0x67)	Reserved	–	–	–	–	–	–	–	–	
(0x66)	OSCCAL	Oscillator Calibration Register [CAL7:0]									36
(0x65)	Reserved	–	–	–	–	–	–	–	–	
(0x64)	PRR	–	–	–	–	PRTIM1	PRSPI	PSUSART0	PRADC	43
(0x63)	Reserved	–	–	–	–	–	–	–	–	
(0x62)	Reserved	–	–	–	–	–	–	–	–	
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	36
(0x60)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	50
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	13
0x3E (0x5E)	SPH	Stack Pointer High									15
0x3D (0x5D)	SPL	Stack Pointer Low									15
0x3C (0x5C)	Reserved	–	–	–	–	–	–	–	–	
0x3B (0x5B)	Reserved	–	–	–	–	–	–	–	–	
0x3A (0x5A)	Reserved	–	–	–	–	–	–	–	–	
0x39 (0x59)	Reserved	–	–	–	–	–	–	–	–	
0x38 (0x58)	Reserved	–	–	–	–	–	–	–	–	
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	262
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–	
0x35 (0x55)	MCUCR	JTD	BODS	BODSE	PUD	–	–	IVSEL	IVCE	58/85/247
0x34 (0x54)	MCUSR	–	–	–	JTRF	WDRF	BORF	EXTRF	PORF	50
0x33 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE	50
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–	
0x31 (0x51)	OCDR	IDRD/OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	221
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	196
0x2F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
0x2E (0x4E)	SPDR	SPI Data Register									155
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	155
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	154
0x2B (0x4B)	GPIOR2	General Purpose I/O Register									27
0x2A (0x4A)	GPIOR1	General Purpose I/O Register									27
0x29 (0x49)	Reserved	–	–	–	–	–	–	–	–	
0x28 (0x48)	Reserved	–	–	–	–	–	–	–	–	
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare A									101
0x26 (0x46)	TCNT0	Timer/Counter0									100
0x25 (0x45)	Reserved	–	–	–	–	–	–	–	–	
0x24 (0x44)	TCCR0A	FOC0A	WGM00	COM0A1	COM0A0	WGM01	CS02	CS01	CS00	98
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	PSR2	PSR10	130/146

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x22 (0x42)	EEARH	–	–	–	–	–	EEPROM Address Register High			25
0x21 (0x41)	EEARL	EEPROM Address Register Low								25
0x20 (0x40)	EEDR	EEPROM Data Register								26
0x1F (0x3F)	EECR	–	–	–	–	EERIE	EEMWE	EEWE	EERE	26
0x1E (0x3E)	GPIOR0	General Purpose I/O Register								27
0x1D (0x3D)	EIMSK	PCIE	PCIE2	PCIE1	PCIE0	–	–	–	INT0	61
0x1C (0x3C)	EIFR	PCIF3	PCIF2	PCIF1	PCIF0	–	–	–	INTF0	62
0x1B (0x3B)	Reserved	–	–	–	–	–	–	–	–	
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	TIFR2	–	–	–	–	–	–	OCF2A	TOV2	145
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	127
0x15 (0x35)	TIFR0	–	–	–	–	–	–	OCF0A	TOV0	130
0x14 (0x34)	PORTG	–	–	–	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	87
0x13 (0x33)	DDRG	–	–	–	DDG4	DDG3	DDG2	DDG1	DDG0	87
0x12 (0x32)	PING	–	–	PING5	PING4	PING3	PING2	PING1	PING0	87
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	87
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	87
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	87
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	86
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	86
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	87
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	86
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	86
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	86
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	86
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	86
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	86
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	85
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	85
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	85
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	85
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	85
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	85

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2

9.3 ATmega325A

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operation Range
20	1.8 - 5.5V	ATmega325A-AU ATmega325A-AUR[4] ATmega325A-MU ATmega325A-MUR[4]	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega325A-AN ATmega325A-ANR[4] ATmega325A-MN ATmega325A-MNR[4]	64A 64A 64M1 64M1	Extended (-40°C to 105°C)[5]

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3. For Speed vs. V_{CC}, see Figure 28-1 on page 302.

4. Tape & Reel

5. See characterizations specifications at 105°C.

Package Type	
64A	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
64M1	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.4 ATmega325PA

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operation Range
20	1.8 - 5.5V	ATmega325PA-AU ATmega325PA-AUR[4] ATmega325PA-MU ATmega325PA-MUR[4]	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega325PA-AN ATmega325PA-ANR[4] ATmega325PA-MN ATmega325PA-MNR[4]	64A 64A 64M1 64M1	Extended (-40°C to 105°C)[5]

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 28-1 on page 302.
4. Tape & Reel
5. See characterization specifications at 105°C.

Package Type	
64A	64-Lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
64M1	64-pad, 9 x 9 x 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

9.5 ATmega3250A

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operation Range
20	1.8 - 5.5V	ATmega3250A-AU ATmega3250A-AUR[4]	100A 100A	Industrial (-40°C to 85°C)
		ATmega3250A-AN ATmega3250A-ANR[4]	100A 100A	Extended (-40°C to 105°C)[5]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 28-1 on page 302.
4. Tape & Reel
5. See characterization specifications at 105°C.

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.6   ATmega3250PA

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operation Range
20	1.8 - 5.5V	ATmega3250PA-AU ATmega3250PA-AUR[4]	100A 100A	Industrial (-40°C to 85°C)
		ATmega3250PA-AN ATmega3250PA-ANR[4]	100A 100A	Extended (-40°C to 105°C)[5]

Notes: 1.   This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2.   Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

3.   For Speed vs. V_{CC}, see Figure 28-1 on page 302.

4.   Tape & Reel

5.   See characterization specifications at 105°C.

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

9.10 ATmega6450P

Speed (MHz)[3]	Power Supply	Ordering Code[2]	Package[1]	Operation Range
20	1.8 - 5.5V	ATmega6450P-AU ATmega6450P-AUR[4]	100A 100A	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 28-1 on page 302.
4. Tape & Reel

Package Type	
100A	100-lead, 14 x 14 x 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

10.2   64M1

TOP VIEW

SIDE VIEW

BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	
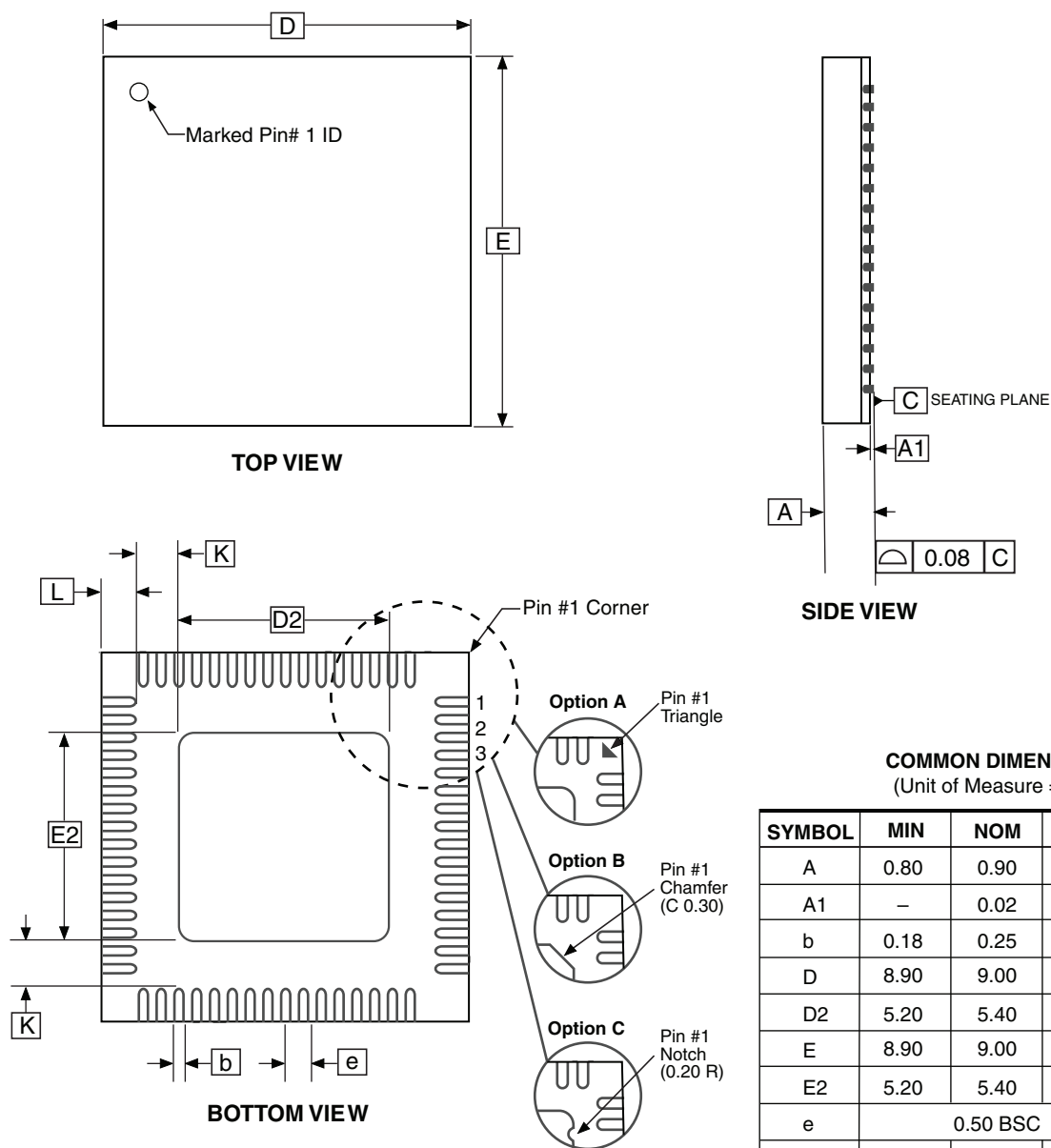
Notes:

1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

2010-10-19

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M1	H

11. Errata

11.1 ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P Rev. G

No known errata.

11.2 ATmega165A/165PA/325A/325PA/3250A/3250PA/645A/645P/6450A/6450P Rev. A to F

Not sampled.

12. Datasheet Revision History

Please note that the referring page numbers in this section are referring to this document. The referring revisions in this section are referring to the document revision.

12.1 8285F – 08/2014

1. New back page from datasheet template 2014-0502
2. Changed chip definition in the text in Section 9.6 "Low-frequency XTAL Oscillator" on page 32.

12.2 8285E – 02/2013

1. Applied partially the Atmel new template. New log, front page, page layout and last page changed.
2. Added "Electrical Characteristics – TA = -40°C to 105°C" on page 308.
3. Removed sections 28.5 and 28.6, page 326.
4. Added "Typical Characteristics – TA = -40°C to 105°C" on page 630.
5. Changed Input hysteresis (mV) to Input hysteresis (V) throughout the "Typical characteristics – TA = -40°C to 85°C" .
6. Updated the typical characteristics to include Port H for all 100-pin devices: ATmega3250A/PA/6450/P.
   Port H has the same performance as Port A, C, D, E, F, G.
7. Updated "Packaging Information" on page 28 to take into account the added the 105°C devices.

12.3 8285D – 06/11

1. Removed "Preliminary" from the front page.

12.4 8285C – 06/11

1. Updated "Signature bytes" on page 267. A, P and PA devices have different signature (0x002) bytes.
2. Updated "DC characteristics" on page 295 for all devices.

12.5   8285B – 03/11

1. Updated the datasheet according to the Atmel new Brand Style Guide

2. Updated "Signature bytes" , Table 27.3 on page 267.

3. Updated the power supply voltage (1.5 - 5.5V) for all devices in "Ordering Information" on page 18.

4. Added "Ordering Information" for Extended Temperature (-40°C to 105°C)

12.6   8285A – 09/10

1. Initial revision (Based on the ATmega165P/325P/3250P/645/6450/V).

2. Changes done compared to ATmega165P/325P/3250P/645/6450/V datasheet:

    – New EIMSK and EIFR register overview
    – New graphics in "Typical characteristics – TA = -40°C to 85°C" on page 314.
    – Ordering Information includes Tape & Reel
    – New "Ordering Information" on page 18.
    – QTouch Library Support Features