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Details	
Product Status	Last Time Buy
Core Processor	SH-3
Core Size	32-Bit Single-Core
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Peripherals	DMA, POR, PWM, WDT
Number of I/O	105
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.4V ~ 1.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
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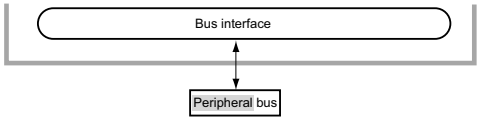
Item	Page	Revisions (See Manual for Details)
9.1 Features Figure 9.1 Block Diagram of Clock Pulse Generator	272	Figure amended 
10.2.2 Watchdog Timer Control/Status Register (WTCSR)	289	Note added Note: If manual reset is selected using the RSTS bit, a frequency division ratio of 1/16, 1/32, 1/64, 1/256, 1/1,024, or 1/4,096 is selected using bits CKS2 to CKS0, and a watchdog timer counter overflow occurs, resulting in a manual reset, the LSI will generate two manual resets in succession. This will not affect its operation but will cause change in the state of the STATUS pin.
11.6.1 Transition to Module Standby Function	301	Description amended This function can be used to reduce the power consumption in the normal mode and sleep mode.
16.5 SCIF Interrupt Sources and DMAC Table 16.4 SCIF Interrupt Sources	427	Table amended

Interrupt Source	Description	DMAC Activation
ERI	Interrupt initiated by receive error flag (ER) or break flag (BRK)	Not possible
RXI	Interrupt initiated by receive FIFO data full flag (RDF) or receive data ready (DR)	Possible*1
TXI	Interrupt initiated by transmit FIFO data empty flag (TDFE) or transmit data stop flag (TSF)	Possible*2

18.1 Features	437	Description amended • The UDC (USB device controller) conforming to USB2.0 and transceiver process USB protocol automatically.
19.2.7 Port F Control Register (PFCR)	489	Note *2 added to Bits 15 and 14 Note 2. Pull-up MOS on.
19.2.9 Port G Control Register (PGCR)	491	Note *2 added to Bits 7 to 0 Note 2. Pull-up MOS on.

Item	Features
Timer unit (TMU)	• Three-channel auto-reload-type 32-bit timer • Input capture function (only channel 2) • Five types of counter input clocks can be selected (Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, TCLK input)
Compare match timer (CMT)	• 16-bit counter • Four types of clocks can be selected (Pϕ/4, Pϕ/8, Pϕ/16, Pϕ/64)
16-bit timer pulse unit (TPU)	• Four PWM output (TO0, TO1, TO2, and TO3) • Supports PWM function
Realtime clock (RTC)	• Clock and calendar functions (BCD format) • 30-second adjust function • Alarm/periodic/carry interrupt • Automatic leap year adjustment
Serial communication interface (SCIF_0, SCIF_2)	• Clock synchronous/asynchronous mode • 64-byte transmit/receive FIFOs • High-speed UART • UART supports FIFO stop and FIFO trigger • Supports $\overline{\text{RTS}}$/$\overline{\text{CTS}}$ • Supports IrDA 1.0 (only channel 0)
USB function module (USB)	• Conforms to USB 2.0 full-speed specification • Supports modes with an on-chip and external USB transceiver • Supports control transfer (endpoint 0), bulk transfer (endpoint 1, 2), and interrupt transfer (endpoint 3) • The USB standard commands are supported, and class and bender commands are handled by firmware • On-chip FIFO buffer for endpoints (128 bytes/endpoint 1, 2) • Module input clock: 48 MHz
I/O port	• Bitwise selection of input/output for input/output port
A/D converter	• 10 bits ± 4 LSB, four channels • Input range: 0 to AVcc (max. 3.6 V)
User break controller (UBC)	• Address, data value, access type, and data size are available for setting as break conditions • Supports the sequential break function • Two break channels

Table 1.2 Pin Functions

Pin No.				
FP-208C	TBP-208A	Pin Name	I/O	Description
1	A1	VssQ	—	I/O power supply (0 V)
2	B1	Vcc-USB	—	USB power supply (3.3 V)
3	C3	D+	I/O	USB data line
4	C2	D-	I/O	USB data line
5	C1	Vss-USB	—	USB power supply (0 V)
6	D3	Vcc-RTC*5	—	RTC power supply (3.3 V)*5
7	D2	XTAL2	O	Crystal oscillator pin for on-chip RTC
8	D1	EXTAL2	I	Crystal oscillator pin for on-chip RTC
9	E4	Vss-RTC*5	—	RTC power supply (0 V)*5
10	E3	VBUS/PTM6	I / I/O	USB power supply detection / input/output port M
11	E2	MD6	I	connect to I/O power supply (0V)
12	E1	D31/PTB7/PINT15	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
13	F4	D30/PTB6/PINT14	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
14	F3	D29/PTB5/PINT13	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
15	F2	D28/PTB4/PINT12	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
16	F1	D27/PTB3/PINT11	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
17	G4	VssQ	—	I/O power supply (0 V)
18	G3	D26/PTB2/PINT10	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
19	G2	VccQ	—	I/O power supply (3.3 V)
20	G1	D25/PTB1/PINT9	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
21	H4	D24/PTB0/PINT8	I/O / I/O / I	Data bus / input/output port B / PINT interrupt
22	H3	D23/PTA7/PINT7	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
23	H2	D22/PTA6/PINT6	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
24	H1	D21/PTA5/PINT5	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
25	J4	D20/PTA4/PINT4	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
26	J2	Vss	—	Internal power supply (0 V)
27	J1	D19/PTA3/PINT3	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
28	J3	Vcc	—	Internal power supply (1.5 V)
29	K1	D18/PTA2/PINT2	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
30	K2	D17/PTA1/PINT1	I/O / I/O / I	Data bus / input/output port A / PINT interrupt
31	K3	D16/PTA0/PINT0	I/O / I/O / I	Data bus / input/output port A / PINT interrupt

Pin No. FP-208C	Pin No. TBP-208A	Pin Name	I/O	Description
180	A10	VssQ	—	I/O power supply (0 V)
181	D9	$\overline{\text{CTS2}}$/SCPT5	I / I/O	SCIF2 transmit clear / SC port
182	B9	Vss	—	I/O power supply (0 V)
183	A9	$\overline{\text{RESETM}}$	I	Manual reset request
184	C9	Vcc	—	Internal power supply (1.5 V)
185	A8	IRQ0/$\overline{\text{IRL0}}$/PTH0	I / I / I/O	External interrupt request / input/output port H
186	B8	IRQ1/$\overline{\text{IRL1}}$/PTH1	I / I / I/O	External interrupt request / input/output port H
187	C8	IRQ2/$\overline{\text{IRL2}}$/PTH2	I / I / I/O	External interrupt request / input/output port H
188	D8	IRQ3/$\overline{\text{IRL3}}$/PTH3	I / I / I/O	External interrupt request / input/output port H
189	A7	IRQ4/PTH4	I / I/O	External interrupt request / input/output port H
190	B7	IRQ5/PTE2	I / I/O	External interrupt request / input/output port E
191	C7	AUDCK/PTG4	O / I/O	AUD clock / input/output port G
192	D7	NMI	I	Nonmaskable interrupt request
193	A6	DREQ0/PTH5	I / I/O	DMA request / input/output port H
194	B6	DREQ1/PTH6	I / I/O	DMA request / input/output port H
195	C6	$\overline{\text{RESETP}}$*6	I	Power-on reset request
196	D6	CA	I	Hardware standby request
197	A5	MD3	I	Area 0 bus width setting
198	B5	MD4	I	Area 0 bus width setting
199	C5	AVss	—	Analog power supply (0 V)
200	D5	AN0/PTL0	I / I	A/D converter input / input port L
201	A4	AN1/PTL1	I / I	A/D converter input / input port L
202	B4	AN2/PTL2	I / I	A/D converter input / input port L
203	C4	AN3/PTL3	I / I	A/D converter input / input port L
204	A3	AVcc	—	Analog power supply (3.3 V)
205	B3	VssQ	—	I/O power supply (0 V)
206	D4	EXTAL_USB	I	USB clock
207	A2	XTAL_USB	O	USB clock
208	B2	VccQ	—	I/O power supply (3.3 V)

Notes: The unused pins should be handled according to table A.1, I/O Port States in Each Processing State, in Appendix.

1. The $\overline{\text{TRST}}$ pin must be driven low for a specified period when power supply is turned on regardless of whether the UDI function is used or not. As the same as the $\overline{\text{RESETP}}$ pin, the $\overline{\text{TRST}}$ pin should be driven low at the power-on set state and driven high after the power-on reset state is released.

Classification	Symbol	I/O	Name	Function
USB	EXTAL_USB	I	USB clock	USB clock input pin. (48-MHz input)
	XTAL_USB	O	USB clock	USB clock pin.
	XVDATA	I	Data input	Receive data input pin from the differential receiver.
	VBUS	I	USB power supply detection	USB-cable connection-monitor pin.
	TXDPLS	O	D+ output	D+ transmit output pin for the driver.
	TXDMNS	O	D– output	D– transmit output pin for the driver.
	DPLS	I	D+ input	D+ signal input pin from the receiver to the driver.
	DMNS	I	D– input	D– signal input pin from the receiver to the driver.
	TXENL	O	Output enable	Output enable pin for the driver.
	SUSPND	O	Suspend	Suspend-state output pin for the transceiver.
	Vcc-USB	—	USB analog power supply	USB power supply pin. When the USB is not in use, connect this pin to the port power supply (VccQ).
	Vss-USB	—	USB analog ground	USB ground pin. Connect this pin to the system power supply (Vss).
	D–	I/O	D– I/O	On-chip USB transceiver D–.
	D+	I/O	D+ I/O	On-chip USB transceiver D+.

2.5 Features of CPU Core Instructions

2.5.1 Instruction Execution Method

Instruction Length: All instructions have a fixed length of 16 bits and are executed in the sequential pipeline. In the sequential pipeline, almost all instructions can be executed in one cycle. All data items are handles in longword (32 bits). Memory can be accessed in byte, word, or longword. In this case, Memory byte or word data is sign-extended and operated on as longword data. Immediate data is sign-extended to longword size for arithmetic operations (MOV, ADD, and CMP/EQ instructions) or zero-extended to longword size for logical operations (TST, AND, OR, and XOR instructions).

Load/Store Architecture: Basic operations are executed between registers. In operations involving memory, data is first loaded into a register (load/store architecture). However, bit manipulation instructions such as AND are executed directly on memory.

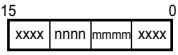
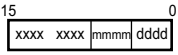
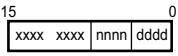
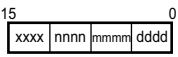
Delayed Branching: Unconditional branch instructions are executed as delayed branches. With a delayed branch instruction, the branch is made after execution of the instruction (called the slot instruction) immediately following the delayed branch instruction. This minimizes disruption of the pipeline when a branch is made.

This LSI supports two types of conditional branch instructions: delayed branch instruction or normal branch instruction.

```
Example:  BRA     TARGET
          ADD     R1, R0      ; ADD is executed before branching to the TARGET
```

T Bit: The result of a comparison is indicated by the T bit in the status register (SR), and a conditional branch is performed according to whether the result is True or False. Processing speed has been improved by keeping the number of instructions that modify the T bit to a minimum.

```
Example:  ADD     #1, R0      ; The T bit cannot be modified by the ADD instruction
          CMP/EQ  #0, R0      ; The T bit is set to 1 if R0 is 0.
          BT      Target      ; Branch to TARGET if the T bit is set to 1 (R0=0).
```

Instruction Format	Source Operand	Destination Operand	Sample Instruction
nm type 	mmmm: register direct	nnnn: register direct	ADD Rm,Rn
	mmmm: register indirect	nnnn: register indirect	MOV.L Rm,@Rn
	mmmm: post-increment register indirect (multiply-and-accumulate operation) nnnn: * post-increment register indirect (multiply-and-accumulate operation)	MACH, MACL	MAC.W @Rm+,@Rn+
	mmmm: post-increment register indirect	nnnn: register direct	MOV.L @Rm+,Rn
	mmmm: register direct	nnnn: pre-decrement register indirect	MOV.L Rm,@-Rn
	mmmm: register direct	nnnn: indexed register indirect	MOV.L Rm,@(R0,Rn)
md type 	mmmmdddd: register indirect with displacement	R0 (register direct)	MOV.B @(disp,Rm),R0
nd4 type 	R0 (register direct)	nnnndddd: register indirect with displacement	MOV.B R0,@(disp,Rn)
nmd type 	mmmm: register direct	nnnndddd: register indirect with displacement	MOV.L Rm,@(disp,Rn)
	mmmmdddd: register indirect with displacement	nnnn: register direct	MOV.L @(disp,Rm),Rn

3.1.1 MMU of This LSI

Virtual Address Space: This LSI supports a 32-bit virtual address space that enables access to a 4-Gbyte address space. As shown in figures 3.2 and 3.3, the virtual address space is divided into several areas. In privileged mode, a 4-Gbyte space comprising areas P0 to P4 is accessible. In user mode, a 2-Gbyte space of U0 area is accessible. Access to any area excluding the U0 area in user mode will result in an address error.

If the MMU is enabled by setting the AT bit of the MMUCR register to 1, P0, P3, and U0 areas can be used as any physical address area in 1- or 4-kbyte page units. By using an 8-bit address space identifier, P0, P2, and U0 areas can be increased to up to 256 areas. Mapping from virtual address to 29-bit physical address can be achieved by the TLB.

1. P0, P3, and U0 Areas

   The P0, P3, and U0 areas can be address translated by the TLB and can be accessed through the cache. If the MMU is enabled, these areas can be mapped to any physical address space in 1- or 4-kbyte page units via the TLB. If the CE bit in the cache control register (CCR1) is set to 1 and if the corresponding cache enable bit (C bit) of the TLB entry is set to 1, access via the cache is enabled. If the MMU is disabled, replacing the upper three bits of an address in these areas with 0s creates the address in the corresponding physical address space. If the CE bit of the CCR1 register is set to 1, access via the cache is enabled. When the cache is used, either the copy-back or write-through mode is selected for write access via the WT bit in CCR1.

   If these areas are mapped to the on-chip module control register area in area 1 in the physical address space via the TLB, the C bit of the corresponding page must be cleared to 0.

2. P1 Area

   The P1 area can be accessed via the cache and cannot be address-translated by the TLB. Whether the MMU is enabled or not, replacing the upper three bits of an address in these areas with 0s creates the address in the corresponding physical address space. Use of the cache is determined by the CE bit in the cache control register (CCR1). When the cache is used, either the copy-back or write-through mode is selected for write access by the CB bit in the CCR1 register.

3. P2 Area

   The P2 area cannot be accessed via the cache and cannot be address-translated by the TLB. Whether the MMU is enabled or not, replacing the upper three bits of an address in this area with 0s creates the address in the corresponding physical address space.

4. P4 Area

   The P4 area is mapped to the on-chip module control register of this LSI. This area cannot be accessed via the cache and cannot be address-translated by the TLB. Figure 3.4 shows the configuration of the P4 area.

Section 5 Exception Handling

Exception handling is separate from normal program processing, and is performed by a routine separate from the normal program. For example, if an attempt is made to execute an undefined instruction code or an instruction protected by the CPU processing mode, a control function may be required to return to the source program by executing the appropriate operation or to report an abnormality and carry out end processing. In addition, a function to control processing requested by LSI on-chip modules or an LSI external module to the CPU may also be required.

Transferring control to a user-defined exception processing routine and executing the process to support the above functions are called exception handling. This LSI has two types of exceptions: general exceptions and interrupts. The user can execute the required processing by assigning exception handling routines corresponding to the required exception processing and then return to the source program.

A reset input can terminate the normal program execution and pass control to the reset vector after register initialization. This reset operation can also be regarded as an exception handling. This section describes an overview of the exception handling operation. Here, general exceptions and interrupts are referred to as exception handling. For interrupts, this section describes only the process executed for interrupt requests. For details on how to generate an interrupt request, refer to section 6, Interrupt Controller (INTC).

5.1 Register Descriptions

There are five registers for exception handling. A register with an undefined initial value should be initialized by the software. Refer to section 24, List of Registers, for the addresses and access sizes of these registers.

- TRAPA exception register (TRA)
- Exception event register (EXPEVT)
- Interrupt event register (INTEVT)
- Interrupt event register 2 (INTEVT2)
- Exception address register (TEA)

5.1.4 Interrupt Event Register 2 (INTEVT2)

INTEVT2 is assigned to address H'A4000000 and consists of a 12-bit exception code. Exception codes to be specified in INTEVT2 are those for interrupt requests. These exception codes are automatically specified by the hardware when an exception occurs. INTEVT2 cannot be modified using the software.

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	INTEVT2	—	R	12-bit Exception Code

5.1.5 Exception Address Register (TEA)

TEA is assigned to address H'FFFFFFFC and stores the logical address for an exception occurrence when an exception related to memory accesses occurs. TEA can be modified using the software.

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TEA	—	R/W	Logical address for exception occurrence

6.3.1 Interrupt Priority Level Setting Registers A to H (IPRA to IPRH)

IPRA to IPRH are 16-bit readable/writable registers in which priority levels from 0 to 15 are set for on-chip peripheral module, and IRQ and PINT interrupts.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	IPR15 to IPR0	0	R/W	These bits set the priority level for each interrupt source in 4-bit units. For details, see table 6.2.

Table 6.2 Interrupt Sources and IPRA to IPRH

Register	Bits 15 to 12	Bits 11 to 8	Bits 7 to 4	Bits 3 to 0
IPRA	TMU0	TMU1	TMU2	RTC
IPRB	WDT	REF	Reserved*	Reserved*
IPRC	IRQ3	IRQ2	IRQ1	IRQ0
IPRD	PINT0 to PINT7	PINT8 to PINT15	IRQ5	IRQ4
IPRE	DMAC	SCIF0	SCIF2	ADC
IPRF	Reserved*	Reserved*	USB	Reserved*
IPRG	TPU0	TPU1	Reserved*	Reserved*
IPRH	TPU2	TPU3	Reserved*	Reserved*

Note: * Always read as 0. The write value should always be 0.

As shown in table 6.2, on-chip peripheral module, or IRQ or PINT interrupts are assigned to four 4-bit groups in each register. These 4-bit groups (bits 15 to 12, bits 11 to 8, bits 7 to 4, and bits 3 to 0) are set with values from H'0 (0000) to H'F (1111). Setting H'0 means priority level 0 (masking is requested); H'F means priority level 15 (the highest level).

CS3WCR

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	TRP1	0	R/W	Number of Cycles from Auto-precharge/PRE Command to ACTV Command Specify the number of minimum cycles from the start of auto-precharge or issuing of PRE command to the issuing of ACTV command for the same bank. The setting for areas 2 and 3 is common. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
13	TRP0	0	R/W	
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11	TRCD1	0	R/W	Number of Cycles from ACTV Command to READ(A)/WRIT(A) Command Specify the number of minimum cycles from issuing ACTV command to issuing READ(A)/WRIT(A) command. The setting for areas 2 and 3 is common. 00: 1 cycle 01: 2 cycles 10: 3 cycles 11: 4 cycles
10	TRCD0	1	R/W	
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
8	A3CL1	1	R/W	CAS Latency for Area 3 Specify the CAS latency for area 3. 00: Setting prohibited. 01: 2 cycles 10: 3 cycles 11: Setting prohibited
7	A3CL0	0	R/W	

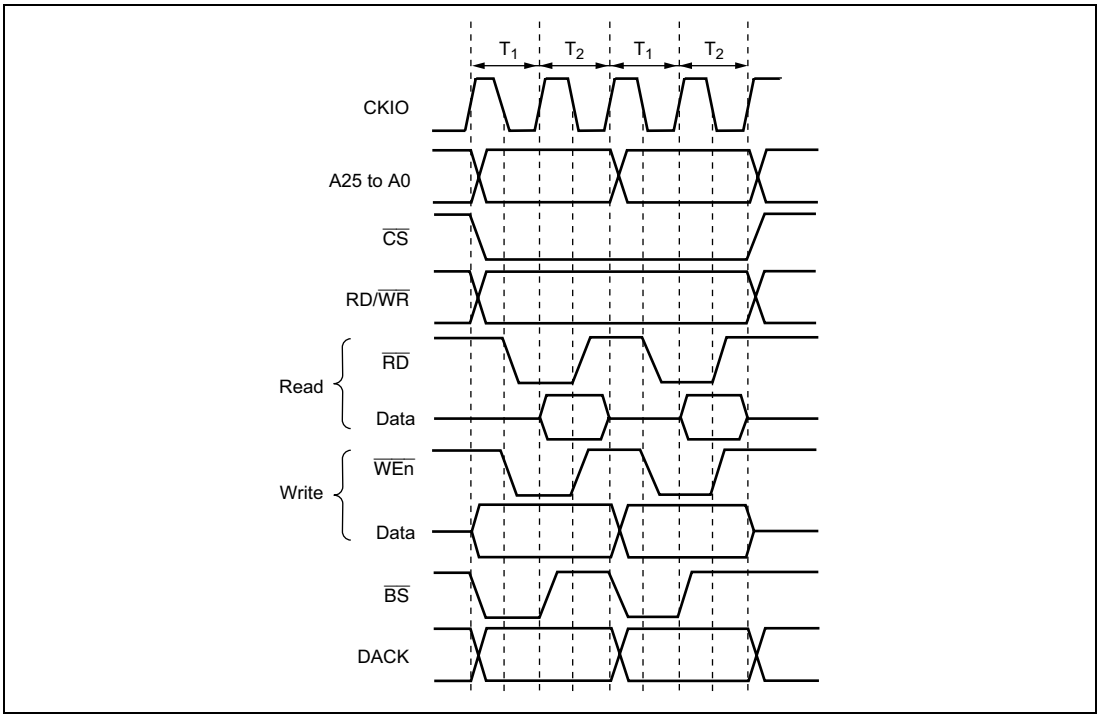


Figure 7.3 Continuous Access for Normal Space (No Wait, WM Bit in CSnWCR = 1, 16-Bit Bus Width, Longword Access, No Wait State between Cycles)

8.2 Input/Output Pins

The external pins for the DMAC are described below.

Table 8.1 lists the configuration of the pins that are connected to external bus. The DMAC has pins for 2 channels (channels 0 and 1) for external bus use. Channel 0 has the DMA transfer end signal.

Table 8.1 Pin Configuration

Channel	Name	Symbol	I/O	Function
0	DMA transfer request	DREQ0	I	DMA transfer request input from external device to channel 0
	DMA transfer request acknowledge	DACK0	O	DMA transfer request acknowledge output from channel 0 to external device
	DMA transfer end	TEND0	O	Transfer end output in channel 0
1	DMA transfer request	DREQ1	I	DMA transfer request input from external device to channel 1
	DMA transfer request acknowledge	DACK1	O	DMA transfer request acknowledge output from channel 1 to external device

8.3 Register Descriptions

The DMAC has the following registers. See section 24, List of Registers, for the addresses of these registers and the states of them in each processing state. The SAR for channel 0 is expressed such as SAR_0.

1. Channel 0
- DMA source address register_0 (SAR_0)
- DMA destination address register_0 (DAR_0)
- DMA transfer count register_0 (DMATCR_0)
- DMA channel control register_0 (CHCR_0)

2. Channel 1
- DMA source address register_1 (SAR_1)
- DMA destination address register_1 (DAR_1)
- DMA transfer count register_1 (DMATCR_1)
- DMA channel control register _1 (CHCR_1)

16.4.3 Serial Operation in Asynchronous Mode

1. Data Transfer Format

Table 16.3 shows the transfer formats that can be used in asynchronous mode. Any of eight transfer formats can be selected according to the SCSMR settings.

Table 16.3 Serial Transfer Formats

SCSMR Settings			Serial Transfer Format and Frame Length											
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	S	8-bit data								STOP		
		1	S	8-bit data								STOP	STOP	
	1	0	S	8-bit data								P	STOP	
		1	S	8-bit data								P	STOP	STOP
1	0	0	S	7-bit data							STOP			
		1	S	7-bit data							STOP	STOP		
	1	0	S	7-bit data							P	STOP		
		1	S	7-bit data							P	STOP	STOP	

S: Start bit
STOP: Stop bit
P: Parity bit

3. Data Stage (Control-Out)

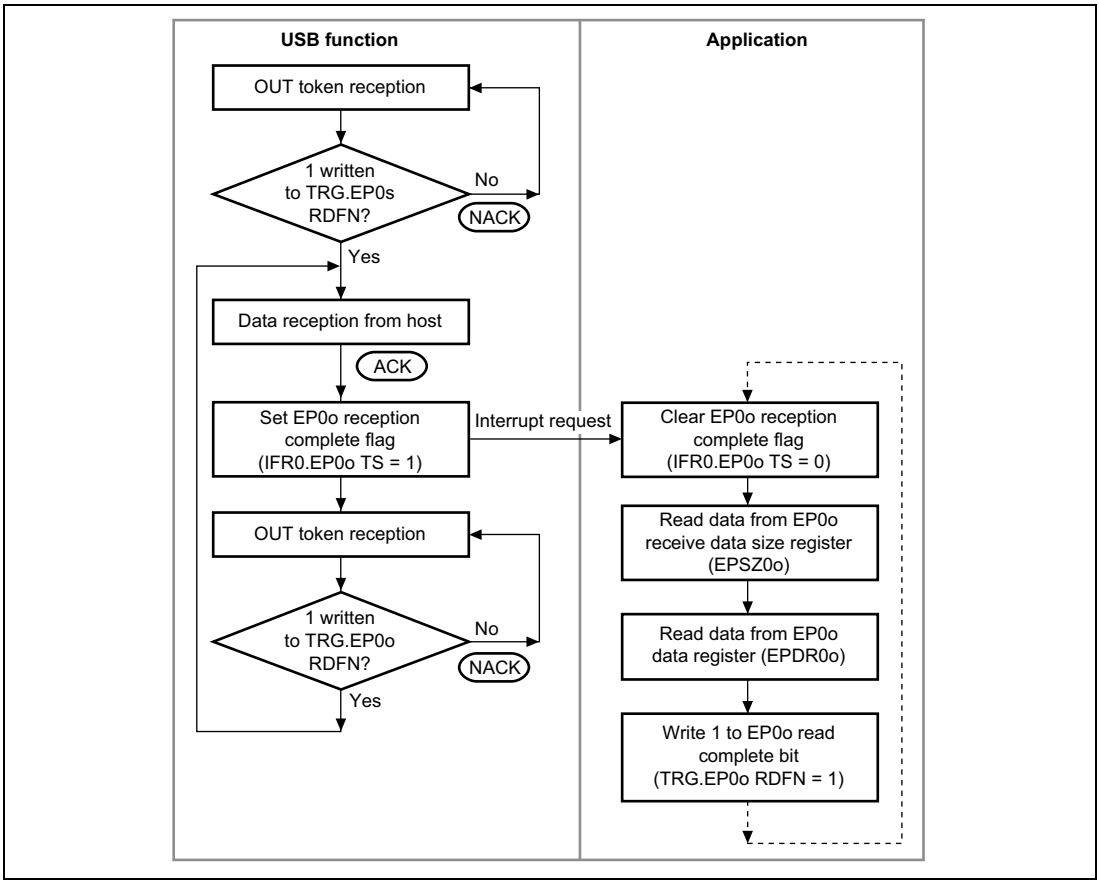


Figure 18.7 Data Stage (Control-Out) Operation

The application first analyzes command data from the host in the setup stage, and determines the subsequent data stage direction. If the result of command data analysis is that the data stage is out-transfer, the application waits for data from the host, and after data is received (EP0oTS bit in IFR0 = 1), reads data from the FIFO. Next, the application writes 1 to the EP0o read complete bit, empties the receive FIFO, and waits for reception of the next data.

The end of the data stage is identified when the host transmits an IN token and the status stage is entered.

Bit	Bit Name	Initial Value	R/W	Description
5	PA2MD1	0	R/W	PTA2 Mode
4	PA2MD0	0	R/W	00: Other functions (see table 19.1) 01: Port output 10: Port input (pull-up MOS: On) 11: Port input (pull-up MOS: Off)
3	PA1MD1	0	R/W	PTA1 Mode
2	PA1MD0	0	R/W	00: Other functions (see table 19.1) 01: Port output 10: Port input (pull-up MOS: On) 11: Port input (pull-up MOS: Off)
1	PA0MD1	0	R/W	PTA0 Mode
0	PA0MD0	0	R/W	00: Other functions (see table 19.1) 01: Port output 10: Port input (pull-up MOS: On) 11: Port input (pull-up MOS: Off)

19.2.2 Port B Control Register (PBCR)

PBCR is a 16-bit readable/writable register that selects the pin function and input pull-up MOS control.

Bit	Bit Name	Initial Value	R/W	Description
15	PB7MD1	0	R/W	PTB7 Mode
14	PB7MD0	0	R/W	00: Other functions (see table 19.1) 01: Port output 10: Port input (pull-up MOS: On) 11: Port input (pull-up MOS: Off)
13	PB6MD1	0	R/W	PTB6 Mode
12	PB6MD0	0	R/W	00: Other functions (see table 19.1) 01: Port output 10: Port input (pull-up MOS: On) 11: Port input (pull-up MOS: Off)

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	PF7DT to PF0DT	0	R/W	Table 20.6 shows the function of PFDR.

Table 20.6 Port F Data Register (PFDR) Read/Write Operations

PFCR State				
PFnMD1	**PFnMD0**	**Pin State**	**Read**	**Write**
0	0	Other function	PFDR value	Data can be written to PFDR but no effect on pin state.
	1	Output	PFDR value	Written data is output from the pin.
1	0	Input (Pull-up MOS on)	Pin state	Data can be written to PFDR but no effect on pin state.
	1	Input (Pull-up MOS off)	Pin state	Data can be written to PFDR but no effect on pin state.

Note: n = 0 to 7

20.7 Port G

Port G is an 8-bit input port with the pin configuration shown in figure 20.7. Each pin has an input pull-up MOS, which is controlled by the port G control register (PGCR) in the PFC.

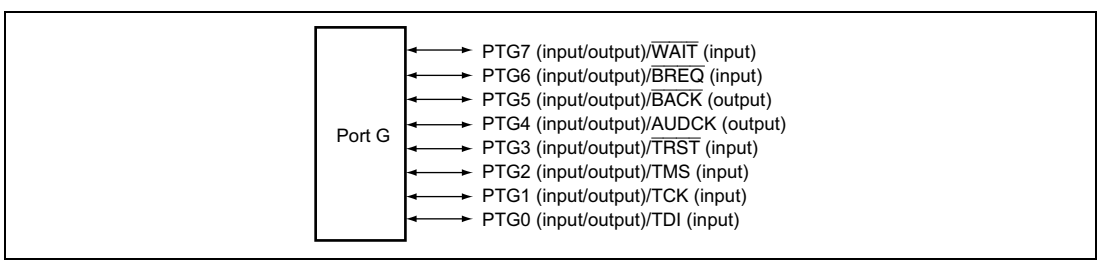


Figure 20.7 Port G

20.7.1 Register Description

Port G has the following register. For details on the register address and access size, see section 24, List of Registers.

- Port G data register (PGDR)

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	PN7DT to PN0DT	0	R/W	Table 20.13 shows the function of PNDR.

Table 20.13 Port N Data Register (PNDR) Read/Write Operations

PNCR State				
PNnMD1	**PNnMD0**	**Pin State**	**Read**	**Write**
0	0	Other function	PNDR value	Data can be written to PNDR but no effect on pin state.
	1	Output	PNDR value	Written data is output from the pin.
1	0	Input (Pull-up MOS on)	Pin state	Data can be written to PNDR but no effect on pin state.
	1	Input (Pull-up MOS off)	Pin state	Data can be written to PNDR but no effect on pin state.

Note: n = 0 to 7

20.14 SC Port

The SC port is an 8-bit input/output port with the pin configuration shown in figure 20.14. Each pin has an input pull-up MOS, which is controlled by the SC port control register (SCPCR) in the PFC.

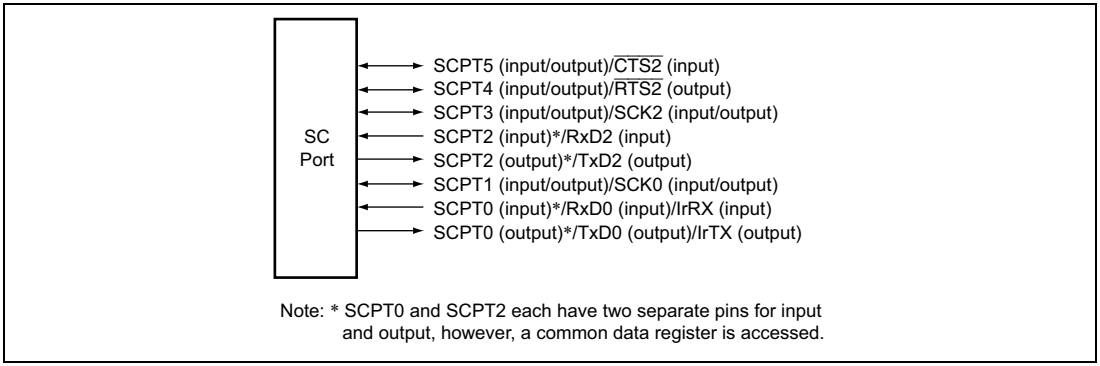


Figure 20.14 SC Port

23.2 Input/Output Pins

Table 23.1 shows the pin configuration of the UDI.

Table 23.1 Pin Configuration

Pin Name	Input/Output	Description
TCK*	Input	Serial Data Input/Output Clock Pin Data is serially supplied to the UDI from the data input pin (TDI), and output from the data output pin (TDO), in synchronization with this clock.
TMS*	Input	Mode Select Input Pin The state of the TAP control circuit is determined by changing this signal in synchronization with TCK. The protocol is supported to the JTAG standard (IEEE Std.1149.1).
$\overline{\text{TRST}}$*	Input	Reset Input Pin Input is accepted asynchronously with respect to TCK, and when low, the UDI is reset. $\overline{\text{TRST}}$ must be held low for a constant period when power is turned on regardless of using the UDI function. As the same as the $\overline{\text{RESETP}}$ pin, the $\overline{\text{TRST}}$ pin should be driven low at the power-on reset state and driven high after the power-on reset state is released. This is different from the JTAG standard. See section 23.4.2, Reset Configuration, for more information.
TDI*	Input	Serial Data Input Pin Data transfer to the UDI is executed by changing this signal in synchronization with TCK.
TDO	Output	Serial Data Output Pin Data read from the UDI is executed by reading this pin in synchronization with TCK. The data output timing depends on the command type set in the SDIR. See section 23.3.2, Instruction Register (SDIR), for more information.
$\overline{\text{ASEMD0}}$*	Input	ASE Mode Select Pin If a low level is input at the $\overline{\text{ASEMD0}}$ pin while the $\overline{\text{RESETP}}$ pin is asserted, ASE mode is entered; if a high level is input, normal mode is entered. In ASE mode, dedicated emulator function can be used. The input level at the $\overline{\text{ASEMD0}}$ pin should be held for at least one cycle after $\overline{\text{RESETP}}$ negation. See section 23.4.2, Reset Configuration, for more information.