Analog Devices Inc./Maxim Integrated - DS80C410-FNY+ Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	75MHz
Connectivity	1-Wire®, CANbus, EBI/EMI, Ethernet, SIO, UART/USART
Peripherals	Power-Fail Reset, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/ds80c410-fny

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Note 2: The user should note that this part is tested and guaranteed to operate down to V_{CC3} = 3.0V and V_{CC1} = 1.62V, while the reset thresholds for those supplies, V_{RST3} and V_{RST1} respectively, may be above or below those points. When the reset threshold for a given supply is greater than the guaranteed minimum operating voltage, that reset threshold should be considered the minimum operating point since execution ceases once the part enters the reset state. When the reset threshold for a given supply is lower than the guaranteed minimum operating voltage, there exists a range of voltages for either supply, (V_{RST3} < V_{CC3} < 1.62V) or (V_{RST1} < V_{CC1} < 3.0V), where the processor's operation is not guaranteed, and the reset trip point has not been reached. This should not be an issue in most applications, but should be considered when proper operation must be maintained at all times. For these applications, it may be desirable to use a more accurate external reset.

Note 3: While the specifications for V_{PFW3} and V_{RST3} overlap, the design of the hardware makes it such that this is not possible. Within the ranges given, there is a guaranteed separation between these two voltages.

Note 4: Current measured with 75MHz clock source on XTAL1, V_{CC3} = 3.6V, V_{CC1} = 2.0V, $\overline{EA}$ and RST = 0V, Port0 = V_{CC3}, all other pins disconnected.

Note 5: While the specifications for V_{PFW1} and V_{RST1} overlap, the design of the hardware makes it such that this is not possible. Within the ranges given, there will be a guaranteed separation between these two voltages.

Note 6: Certain pins exhibit stronger drive capability when being used to address external memory. These pins and associated memory interface function (in parentheses) are as follows: Port 3.6-3.7 ($\overline{WR}$, $\overline{RD}$), Port 4 ($\overline{CE0\text{-}3}$, A16-A19), Port 5.4-5.7 ($\overline{PCE0\text{-}3}$), Port 6.0-6.5 ($\overline{CE4\text{-}7}$, A20, A21), Port 7 (demultiplexed mode A0-A7).

Note 7: This measurement reflects the weak I/O pullup state that persists following the momentary strong 0 to 1 port pin drive (V_{OH2}). This I/O pin state can be achieved by applying RST = V_{CC3}.

Note 8: The measurement reflects the momentary strong port pin drive during a 0-to-1 transition in I/O mode. During this period, a one shot circuit drives the ports hard for two clock cycles. A weak pullup device (V_{OH1}) remains in effect following the strong two-clock cycle drive. If a port 4 or 6 pin is functioning in memory mode with pin state of 0 and the SFR bit contains a 1, changing the pin to an I/O mode (by writing to P4CNT, for example) does not enable the two-cycle strong pullup.

Note 9: Port 3 pins 3.6 ($\overline{WR}$) and 3.7($\overline{RD}$) have a stronger than normal pullup drive for only one system clock period following the transition of either $\overline{WR}$ or $\overline{RD}$ from a 0 to a 1.

Note 10: This is the current required from an external circuit to hold a logic low level on an I/O pin while the corresponding port latch bit is set to 1. This is only the current required to hold the low level; transitions from 1 to 0 on an I/O pin also have to overcome the transition current.

Note 11: Following the 0 to 1 one-shot timeout, ports in I/O mode source transition current when being pulled down externally. It reaches a maximum at approximately 2V.

Note 12: During external addressing mode, weak latches are used to maintain the previously driven state on the pin until such time that the Port 0 pin is driven by an external memory source.

Note 13: The OW pin (when configured to output a 1) at V_{IN} = 5.5V, $\overline{EA}$, $\overline{MUX}$, and all MII inputs (TXCLk, RXCLk, RX_DV, RX_ER, RXD[3:0], CRS, COL, MDIO) at V_{IN} = 3.6V.

AC ELECTRICAL CHARAC TERISTICS (MULTIPLEXED ADDRESS/DATA BUS)

(V_{CC3} = 3.0V to 3.6V, V_{CC1} = 1.8V ±10%, T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	75MHz		VARIABLE CLOCK		UNITS
		MIN	MAX	MIN	MAX	
External Crystal Frequency	1 / t_{CLK}			4	40	MHz
Clock Mutliplier 2X Mode				16	37.5	
Clock Multiplier 4X Mode				11	18.75	
External Clock Oscillator Frequency	1 / t_{CLK}			DC	75	MHz
Clock Mutliplier 2X Mode				16	37.5	
Clock Multiplier 4X Mode				11	18.75	
ALE Pulse Width	t_{LHLL}	15.0		t_{CLCL} + t_{CHCL} - 5		ns
Port 0 Instruction Address Valid to ALE Low	t_{AVLL}	1.7		t_{CHCL} - 5		ns
Address Hold After ALE Low	t_{LLAX}	4.7		t_{CLCH} - 2		ns
ALE Low to Valid Instruction In	t_{LLIV}		14.3		$2t_{CLCL}$ + t_{CLCH} - 19	ns
ALE Low to $\overline{PSEN}$ Low	t_{LLPL}	3.7		t_{CLCH} - 3		ns
$\overline{PSEN}$ Pulse Width	t_{PLPH}	21.7		$2t_{CLCL}$ - 5		ns
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		8.7		$2t_{CLCL}$ -18	ns
Input Instruction Hold After $\overline{PSEN}$	t_{PXIX}	0		0		ns
Input Instruction Float After $\overline{PSEN}$	t_{PXIZ}		8.3		t_{CLCL} - 5	ns
Port 0 Address to Valid Instruction In	t_{AVIV0}		21.0		$3t_{CLCL}$ - 19	ns
Port 2, 4, 6 Address or Port 4 CE to Valid Instruction In	t_{AVIV2}		24.7		$3t_{CLCL}$ + t_{CLCH} - 22	ns
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}		0		0	ns

Note 1: AC electrical characteristics assume 50% duty cycle for the oscillator, oscillator frequency ≤ 75MHz, and are not 100% production tested, but are guaranteed by design.

Note 2: All parameters apply to both commercial and industrial temperature operation, unless otherwise noted.

Note 3: t_{CLCL}, t_{CLCH}, t_{CHCL} are time periods associated with the internal system clock and are related to the external clock (t_{CLK}) as defined in the External Clock Oscillator (XTAL1) Characteristics table.

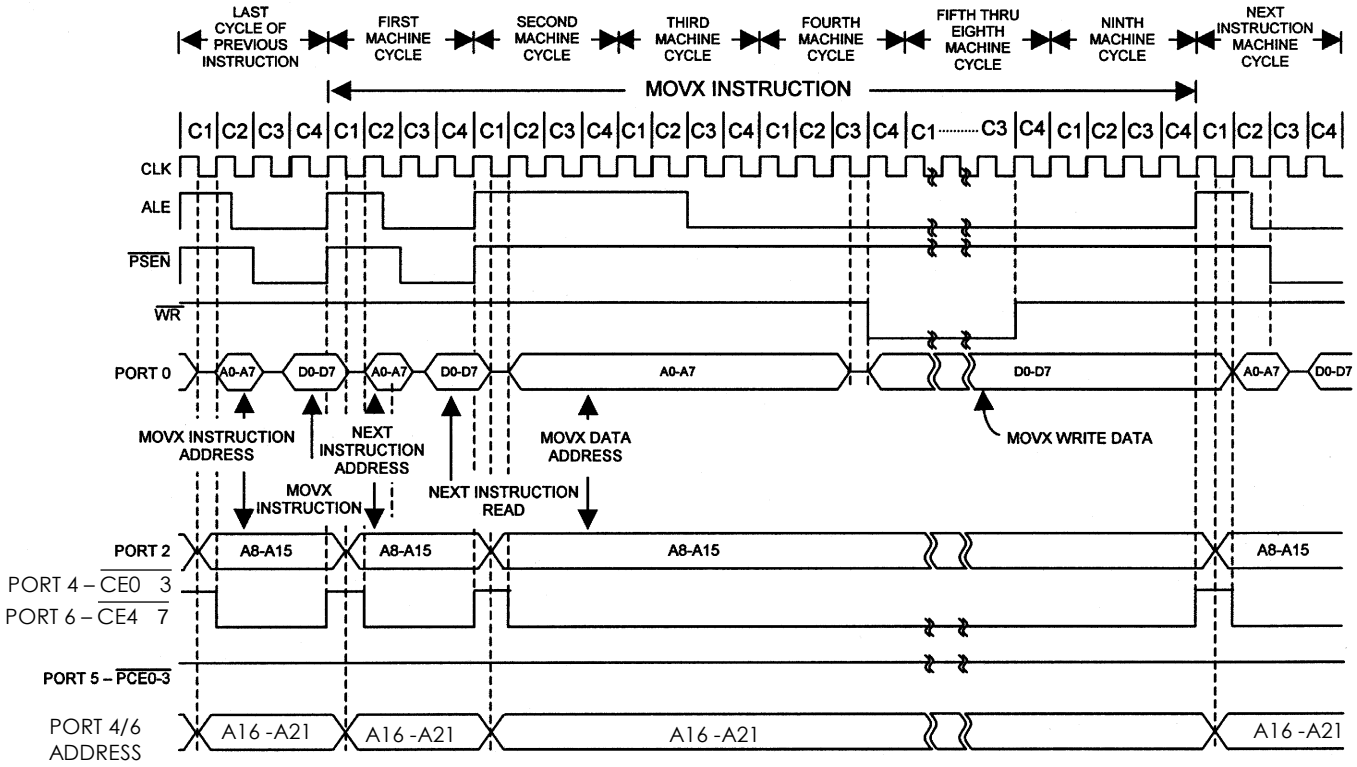
Note 4: The precalculated 75MHz MIN/MAX timing specifications assume an exact 50% duty cycle.

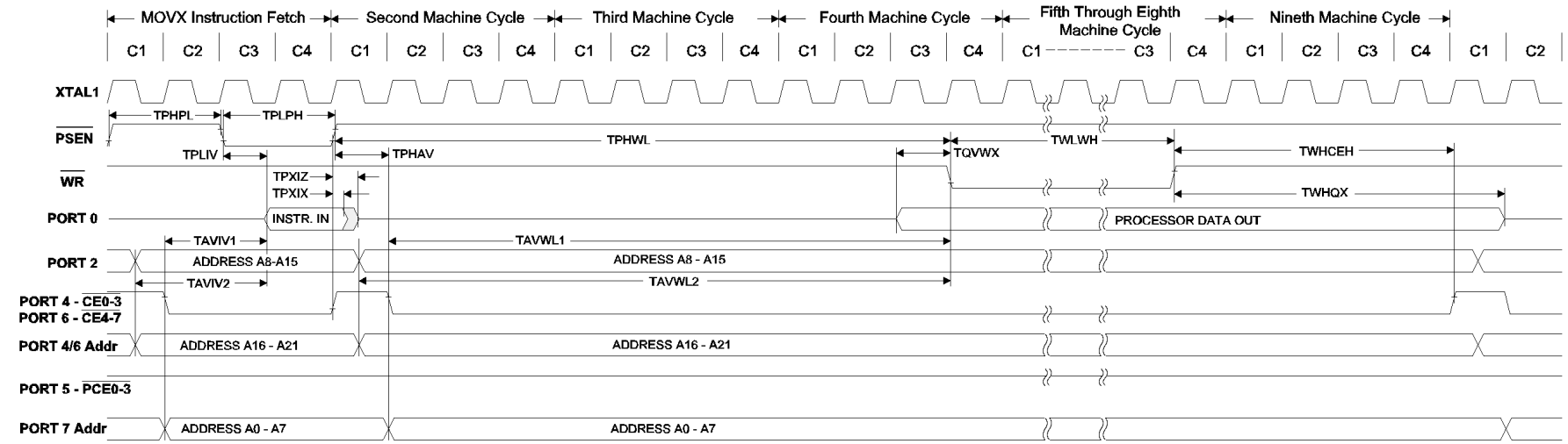
Note 5: All signals guaranteed with load capacitance of 80pF except Port 0, Port 2, $\overline{ALE}$, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF. The following signals, when configured for memory interface, are also characterized with 100pF loading: Port 4 ($\overline{CE0\text{-}3}$, A16–A19), Port 5.4–5.7 ($\overline{PCE0\text{-}3}$), Port 6.0–6.5 ($\overline{CE4\text{-}7}$, A20, A21), Port 7 (demultiplexed mode A0–A7).

Note 6: For high-frequency operation, special attention should be paid to the float times of the interfaced memory devices so as to avoid bus contention.

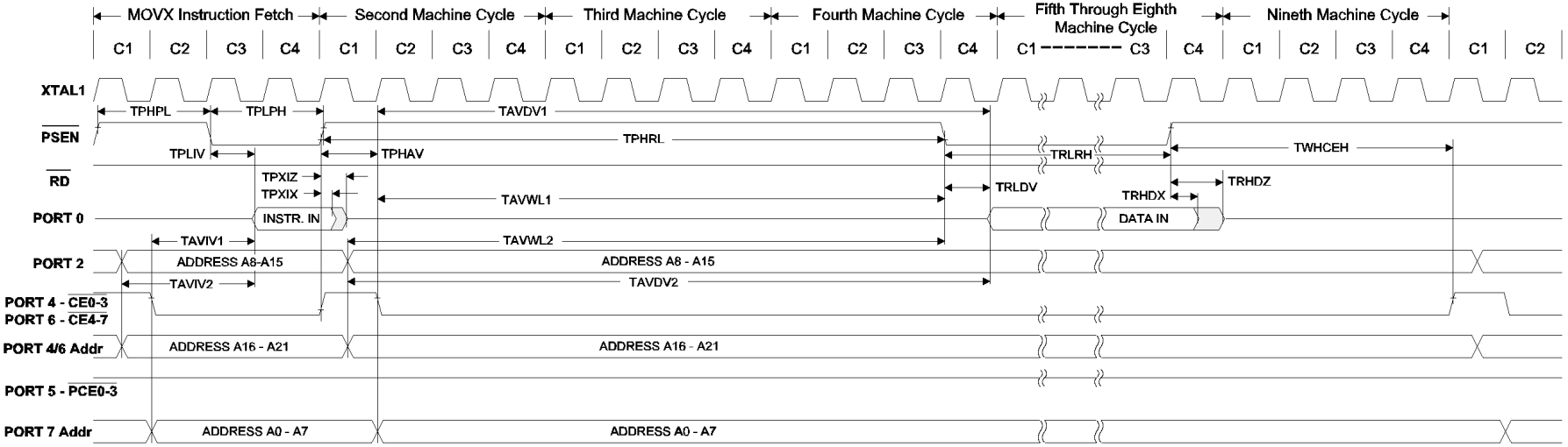
Note 7: References to the XTAL, XTAL1 or CLK signal in timing diagrams is to assist in determining the relative occurrence of events, not for determing absolute signal timing with respect to the external clock.

MULTIPLEXED, 9-CYCLE DATA MEMORY $\overline{CE0\text{-}7}$ WRITE





Non-Multiplexed Address/Data 9 Cycle CE0-7 MOVX Write



Non-Multiplexed Address/Data 9 Cycle CE0-7 MOVX Read

PIN	NAME	FUNCTION
50	P6.6	P6.3 $\overline{CE7}$ Program Memory Chip Enable 7 P6.4 A20 Program/Data Memory Address 20 P6.5 A21 Program/Data Memory Address 21 P6.6 RXD2 Serial Port 2 Receive P6.7 TXD2 Serial Port 2 Transmit
49	P6.7	
78	A0	Port 7, I/O. Port 7 can function as either an 8-bit, bidirectional I/O port or the nonmultiplexed A0–A7 signals (when the $\overline{MUX}$ pin = 1). The reset condition of Port 7 is all bits at logic 1 through a weak pullup. The logic 1 state also serves as an input mode, since external circuits writing to the port can override the weak pullup. When software clears any port pin to 0, a strong pulldown is activated that remains on until either a 1 is written to the port pin or a reset occurs. Writing a 1 after the port has been at 0 activates a strong transition driver, followed by a weaker sustaining pullup. Once the momentary strong driver turns off, the port once again becomes the output (and input) high state. Port Alternate Function P7.0 A0 Program/Data Memory Address 0 P7.1 A1 Program/Data Memory Address 1 P7.2 A2 Program/Data Memory Address 2 P7.3 A3 Program/Data Memory Address 3 P7.4 A4 Program/Data Memory Address 4 P7.5 A5 Program/Data Memory Address 5 P7.6 A6 Program/Data Memory Address 6 P7.7 A7 Program/Data Memory Address 7
77	A1	
76	A2	
75	A3	
74	A4	
73	A5	
72	A6	
71	A7	
8	TXClk	Transmit Clock, Input. The transmit clock is a continuous clock sourced from the Ethernet PHY controller. It is used to provide timing reference for transferring of TX_EN and TXD[3:0] signals from the MAC to the external Ethernet PHY controller. The input clock frequency of TXClk should be 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. For ENDEC operation, TXClk serves the same function, but the input clock frequency should be 10MHz.
7	TX_EN	Transmit Enable, Output. The transmit enable is an active-high output and is synchronous with respect to the TXClk signal. TX_EN is used to indicate valid nibbles of data for transmission on the MII pins TXD.3–TXD.0. TX_EN is asserted with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented on the TXD.3–TXD.0 pins. TX_EN negates prior to the first TXClk following the final nibble of the frame. TX_EN serves the same function for ENDEC operation.
3	TXD.3	Transmit Data, Output. The transmit data outputs provide 4-bit nibbles of data for transmission over the MII. The transmit data is synchronous with respect to the TXClk signal. For each TXClk period when TX_EN is asserted, TXD.3–TXD.0 provides the data for transmission to the Ethernet PHY controller. When TX_EN is deasserted, the TXD data should be ignored. For ENDEC operation, only TXD.0 is used for transmission of frames.
4	TXD.2	
5	TXD.1	
6	TXD.0	
10	RXClk	Receive Clock, Input. The receive clock is a continuous clock sourced from the Ethernet PHY controller. It is used to provide timing reference for transferring of RX_DV, RX_ER, and RXD[3:0] signals from the external Ethernet PHY controller to the MAC. The input clock frequency of RXClk should be 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. For ENDEC operation, RXClk serves the same function, but the input clock frequency should be 10MHz.
11	RX_DV	Receive Data Valid, Input. The receive data valid is an active-high input from the external Ethernet PHY controller and is synchronous with respect to the RXClk signal. RX_DV is used to indicate valid nibbles of data for reception on the MII pins RXD.3–RXD.0. RX_DV is asserted continuously from the first nibble of the frame through the final nibble. RX_DV negates prior to the first RXClk following the final nibble. RX_DV serves the same function for ENDEC operation.
9	RX_ER	Receive Error, Input. The receive error is an active-high input from the external Ethernet PHY controller and is synchronous with respect to the RXClk signal. RX_ER is used to indicate to the MAC that an error (e.g., a coding error, or any error detectable by the PHY) was detected somewhere in the frame presently being transmitted by the PHY. RX_ER has no effect on the MAC while RX_DV is deasserted. RX_ER should be low for ENDEC operation.
17	RXD.3	Receive Data, Input. The receive data inputs provide 4-bit nibbles of data for reception over the MII. The receive data is synchronous with respect to the RXClk signal. For each RXClk period when RX_DV is asserted, RXD.3–RXD.0 have the data to be received by the MAC. When RX_DV is deasserted, the RXD data should be ignored. For ENDEC operation, only RXD.0 is used for reception of frames.
16	RXD.2	
15	RXD.1	
14	RXD.0	
1	CRS	Carrier Sense, Input. The carrier sense signal is an active-high input and should be asserted by the external Ethernet PHY controller when either the transmit or receive medium is not idle. CRS should be deasserted by the PHY when the transmit and receive mediums are idle. The PHY should ensure that the CRS signal remains asserted throughout the duration of a collision condition. The transitions on the CRS signal need not be synchronous to TXClk or RXClk. CRS serves the same function for ENDEC operation.
2	COL	Collision Detect, Input. The collision detect signal is an active-high input and should be asserted by the external Ethernet PHY controller upon detection of a collision on the medium. The PHY should ensure that COL remains asserted while the collision condition persists. The transitions on the COL signal need not be synchronous to TXClk or RXClk. The COL signal is ignored by the MAC when operating in full-duplex mode. COL serves the same function for ENDEC operation.
18	MDC	MII Management Clock, Output. The MII management clock is generated by the MAC for use by the external Ethernet PHY controller as a timing referenced for transferring information on the MDIO pin. MDC is a periodic signal that has no maximum high or low times. The minimum high and low times are 160ns each. The minimum period for MDC is 400ns independent of the period of TXClk and RXClk.

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
C0M9C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	B6h
C0M10C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	B7h
IP	—	PS1	PT2	PS0	PT1	PX1	PT0	PX0	B8h
SADEN0									B9h
SADEN1									BAh
C0M11C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	BBh
C0M12C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	BCh
C0M13C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	BDh
C0M14C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	BEh
C0M15C	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP	BFh
SCON1	SM0/FE_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	C0h
SBUF1									C1h
PMR	CD1	CD0	SWB	CTM	4X/$\overline{2X}$	ALEOFF	—	—	C4h
STATUS	PIP	HIP	LIP	—	SPTA1	SPRA1	SPTA0	SPRA0	C5h
MCON	—	—	—	—	PDCE3	PDCE2	PDCE1	PDCE0	C6h
TA									C7h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/$\overline{T2}$	CP/$\overline{RL2}$	C8h
T2MOD	—	—	—	D13T1	D13T2	—	T2OE	DCEN	C9h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
COR	IRDACK	—	—	C0BPR7	C0BPR6	COD1	COD0	CLKOE	CEh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
MCNT0	$\overline{LSHIFT}$	CSE	SCE	MAS4	MAS3	MAS2	MAS1	MAS0	D1h
MCNT1	MST	MOF	SCB	CLM	—	—	—	—	D2h
MA									D3h
MB									D4h
MC									D5h
MCON1	IRAMD	PRAME	—	—	PDCE7	PDCE6	PDCE5	PDCE4	D6h
WDCON	SMOD_1	POR	EPFI	PFI	WDIF	WTRF	EWT	RWT	D8h
SADDR2									D9h
BPA1									DAh
BPA2									DBh
BPA3									DCh
ACC									E0h
OCAD									E1h
CSRD									E3h
CSRA									E4h
EBS	FPE	RBF	—	BS4	BS3	BS2	BS1	BS0	E5h
BCUD									E6h
BCUC	BUSY	EPMF	TIF	RIF	BC3	BC2	BC1	BC0	E7h
EIE	EPMIE	C0IE	EAIE	EWDI	EWPI	ES2	ET3	EX2-5	E8h
MXAX									EAh
DPX2									EBh
DPX3									EDh
OWMAD	—	—	—	—	—	A2	A1	A0	EEh
OWMDR									EFh
B									F0h
SADEN2									F1h
DPL2									F2h
DPH2									F3h

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDRESS
STATUS	0	0	0	1	0	0	0	0	C5h
MCON	1	1	1	1	0	0	0	0	C6h
TA	1	1	1	1	1	1	1	1	C7h
T2CON	0	0	0	0	0	0	0	0	C8h
T2MOD	1	1	0	0	0	1	0	0	C9h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
COR	0	1	1	0	0	0	0	0	CEh
PSW	0	0	0	0	0	0	0	0	D0h
MCNT0	0	0	0	0	0	0	0	0	D1h
MCNT1	0	0	0	0	1	1	1	1	D2h
MA	0	0	0	0	0	0	0	0	D3h
MB	0	0	0	0	0	0	0	0	D4h
MC	0	0	0	0	0	0	0	0	D5h
MCON1	0	0	1	1	0	0	0	0	D6h
WDCON	0	Special	0	Special	0	Special	0	0	D8h
SADDR2	0	0	0	0	0	0	0	0	D9h
BPA1	0	0	0	0	0	0	0	0	DAh
BPA2	0	0	0	0	0	0	0	0	DBh
BPA3	0	0	0	0	0	0	0	0	DCh
ACC	0	0	0	0	0	0	0	0	E0h
OCAD	0	0	0	0	0	0	0	0	E1h
CSRD	0	0	0	0	0	0	0	0	E3h
CSRA	0	0	0	0	0	0	0	0	E4h
EBS	0	1	1	0	0	0	0	0	E5h
BCUD	0	0	0	0	0	0	0	0	E6h
BCUC	0	0	0	0	0	0	0	0	E7h
EIE	0	0	0	0	0	0	0	0	E8h
MXAX	0	0	0	0	0	0	0	0	EAh
DPX2	0	0	0	0	0	0	0	0	EBh
DPX3	0	0	0	0	0	0	0	0	EDh
OWMAD	0	0	0	0	0	1	1	1	EEh
OWMDR	0	0	0	0	0	0	0	0	EFh
B	0	0	0	0	0	0	0	0	F0h
SADEN2	0	0	0	0	0	0	0	0	F1h
DPL2	0	0	0	0	0	0	0	0	F2h
DPH2	0	0	0	0	0	0	0	0	F3h
DPL3	0	0	0	0	0	0	0	0	F4h
DPH3	0	0	0	0	0	0	0	0	F5h
DPS1	0	0	1	1	1	1	1	1	F6h
STATUS1	1	1	1	1	1	1	0	0	F7h
EIP	0	0	0	0	0	0	0	0	F8h
P7	1	1	1	1	1	1	1	1	F9h
TL3	0	0	0	0	0	0	0	0	FBh
TH3	0	0	0	0	0	0	0	0	FCh
T3CM	0	0	0	0	0	0	0	0	FDh
SCON2	0	0	0	0	0	0	0	0	FEh
SBUF2	0	0	0	0	0	0	0	0	FFh

Note: Shaded bits are timed-access protected. “Special” bits are affected only by certain types of reset. Refer to the user’s guide for details.

TIMED-ACCESS PROTECTION

Selected SFR bits are critical to operation, making it desirable to protect them against an accidental write operation. The timed-access procedure prevents errant behavior from accidentally altering bits that would seriously affect microcontroller operation. The timed-access procedure requires that the write of a protected bit be immediately preceded by the following two instructions:

```
MOV   0C7h, #0AAh
MOV   0C7h, #55h
```

Writing an AAh followed by a 55h to the timed access register (location C7h), opens a three-cycle window that allows software to modify one of the protected bits. The protected bits are:

SFR	BIT(S)	NAME	FUNCTION
EXIF (91h)	EXIF.0	BGS	Bandgap Select
P4CNT (92h)	P4CNT.5–0	—	Port 4 Pin Configuration Control Bits
ACON (9Dh)	ACON.5	MROM	Merge ROM
—	ACON.4	BPME	Breakpoint Mode Enable
—	ACON.3	BROM	By-Pass ROM
—	ACON.2	SA	Stack Address Mode
—	ACON.1–0	AM1–AM0	Address Mode Select Bits
P5CNT (A2h)	P5CNT.2–0	—	Port 5 Pin Configuration Control Bits
C0C (A3h)	C0C.3	CRST	CAN 0 Reset
P6CNT (B2h)	P6CNT.5–0	—	Port 6 Pin Configuration Control Bits
—	MCON.5	CAN	CMA Data Memory Assignment
—	MCON.3–0	PDCE3–PDCE0	Program/Data-Chip Enables
COR (CEh)	COR.7	IRDACK	IRDA Clock-Output Enable
—	COR.4–3	C0BPR7–C0BPR6	CAN 0 Baud Rate Prescale Bits
—	COR.2–1	COD1–COD0	CAN Clock-Output Divide Bits
—	COR.0	CLKOE	CAN Clock-Output Enable
MCON1 (D6h)	MCON1.3–0	PDCE7–PDCE4	Program/Data Chip Enable
MCON2 (D7h)	MCON2.6–4	WPR2–WPR0	Write-Protect Range Bits
	MCON2.3–0	WPE3–WPE0	Write-Protect Enable Bits
WDCON (D8h)	WDCON.6	POR	Power-On Reset Flag
—	WDCON.3	WDIF	Watchdog Interrupt Flag
—	WDCON.1	EWT	Watchdog Reset Enable
—	WDCON.0	RWT	Reset Watchdog Timer
EBS (E5h)	EBS.7	FPE	Flush Filter Failed-Packet Enable
—	EBS.4–0	BS4-BS0	Buffer Size Configuration Bits

MEMORY ARCHITECTURE

The DS80C410 incorporates six internal memory areas:

- 256 Bytes of scratchpad (or direct) RAM
- 8kB of SRAM for Ethernet MAC transmit/receive buffer memory
- 64kB SRAM configurable as a combination of MOVX data memory and code memory
- 1kB SRAM configurable as extended stack memory or MOVX data memory
- 256 Bytes of RAM reserved for the CAN message centers (not available on the DS80C411)
- 64kB embedded ROM firmware

Up to 16MB of external code memory can be addressed through a multiplexed or demultiplexed 22-bit address bus/8-bit data bus through eight available chip enables. Up to 4MB of external data memory can be accessed over the same address/data buses through peripheral-enable signals. The DS80C410 also permits a 16MB merged program/data memory map.

Table 6. External Memory Addressing Pin Assignments

	SIGNAL	MULTIPLEXED ($\overline{MUX}$ = 0)	DEMULTIPLEXED ($\overline{MUX}$ = 1)
ADDRESS	A21	P6.5	P6.5
	A20	P6.4	P6.4
	A19	P4.7	P4.7
	A18	P4.6	P4.6
	A17	P4.5	P4.5
	A16	P4.4	P4.4
	A15–A8	P2.7–P2.0	P2.7–P2.0
	A7–A0	P0.7–P0.0	P7.7–P7.0
DATA	D7–D0	P0.7–P0.0	P0.7–P0.0
CHIP ENABLES	$\overline{CE7}$	P6.3	P6.3
	$\overline{CE6}$	P6.2	P6.2
	$\overline{CE5}$	P6.1	P6.1
	$\overline{CE4}$	P6.0	P6.0
	$\overline{CE3}$	P4.3	P4.3
	$\overline{CE2}$	P4.2	P4.2
	$\overline{CE1}$	P4.1	P4.1
	$\overline{CE0}$	P4.0	P4.0
PERIPHERAL CHIP ENABLES	$\overline{PCE3}$	P5.7	P5.7
	$\overline{PCE2}$	P5.6	P5.6
	$\overline{PCE1}$	P5.5	P5.5
	$\overline{PCE0}$	P5.4	P5.4

Combined Program/Data Memory Access

The DS80C410 can be configured to allow data memory access (MOVX) to the program memory area. This feature might be useful, for example, when modifying lookup tables or supporting in-application programming of code space. Setting any of the $\overline{PDCE7\text{-}4}$ (MCON1.3-0) or $\overline{PDCE3\text{-}0}$ (MCON.3-0) bits enables combined program/data memory access and causes the corresponding chip-enable ($\overline{CE}$) signal to function for both MOVC and MOVX operations. When combined program/data memory access is enabled, the peripheral chip-enable ($\overline{PCE}$) signals previously assigned to that data memory space are disabled. Write access to combined program and data memory blocks is controlled by the $\overline{WR}$ signal, and read access is controlled by the $\overline{PSEN}$ signal. This feature is especially useful if the design achieves in-system reprogrammability through external flash memory, in which a single device is accessed through both MOVC instructions (program fetch) and MOVX write operations (updates to code memory). Figure 1 demonstrates how setting $\overline{PDCE}$ bits can alter external memory data access.

When combined program/data memory access is enabled, there is the potential to inadvertently modify code that a user meant to leave fixed. For this reason, the DS80C410 provides the ability to write protect the first 0–16kB of memory accessible through each of the chip enables $\overline{CE3}$, $\overline{CE2}$, $\overline{CE1}$, and $\overline{CE0}$. The write-protection feature for each chip enable is invoked by setting the appropriate WPE3–0 (MCON2.3-0) bit. The protected range is defined by the WPR2–0 (MCON2.6–4) bit settings as shown in Table 7. Any MOVX instructions attempting to write to a protected area are disallowed and set the write-protected interrupt flag (WPIF–MCON2.7), causing a write-protect interrupt if enabled.

Table 7. Write-Protection Range

MCON2.6–4	RANGE PROTECTED (kB)
000	0 to 2
001	0 to 4
010	0 to 6
011	0 to 8
100	0 to 10
101	0 to 12
110	0 to 14
111	0 to 16

Each CSR register is documented as follows:

CSR Register: MAC Control
Register Address: 00h

Bit Names:

31	RA	BLE	—	HBD	PS	—	—	—	24
23	DRO	OM[1:0]		F	PM	PR	IF	PB	16
15	HO	—	HP	LCC	DBF	DRTY	—	ASTP	8
7	BLOMT[1:0]		DC	—	TE	RE	—	—	0

Reset State:

31	0	0	0	0	0	0	0	0	24
23	0	0	0	0	0	1	0	0	16
15	0	0	0	0	0	0	0	0	8
7	0	0	0	0	0	0	0	0	0

RA, Receive All . This bit overrides the flush-filter failed-packet function if that function has been enabled (EBS.7 = 1).
0 = default frame handling (default)
1 = all error-free frames are received with packet filter bit set (= 1) in the receive status word

BLE, Big/Little Endian Mode
0 = data buffers are operated in little Endian mode (default)
1 = data buffers are operated in big Endian mode

HBD, Heart-Beat Disable . This bit is only useful in ENDEC mode and has no affect on MII mode operation.
0 = heart-beat signal quality-generator function enabled (default)
1 = heart-beat signal quality-generator function is disabled

PS, Port Select
0 = MII mode (default)
1 = ENDEC mode

DRO, Disable Receive Own. This bit should always be cleared to a logic 0 for full-duplex operation and any loopback operating modes other than “normal mode.”
0 = MAC receives all packets given by the PHY (default)
1 = MAC disables reception of frames during frame transmission (TX_EN = 1)

OM[1:0], Loopback Operating Mode
00 = normal mode, no loopback (default)
01 = internal loopback through MII
10 = external loopback through PHY
11 = reserved

F, Full-Duplex Mode
0 = half-duplex mode (default)
1 = full-duplex mode

PM, Pass All Multicast
0 = multicast frames filtered according to current multicast filter mode (default)
1 = pass all multicast frames; filter-fail bit is reset (= 0) for all multicast frames received

PR, Promiscuous Mode
0 = promiscuous mode disabled
1 = promiscuous mode enabled (default)

IF, Inverse Filtering
0 = inverse filtering disabled (default)
1 = inverse filtering by the address check block enabled

PB, Pass Bad Frames
0 = packet filter bit in the receive status word is set (= 1) only when error-free frames received (default)
1 = packet filter bit in the receive status word is set (= 1) for frames that pass the destination address filter even when they contain errors. Promiscuous mode should always be used when this bit is set.

HO, Hash-Only Filtering Mode
This bit should only be set when HP = 1.
0 = filter unicast frames according to filter mode configuration (default)
1 = hash filtering of unicast and multicast frames by the address check block

HP, Hash/Perfect Filtering Mode
0 = perfect filtering by the address check block for unicast and multicast frames (default)
1 = hash filtering by the address check block for multicast frames and perfect filtering of unicast frames

LCC, Late Collision Control
0 = transmission is aborted if a late collision is encountered (default)
1 = allows frame retransmission attempts even when a late collision is encountered

DBF, Disable Broadcast F rames
0 = packet filter bit in the receive status word is set (= 1) for each broadcast frame received (default)
1 = packet filter bit in the receive status word is reset (= 0) for each broadcast frame received

DRTY, Disable Retry
0 = MAC attempts to transmit a frame 16 times before signaling a retry error (default)
1 = MAC attempts to transmit a frame only once before signaling a retry error

ASTP, Automatic Pad Stripping
0 = receive frames are transferred to the BCU without modification (default)
1 = zero padding and CRC are stripped for receive frames, which specify a data length less than 46 Bytes

BOLMT[1:0], Back-Off Limit. The back -off protocol requires that the MAC wait some number of time slots (512bits / time slot) before rescheduling a transmission attempt. A 10-bit free-running counter is used to generate this back-off delay. The BOLMT[1:0] bits select the number of bits to be used from the 10-bit counter.
00 = 10 bits (0 to 1024 time slots, default)
01 = 8 bits (0 to 256 time slots)
10 = 4 bits (0 to 16 time slots)
11 = 1 bit (none or 1 time slot)

DC, Deferral Check
0 = MAC can defer indefinitely while waiting to transmit (default)
1 = MAC aborts a transmission attempt if it has deferred for more than 24,288 consecutive bit times

TE, Transmitt er Enable
0 = transmitter disabled (default)
1 = transmitter enabled

RE, Receiver Enable
0 = receiver disabled (default)
1 = receiver enabled

CSR Register: MII Address
Register Address: 14h

Bit Names:

31	—	—	—	—	—	—	—	—	24
23	—	—	—	—	—	—	—	—	16
15	PHYA [4:0]					PHYR [4:2]			8
7	PHYR [1:0]		—	—	—	—	W/$\overline{R}$	BUSY	0

Reset State:

31	0	0	0	0	0	0	0	0	24
23	0	0	0	0	0	0	0	0	16
15	0	0	0	0	0	0	0	0	8
7	0	0	0	0	0	0	0	0	0

PHYA[4:0], PHY Address [4:0]. This 5-bit address specifies the PHY address for 2-wire MII serial-management bus communication.

PHYR[4:0], PHY Register Select [4:0]. This 5-bit field specifies the PHY register to be accessed in 2-wire MII serial-management bus communication.

W/$\overline{R}$, Write/Read. This bit is used to indicate whether a write or read operation is to be requested of the addressed PHY/PHY register.
0 = read
1 = write

BUSY, Busy. This status bit indicates when PHY communication is currently taking place on the MII serial-management bus. The application must wait until BUSY = 0 before modifying the MII address and MII data registers prior to each read/write operation.
0 = MII serial-management bus idle
1 = MII serial-management bus busy (write/read in progress)

CSR Register: MII Data
Register Address: 18h

Bit Names:

31	—	—	—	—	—	—	—	—	24
23	—	—	—	—	—	—	—	—	16
15	PHYD [15:8]								8
7	PHYD [7:0]								0

Reset State:

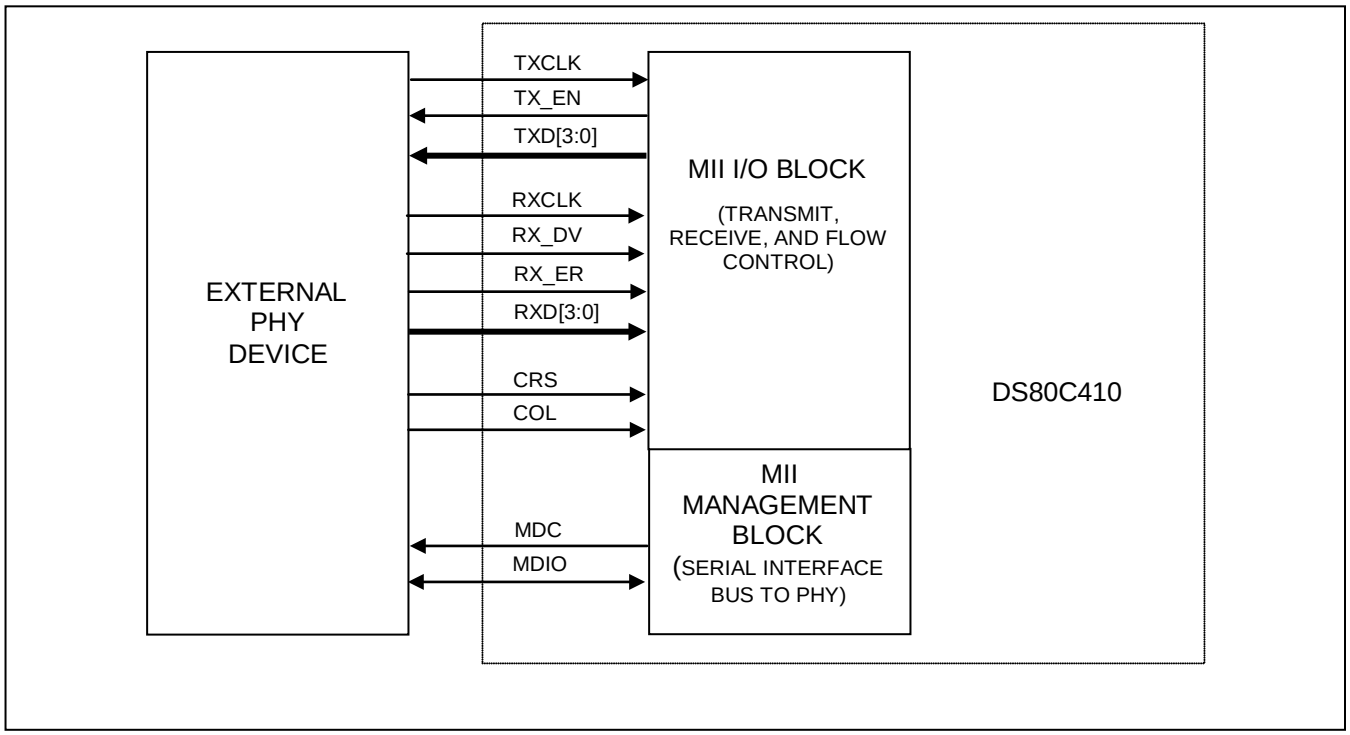
31	0	0	0	0	0	0	0	0	24
23	0	0	0	0	0	0	0	0	16
15	0	0	0	0	0	0	0	0	8
7	0	0	0	0	0	0	0	0	0

PHYD[15:0], PHY Data [15:0]. These 16 bits contain the data read from the PHY register following a read operation, or the data to be written to the PHY register prior to a write operation.

Media Independent Interface (MII)

The DS80C410 contains an IEEE 802.3 MII-compliant PHY interface. This interface contains two basic blocks. The MII I/O block provides independent transmit and receive data-path I/O and PHY network-status signal inputs. The MII management block implements a 2-wire serial communication bus to facilitate PHY register access. The block diagram in Figure 5 shows the signals associated with the DS80C410 MII.

Figure 5. MII Block Diagram



MII Management Block

The MII management block allows the host to write control data to and read status from any of 32 registers in any of 32 PHY controllers. The MII management block communicates with external PHY(s) over a 2-wire serial interface composed of the MDC serial-clock output pin and the MDIO pin that serves as the I/O line for all address and data transactions. Data (MDIO) is valid on the rising edge of clock (MDC). The MII address (14h) and MII data (18h) CSR registers, outlined previously in the CSR Register section, are used by the CPU to monitor and control the 2-wire MII serial bus. A write to the CSR register MII address triggers the read or write operation. Figure 6 shows the MII management frame format.

Figure 6. MII Management Frame Format

	PREAMBLE (32 bits)	START (2 bits)	OP CODE (2 bits)	PHY ADDRESS (5 bits)	PHY REGISTER (5 bits)	TURN AROUND (2 bits)	DATA (16 bits)	IDLE (1 bit)
READ	111…111	01	10	PHYA [4:0]	PHYR[4:0]	ZZ*	ZZ….ZZ*	Z
WRITE	111…111	01	01	PHYA [4:0]	PHYR[4:0]	10	PHYD[15:0]	Z

*During a read operation, the external PHY drives the MDIO line low for the second bit of the turnaround field to indicate proper synchronization, and then drives the 16-bits of read data requested.

Transmit/Receive Status Words

For each attempt made by the MAC to receive or transmit packet data, the BCU writes a 32-bit transmit or receive status word back to the first word of the starting page for the packet. This word provides status information needed by the CPU to determine when and what action should be taken.

Transmit Status Word

Bit Names:

31	RETRY	—	—	—	—	—	—	—	24
23	—	—	—	—	—	—	—	—	16
15	—	HBF	COL_CNT [3:0]				OLTCOL	DFR	8
7	NODAT	XCOL	LTCOL	XDFR	LSCRS	NOCRS	JABTO	ABORT	0

RETRY, Packet Retry. This bit indicates that the current transmit packet has to be retried because of a collision on the bus. The application has to restart the transmission of the frame when this bit is set to 1. When this bit is reset, it indicates that the transmission of the current frame is completed. The success or failure to transmit a frame is indicated by the framed aborted (ABORT) bit.

HBF, Heart-Beat Fail. This bit is only meaningful for ENDEC mode. This bit is not valid if the NODAT or XFDR bit is set.
0 = heart-beat collision check successful
1 = heart-beat collision check failed

COL_CNT [3:0], Collision Count. These four bits indicate the number of collisions that occurred before the frame was transmitted. Collision count is valid only in half-duplex mode and it is not valid when the excessive collisions (XCOL) bit is set.

OLTCOL, Late Collision Observed. This bit is only valid in half -duplex mode and is always set if the late collision abort (LTCOL) bit is set in the status word.
0 = no late collisions observed
1 = late collision (collision after the first time slot) observed.

DFR, Deferred. This bit is only valid in half-duplex mode.
0 = no deferral required for the frame transmission attempt
1 = MAC had to defer while waiting to transmit because the carrier was not idle

NODAT, Underrun
0 = transmit frame was not aborted due to data underrun
1 = transmit frame aborted because the MAC did not have sufficient data to complete the current frame transmission

XCOL, Excessive Collisions. This bit is only valid in half -duplex mode.
0 = transmit frame was not aborted due to excessive collisions
1 = transmit frame aborted because of excessive collisions (16 transmit attempts unless DRTY = 1)

LTCOL, Late Collision. This bit is only valid in half-duplex mode.
0 = transmit frame was not aborted due to a late collision
1 = transmit frame aborted due to collision occurring after the collision window of 64 Bytes. This bit is not valid if the NODAT bit is set.

XDFR, Excessive Deferral. This bit is only valid in half -duplex mode when the MAC control register bit DFR is set.
0 = transmit frame was not aborted due to excessive deferral
1 = transmit frame aborted due to deferral of over 24,288 bit times

LSCRS, Loss of Carrier. This bit is only valid in half-duplex mode.
0 = transmit frame was not aborted due to loss of carrier
1 = transmit frame aborted due to loss of carrier (CRS = 0 during the frame transmission)

VLAN2, Two_Level VLAN Frame
0 = receive frame did not contain a VLAN tag that matched the VLAN2 register
1 = receive frame 13th and 14th bytes matched the two-level VLAN tag register (VLAN2)

VLAN1, One_Level VLAN Frame
0 = receive frame did not contain a VLAN tag that matched the VLAN1 register
1 = receive frame 13th and 14th bytes matched the one-level VLAN tag register (VLAN1)

CRC, CRC Error. This bit is also set to 1 if the RX_ER pin is asserted by the PHY during a reception, even if the CRC-32 for the frame is correct.
0 = CRC-32 error was not detected for the receive frame
1 = CRC-32 error was detected for the receive frame

DRIB, Dribbling Bit. This bit is not valid if the COL or RUNT bits are set to 1. If DRIB = 1 and CRC = 0, then the packet is valid.
0 = receive frame did not contain any dribbling bits
1 = receive frame contained dribbling bits (a noninteger multiple of 8 bits)

MII_ER, MII Error
0 = PHY did not assert the RX_ER signal during reception of the frame
1 = PHY asserted the RX_ER signal (indicating an error was detected) during the receive frame

TYPE, Frame Type. This bit is not valid for runt frames less than 14 Bytes.
0 = length specified in the length/type field (i.e., value equal or less than 1500)
1 = type specified in the length/type field (i.e., value greater than 1500)

COL, Collision Seen
0 = receive frame did not incur any collisions
1 = receive frame is damaged by a late collision (one that occurred after the first 64 bytes)

LONG, Frame Too Long. This bit only serves as a status indicator and does not cause frame truncation.
0 = receive frame did not exceed the maximum frame length check
1 = receive frame exceeded the maximum frame length (1518 Bytes, unless VLAN tagged)

RUNT, Runt Frame
0 = receive frame is not a runt frame (<64 Bytes)
1 = receive frame does not meet the minimum required frame size (64 Bytes = 1 time slot) due to a collision or premature frame termination

WDOG, Watchdog Timeout. The FLEN[13:0] field is not valid when this bit is set.
0 = MAC watchdog timer did not timeout during the receive frame
1 = MAC watchdog timer timed out during the receive frame. The watchdog timer is programmed to twice the maximum frame length (3036 bit times).

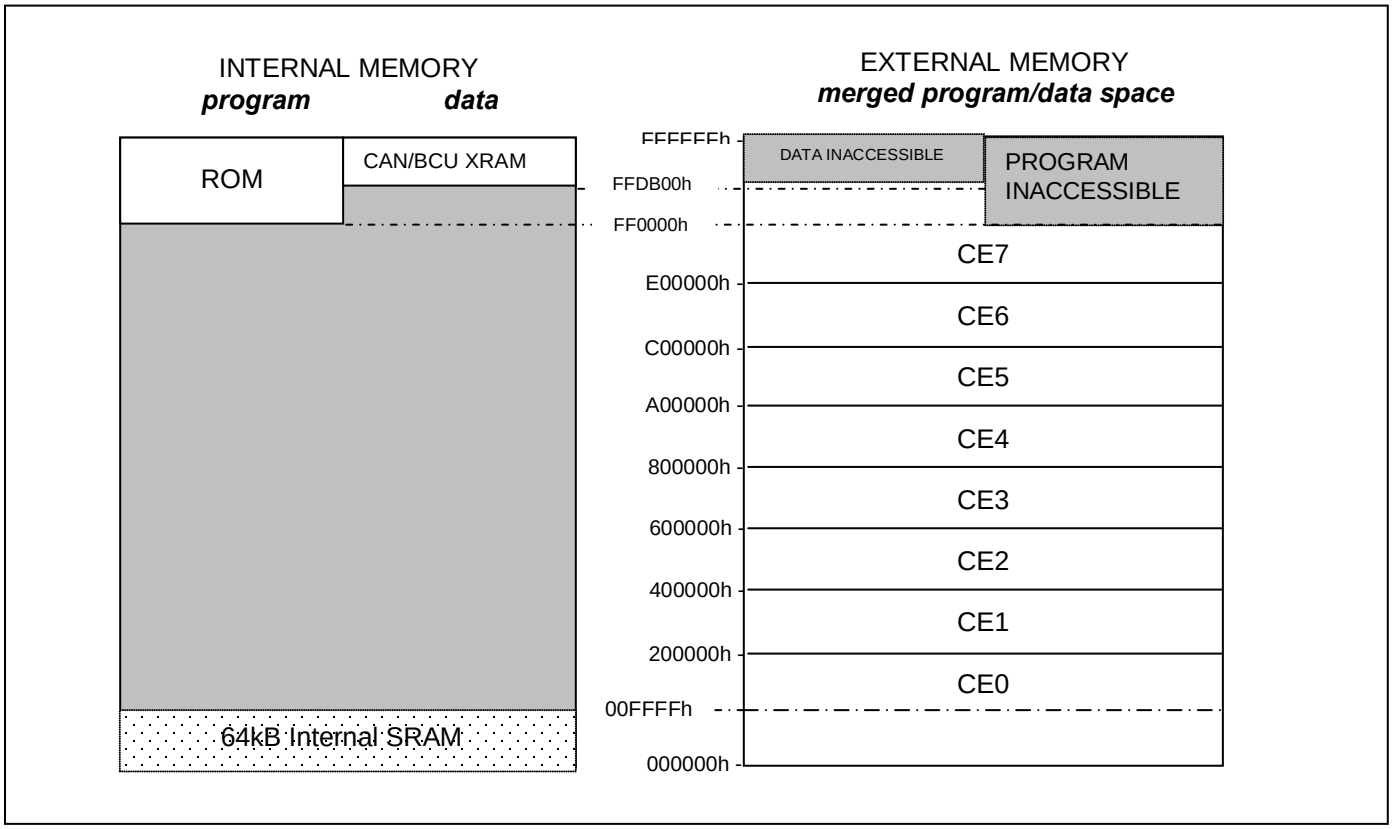
FLEN [13:0], Frame Length [13:0]. This field indicates the receive frame length in bytes, including zero padding pad (if applicable) and the CRC-32 field, unless automatic pad stripping has been enabled (ASTP = 1). When ASTP = 1, the frame length includes only the data field.

DS80C410 ROM Initialization Code

The DS80C410 firmware automatically executes Initialization Code (ROM_Init) to generate the memory map as shown in Figure 14 and configure the hardware as follows:

Enables 24-bit contiguous address mode	(ACON.1:0 = 11b)
Logically relocates ROM to addresses FF0000h–FF7FFFh	(ACON.5 =1)
Enables CE0–3, 2MB/chip enable	(P4CNT = 2Fh)
Enables PCE0–3	(P5CNT = 07h)
Enables CE4–7, 1M/peripheral chip enable	(P6CNT = 27h)
Merged program/data CE0–3, relocate internal XRAM	(MCON = AFh)
Enables extended 1kB stack option	(ACON.2 = 1)
Configure to maximum MOVX stretch value	(CKCON.2:0 = 111b)
Configure UARTs for Mode 1 serial operation	

Figure 14. Memory Map Following Execution of ROM_I nit on DS80C410/DS80C411



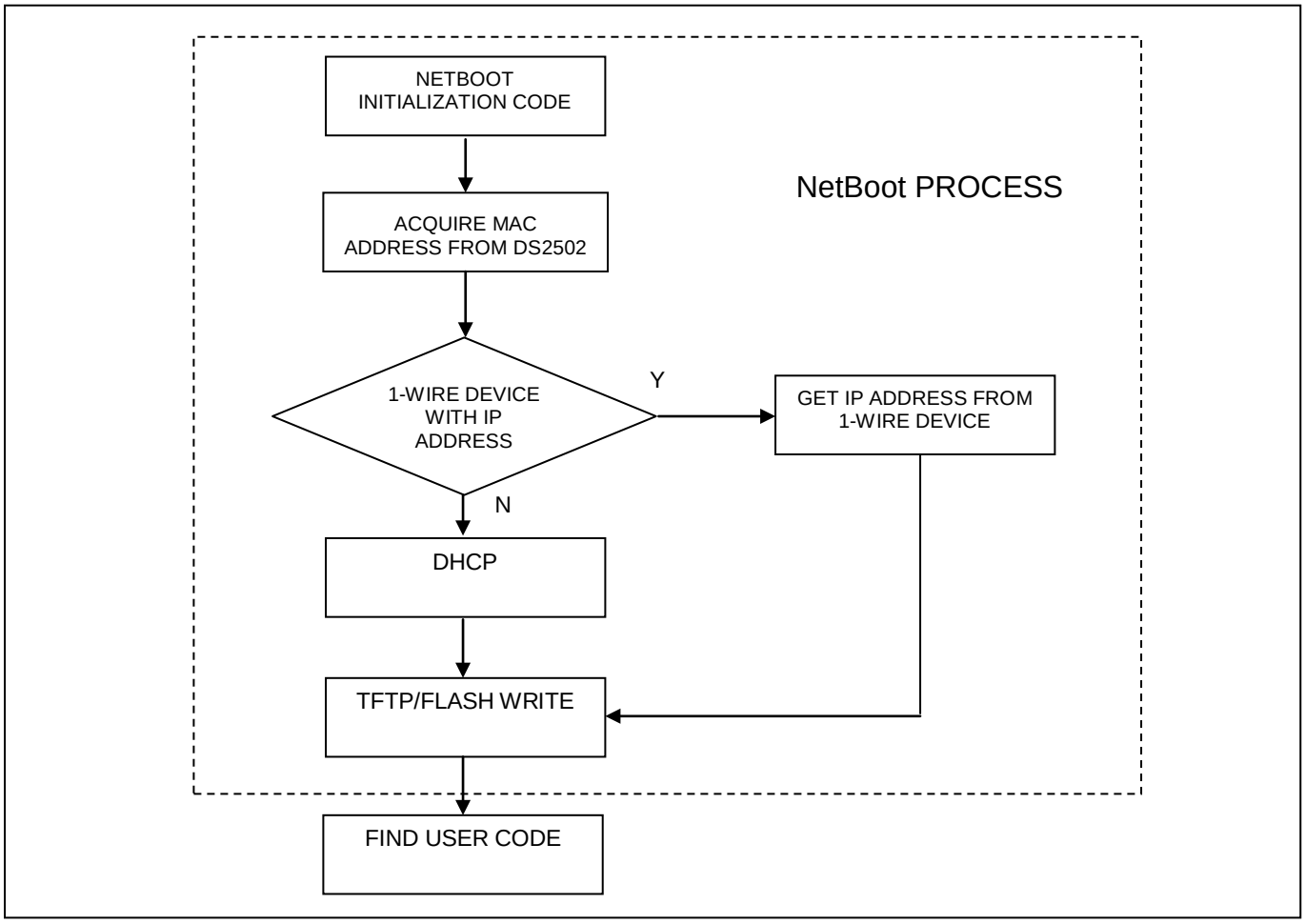
NetBoot

The NetBoot process affords the user flexibility to download or update code remotely over the network. This capability is quite powerful. Not only does it make firmware revisions trivial, but it also makes remote diagnostics very practical. Also, since NetBoot can automatically reload the latest version of the user application code, the system designer now has the option to select volatile SRAM for code storage.

For the NetBoot function to work, the DS80C410 ROM firmware must initialize certain hardware components and create the environment needed to support the process. The NetBoot initialization code implements a primitive memory manager, kicks off the task scheduler, and initializes the 1-Wire hardware, Ethernet driver, TCP/IP stack, and socket layer.

Once the NetBoot initialization code has completed, the true network boot process can begin. The DS80C410 Ethernet MAC first must be assigned a physical address. Within the NetBoot process, the physical MAC address can only be acquired through an external DS2502-(E48) 1-Wire chip. Hence, this 1-Wire chip, containing the MAC address, is required for successful NetBoot operation. Figure 15 shows the NetBoot code flow chart.

Figure 15. NetBoot Code Flow Chart



Next, the DS80C410 ROM searches the 1-Wire bus for an external device (separate from the device containing the MAC address) that contains an IP address and TFTP server IP address. In order to correctly acquire the IP and TFTP server addresses from an external 1-Wire device, the data read from the device must conform to a specific format. This format is shown in Figure 16.

Table 16. ROM Export Tabl e

INDEX	FUNCTION	DESCRIPTION/GROUP
0	Num_Fn,0,0	Number of functions following in the table
1	crc16	Utility functions
2	mem_clear	
3	mem_copy	
4	mem_compare	
5	add_dptr0	
6	add_dptr1	
7	sub_dptr0	
8	sub_dptr1	
9	getpseudorandom	
10	rom_kernelmalloc	Memory manager
11	rom_kernelfree	
12	rom_malloc	
13	rom_malloc_dirty	
14	rom_free	
15	rom_deref	
16	rom_getfreeram	
17	socket	Socket functions
18	closesocket	
19	sendto	
20	recvfrom	
21	connect	
22	bind	
23	listen	
24	accept	
25	recv	
26	send	
27	getsockopt	
28	setsockopt	
29	getsockname	
30	getpeername	
31	cleanup	
32	avail	
33	join	
34	leave	
35	ping	
36	getnetworkparams	
37	setnetworkparams	
38	getipv6params	
39	getethernetstatus	
40	gettftpserver	
41	settftpserver	
42	eth_processinterrupt	Ethernet interrupt handler
43	arp_generaterequest	Generates ARP request
44	MAC_ID	Pointer to MAC ID
45	dhcp_init	DHCP functions
46	dhcp_setup	
47	dhcp_startup	
48	dhcp_run	
49	dhcp_status	
50	dhcp_stop	
51	rom_dhcp_notify	
52	tftp_init	TFTP functions
53	tftp_first	
54	tftp_next	
55	TFTP_MSG	
56	task_genesis	Task scheduler functions
57	task_getcurrent	
58	task_getpriority	
59	task_setpriority	
60	task_fork	

Status

The STATUS (C5h) register and STATUS1 (F7h) register provide information about interrupt and serial port activity to assist in determining if it is possible to enter PMM. The microcontroller supports three levels of interrupt priority: power-fail, high, and low. The PIP (power-fail priority interrupt status; STATUS.7), HIP (high priority interrupt status; STATUS.6), and LIP (low priority interrupt status; STATUS.5) status bits, when set to a logic 1, indicate the corresponding level is in service.

Software should not rely on a lower-priority level interrupt source to remove PMM (switchback) when a higher level is in service. Check the current priority service level before entering PMM. If the current service level locks out a desired switchback source, then it would be advisable to wait until this condition clears before entering PMM. Alternately, software can prevent an undesired exit from PMM by intentionally entering a low priority interrupt-service level before entering PMM. This prevents other low priority interrupts from causing a switchback.

Entering PMM during an ongoing serial port transmission or reception can corrupt the serial port activity. To prevent this, a hardware lockout feature ignores changes to the clock divisor bits while the serial ports are active. Serial port transmit and receive activity can be monitored through the serial port activity bits located in the STATUS and STATUS1 registers.

Oscillator -Fail Detect

The microcontroller contains a safety mechanism called an on-chip oscillator-fail detect circuit. When enabled, this circuit causes the microcontroller to be held in reset if the oscillator frequency falls below ~100kHz. When activated, this circuit complements the watchdog timer. Normally, the watchdog timer is initialized so that it times out and causes a reset in the event that the microcontroller loses control. In the event of a crystal or external oscillator failure, however, the watchdog timer does not function, and there is the potential to fail in an uncontrolled state. Using the oscillator-fail detect circuit forces the microcontroller to a known state (i.e., reset) even if the oscillator stops.

The oscillator-fail detect circuitry is enabled when software sets the enable bit OFDE (PCON.4) to a 1. Please note that software must use a timed-access procedure (described earlier) to write this bit. The OFDF (PCON.5) bit also sets to a 1 when the circuitry detects an oscillator failure, and the microcontroller is forced into a reset state. This bit can only be cleared to a 0 by a power-fail reset or by software. The oscillator-fail detect circuitry is not triggered when the oscillator is stopped upon entering stop mode.

Power -Fail Reset

The microcontroller incorporates an internal precision bandgap voltage reference and comparator circuit that provide a power-on and power-fail reset function. This circuit monitors the incoming power supply voltages (V_{CC1} and V_{CC3}) and holds the microcontroller in reset if either supply is below a minimum voltage level. When power exceeds the reset threshold, a full power-on reset is performed. In this way, this internal voltage monitoring circuitry handles both power-up and power-down conditions without the need for additional external components.

Once V_{CC1} and V_{CC3} have risen above minimum voltages, V_{RST1} and V_{RST3} respectively, the device automatically restarts the oscillator for the external crystal and counts 65,536 clock cycles before program execution begins at location 0000h. This helps the system maintain reliable operation by only permitting operation when the supply voltage is in a known good state. Software can determine that a power-on reset has occurred by checking the power-on reset flag (POR;WDCON.6). Software should clear the POR bit after reading it.

Power -Fail Interrupt

The bandgap voltage reference that sets precise reset thresholds also generates an optional early warning power-fail interrupt (PFI). When enabled by software, the microcontroller vectors to code address 0033h if either V_{CC1} or V_{CC3} drop below V_{PFW1} or V_{PFW3}, respectively. PFI has the highest priority. The PFI enable is in the watchdog control SFR (EPFI;WDCON.5). Setting this bit to logic 1 enables the PFI. Application software can also read the PFI flag at WDCON.4. A PFI condition sets this bit to a 1. The flag is independent of the interrupt enable and must be cleared by software.