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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	66MHz
Non-Volatile Memory	External
On-Chip RAM	40kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2186mbstz-266

- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board
- EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
- EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0++
- EE-153: ADSP-2191 Programmable PLL
- EE-154: ADSP-2191 Host Port Interface
- EE-156: Support for the H.100 protocol on the ADSP-2191
- EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
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- ADSP-2186M: 16-Bit, 75 MIPS, 2.5V, 2 Serial Ports, Host Port, 40 KB RAM Data Sheet

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- ADSP-218x DSP family and ADSP-2192 EZ-KIT Lite® Installation Procedure -Non-USB

Integrated Circuit Anomalies

- ADSP-2186M Anomaly List for Revision 2.0

Processor Manuals

- ADSP 21xx Processors: Manuals
- ADSP-218x DSP Hardware Reference
- ADSP-218x DSP Instruction Set Reference
- Using the ADSP-2100 Family Volume 1
- Using the ADSP-2100 Family Volume 2

Software Manuals

- VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
- VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
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- VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
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- PCN-PDN Information
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GENERAL DESCRIPTION

The ADSP-2186M is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications.

The ADSP-2186M combines the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2186M integrates 40K bytes of on-chip memory configured as 8K words (24-bit) of program RAM, and 8K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-2186M is available in a 100-lead LQFP package and 144 Ball Mini-BGA.

In addition, the ADSP-2186M supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (× squared), biased rounding, result-free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility.

Fabricated in a high-speed, low-power, CMOS process, the ADSP-2186M operates with a 13.3 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2186M's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-2186M can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2186M. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

The EZ-KIT Lite is a hardware/software kit offering a complete evaluation environment for the ADSP-218x family: an ADSP-2189M-based evaluation board with PC monitor software plus assembler, linker, simulator, and PROM splitter software. The ADSP-2189M EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE Connector for Emulator Control
- DSP Demo Programs
- Evaluation Suite of VisualDSP

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-2186M system. The ADSP-2186M integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2186M device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See *Designing An EZ-ICE-Compatible Target System* in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections) as well as the Designing an EZ-ICE-Compatible System section of this data sheet for the exact specifications of the EZ-ICE target board connector.

Additional Information

This data sheet provides a general overview of ADSP-2186M functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*. For more information about the development tools, refer to the ADSP-2100 Family Development Tools data sheet.

external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2186M to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2186M can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2186M provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2186M incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2186M SPORTs. For additional information on Serial Ports, refer to the *ADSP-2100 Family User's Manual.*

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time- division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

PIN DESCRIPTIONS

The ADSP-2186M is available in a 100-lead LQFP package and a 144-Ball Mini-BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{RESET}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

Common-Mode Pins

Pin Name	# of Pins	I/O	Function
$\overline{RESET}$	1	I	Processor Reset Input
$\overline{BR}$	1	I	Bus Request Input
$\overline{BG}$	1	O	Bus Grant Output
$\overline{BGH}$	1	O	Bus Grant Hung Output
$\overline{DMS}$	1	O	Data Memory Select Output
$\overline{PMS}$	1	O	Program Memory Select Output
$\overline{IOMS}$	1	O	Memory Select Output
$\overline{BMS}$	1	O	Byte Memory Select Output
$\overline{CMS}$	1	O	Combined Memory Select Output
$\overline{RD}$	1	O	Memory Read Enable Output
$\overline{WR}$	1	O	Memory Write Enable Output
$\overline{IRQ2}$	1	I	Edge- or Level-Sensitive Interrupt Request[1]
PF7		I/O	Programmable I/O Pin
$\overline{IRQL1}$	1	I	Level-Sensitive Interrupt Requests[1]
PF6		I/O	Programmable I/O Pin
$\overline{IRQL0}$	1	I	Level-Sensitive Interrupt Requests[1]
PF5		I/O	Programmable I/O Pin
$\overline{IRQE}$	1	I	Edge-Sensitive Interrupt Requests[1]
PF4		I/O	Programmable I/O Pin
Mode D	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF3		I/O	Programmable I/O Pin During Normal Operation
Mode C	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A	1	I	Mode Select Input—Checked Only During $\overline{RESET}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port I/O Pins
$\overline{IRQ1:0}$, FI, FO			Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{PWD}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (2.5 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (2.5 V or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (2.5 V) Power (Mini-BGA)
V_{DDEXT}	7	I	External V_{DD} (2.5 V or 3.3 V) Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

NOTES

[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.

[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2186M processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

The following tables list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinout tables.

Full Memory Mode Pins (Mode C = 0)

Pin Name	# of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Host Mode Pins (Mode C = 1)

Pin Name	# of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23:8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

NOTE
[1]In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Slow Idle

The IDLE instruction is enhanced on the ADSP-2186M to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

IDLE (n);

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2186M will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-2186M, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2186M also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

The ADSP-2186M can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual,* for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The ADSP-2186M uses an input clock with a frequency equal to half the instruction rate; a 37.50 MHz input clock yields a 13 ns processor cycle (which is equivalent to 75 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2186M includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

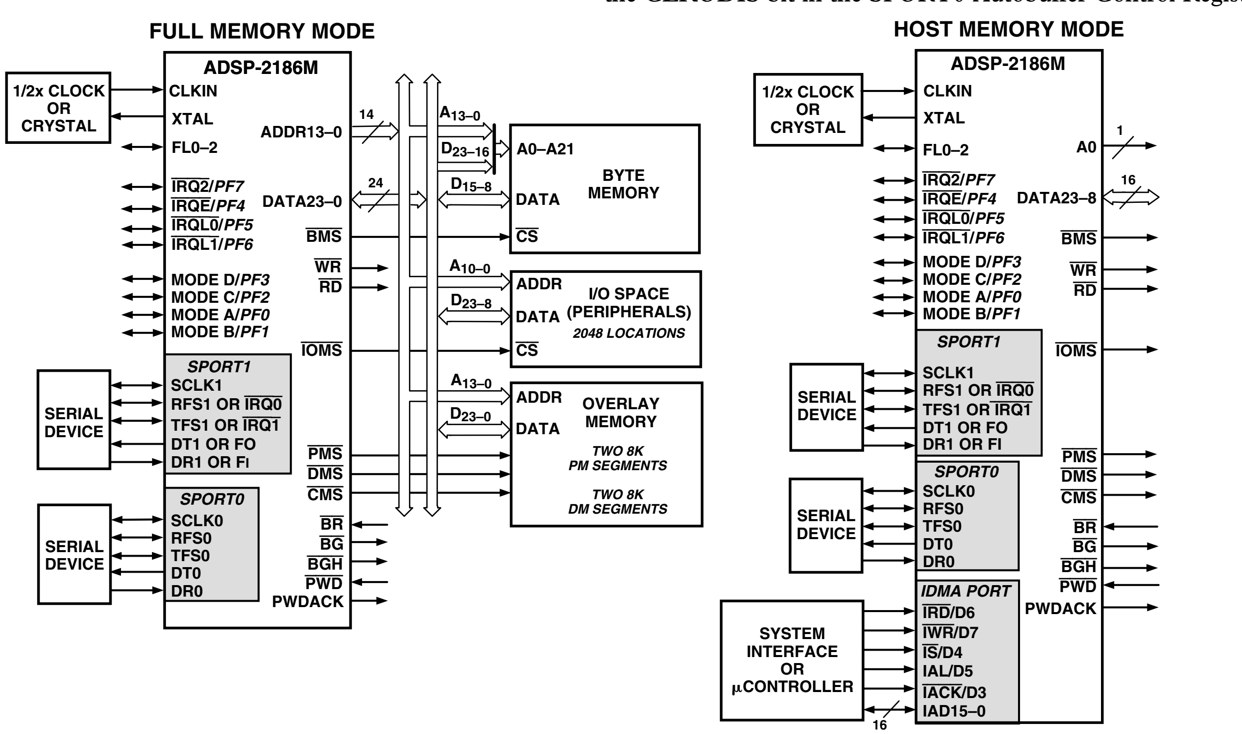


Figure 2. Basic System Interface

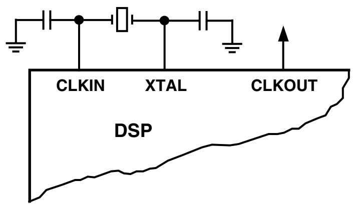


Figure 3. External Crystal Connections

$\overline{RESET}$

The $\overline{RESET}$ signal initiates a master reset of the ADSP-2186M. The $\overline{RESET}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{RESET}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{RESET}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{RESET}$ signal should be held low. On any subsequent resets, the $\overline{RESET}$ signal must meet the minimum pulsewidth specification, t_{RSP}.

The $\overline{RESET}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{RESET}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{RESET}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Power Supplies

The ADSP-2186M has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply can be connected to either a 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.5 V and 3.3 V components.

MODES OF OPERATION

Setting Memory Mode

Memory Mode selection for the ADSP-2186M is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Table II. Modes of Operation

MODE D	MODE C	MODE B	MODE A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{IACK}$ has active pull-down. (REQUIRES ADDITIONAL HARDWARE).
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. $\overline{IACK}$ has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{IACK}$ requires external pull down. (REQUIRES ADDITIONAL HARDWARE)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. $\overline{IACK}$ requires external pull-down.[1]

NOTE
[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2186M has 8K words on Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

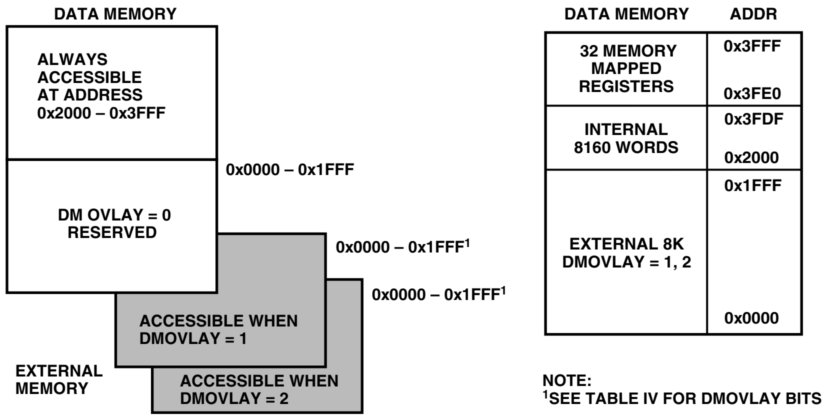


Figure 5. Data Memory Map

Table IV. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0	Reserved	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Memory Mapped Registers (New to the ADSP-2186M)

The ADSP-2186M has three memory mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-2186M's wait state and $\overline{BMS}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

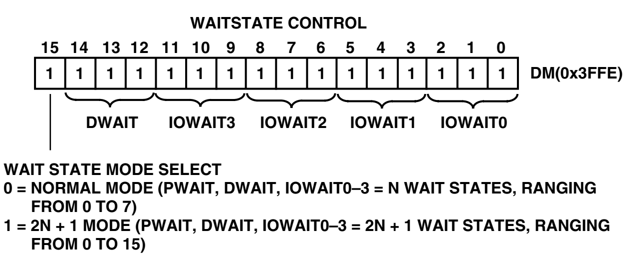


Figure 6. Wait State Control Register

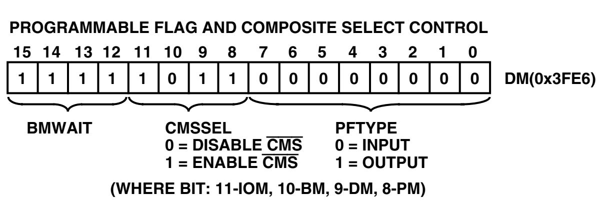


Figure 7. Programmable Flag and Composite Control Register

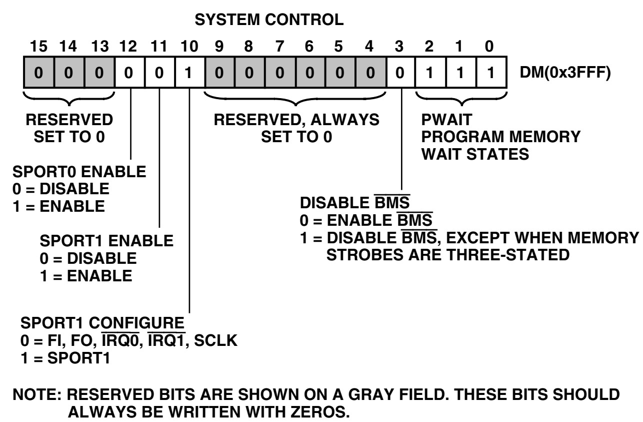


Figure 8. System Control Register

I/O Space (Full Memory Mode)

The ADSP-2186M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

Table V. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)

The ADSP-2186M has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)

The ADSP-2186M's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2186M supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

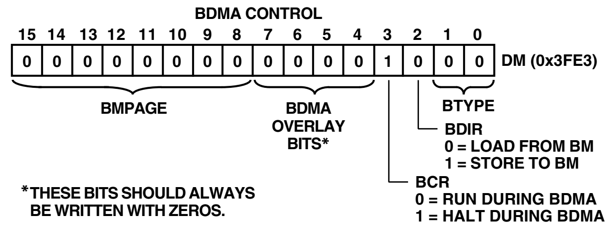


Figure 9. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table VI shows the data formats supported by the BDMA circuit.

Table VI. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. For ADSP-2186M, set to zero BDMA overlay bits in BDMA control register.

The BMWAIT field, which has four bits on ADSP-2186M, allows selection of up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2186M. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks IACK control line to see if the DSP is busy.
3. Host uses IS and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of bits 7:0 represent the IDMA overlay: bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.
4. Host uses IS and IRD (or IWR) to read (or write) DSP internal memory (PM or DM).
5. Host checks IACK line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-2186M is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal (IS) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-2186M's on-chip memory. Asserting the select line (IS) and the appropriate read or write line (IRD and IWR respectively) signals the ADSP-2186M that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select (IS) and address latch enable (IAL) directs the ADSP-2186M to write the address onto the IAD0–14 bus into the IDMA Control Register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 31 applies for short reads. When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 32. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.

Refer to the following figures for more information on IDMA and DMA memory maps.

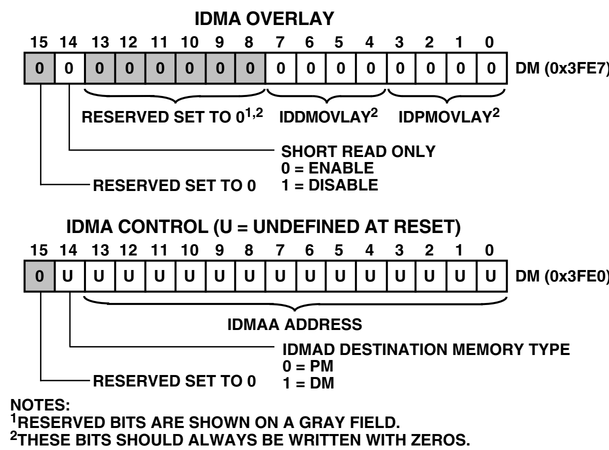


Figure 10. IDMA Control/OVLAY Registers

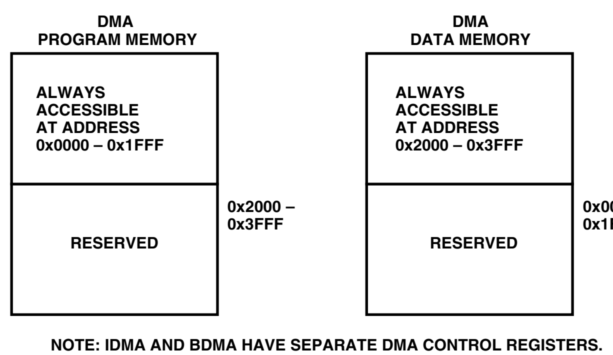


Figure 11. Direct Memory Access—PM and DM Memory Maps

Bootstrap Loading (Booting)

The ADSP-2186M has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the MODE pins specify BDMA booting, the ADSP-2186M initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory.

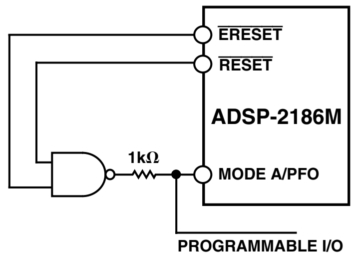


Figure 12. Mode A Pin/EZ-ICE Circuit

See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-2186M pins: $\overline{EBR}$, $\overline{EINT}$, EE, $\overline{EBG}$, ECLK, $\overline{ERESET}$, ELIN, $\overline{EMS}$, and ELOUT

These ADSP-2186M pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2186M and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{BR}$, $\overline{BG}$, $\overline{RESET}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2186M in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$, and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$, and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in Figure 13. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

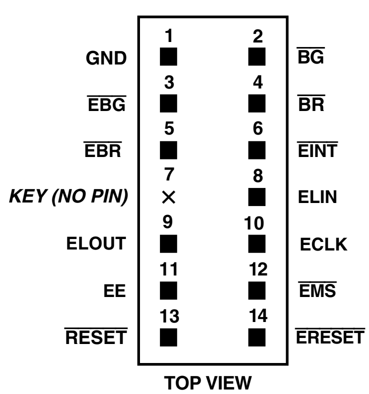


Figure 13. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ- ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface

For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, AND CM

Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ- ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst-case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2186M ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ- ICE board's DSP.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Value Min	Value Max
Internal Supply Voltage (V_{DDINT})	–0.3 V	+3.0 V
External Supply Voltage (V_{DDEXT})	–0.3 V	+4.0 V
Input Voltage[2]	–0.5 V	+4.0 V
Output Voltage Swing[3]	–0.5 V	V_{DDEXT} + 0.5 V
Operating Temperature Range	–40°C	+85°C
Storage Temperature Range	–65°C	+150°C
Lead Temperature (5 sec) LQFP		280°C

NOTES

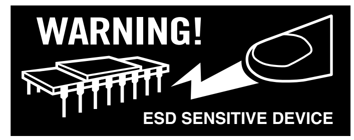
[1]Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Applies to Bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and Input only pins (CLKIN, $\overline{RESET}$, $\overline{BR}$, DR0, DR1, $\overline{PWD}$).

[3]Applies to Output pins ($\overline{BG}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{IOMS}$, $\overline{CMS}$, $\overline{RD}$, $\overline{WR}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{BGH}$).

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2186M features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



TIMING SPECIFICATIONS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-2186M timing parameters, for your convenience.

Memory Device Specification	Parameter	Timing Parameter Definition[1]
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{xMS}$ Hold before $\overline{WR}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
OE to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid

NOTE

[1]$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$ or $\overline{IOMS}$.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2186M uses an input clock with a frequency equal to half the instruction rate. For example, a 37.50 MHz input clock (which is equivalent to 26.6 ns) yields a 13.3 ns processor cycle (equivalent to 75 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: $t_{CKH} = 0.5\ t_{CK} - 2\ ns = 0.5\ (15\ ns) - 2\ ns = 5.5\ ns$

ENVIRONMENTAL CONDITIONS[1]

Rating Description	Symbol	LQFP	Mini-BGA
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48°C/W	63.3°C/W
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50°C/W	70.7°C/W
Thermal Resistance (Junction-to-Case)	θ_{JC}	2°C/W	7.4°C/W

NOTE
[1]Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DDEXT} = 3.3 V and t_{CK} = 30 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DDEXT}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 15).

$(C \times V_{DDEXT}^2 \times f)$ is calculated for each output:

Parameters	# of Pins	× C pF	× V_{DDEXT}^2 V	× f MHz	PD mW
Address	7	10	3.3^2	16.67	12.7
Data Output, $\overline{WR}$	9	10	3.3^2	16.67	16.3
$\overline{RD}$	1	10	3.3^2	16.67	1.8
CLKOUT, $\overline{DMS}$	2	10	3.3^2	33.3	7.2
					38.0

Total power dissipation for this example is P_{INT} + 38.0 mW.

Output Drive Currents

Figure 14 shows typical I-V characteristics for the output drivers on the ADSP-2186M. The curves represent the current drive capability of the output drivers as a function of output voltage.

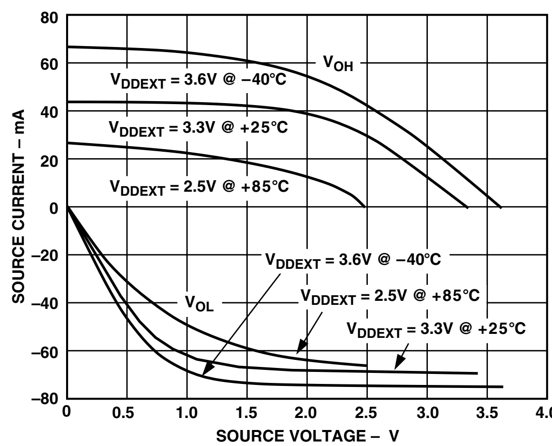
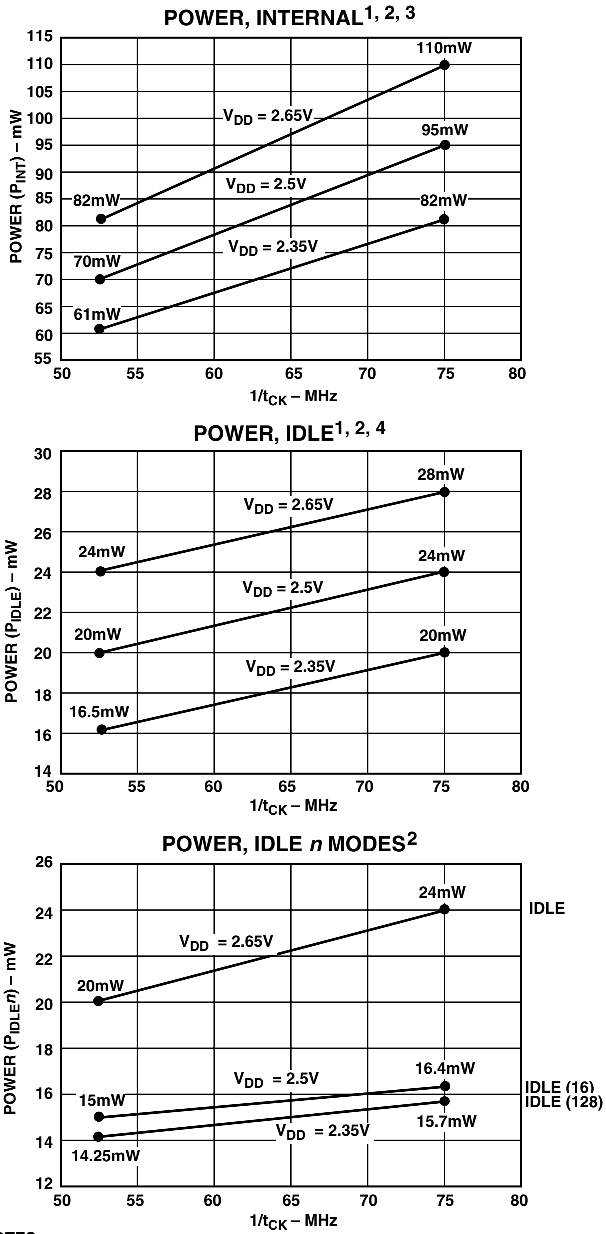


Figure 14. Typical Output Driver Characteristics



NOTES:
VALID FOR ALL TEMPERATURE GRADES.
[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] TYPICAL POWER DISSIPATION AT 2.5V V_{DDINT} AND 25°C, EXCEPT WHERE SPECIFIED.
[3] I_{DD} MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
[4] IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 15. Power vs. Frequency

Capacitive Loading

Figure 16 and Figure 17 show the capacitive loading characteristics of the ADSP-2186M.

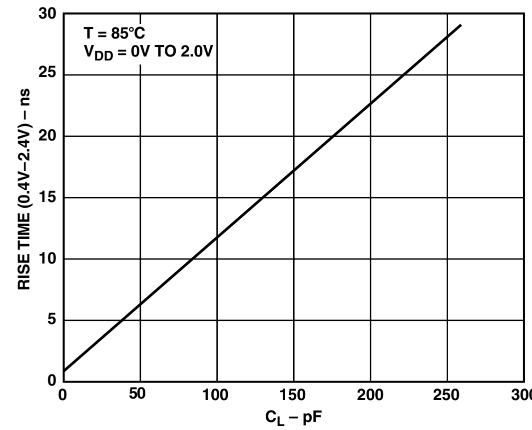


Figure 16. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

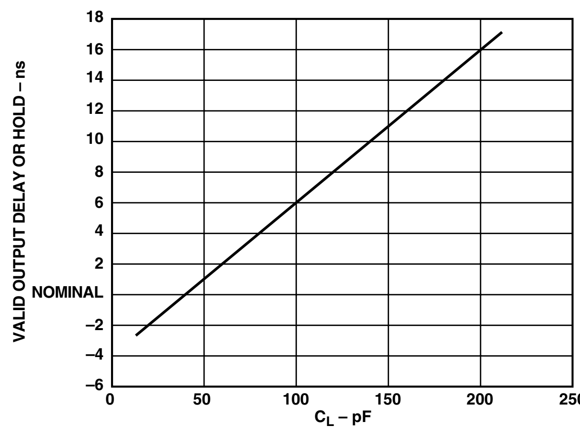


Figure 17. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	3		ns
t_{IKA}	$\overline{\text{IACK}}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{\text{IS}}$ Low and IAL High.
[2]End of Address Latch = $\overline{\text{IS}}$ High or IAL Low.
[3]Start of Write or Read = $\overline{\text{IS}}$ Low and $\overline{\text{IWR}}$ Low or $\overline{\text{IRD}}$ Low.

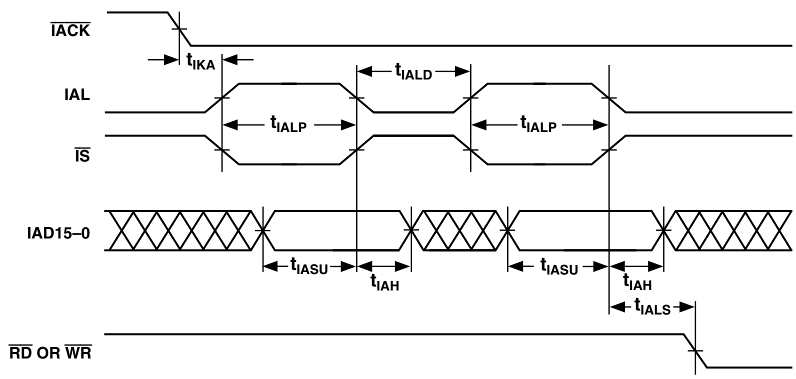


Figure 27. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{\text{IACK}}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	$0.5t_{CK} + 5$		ns
t_{IKH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{\text{IACK}}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{\text{IACK}}$ High		10	ns

NOTES
[1]Start of Write = $\overline{\text{IS}}$ Low and $\overline{\text{IWR}}$ Low.
[2]If Write Pulse ends before $\overline{\text{IACK}}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{\text{IACK}}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{\text{IACK}}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

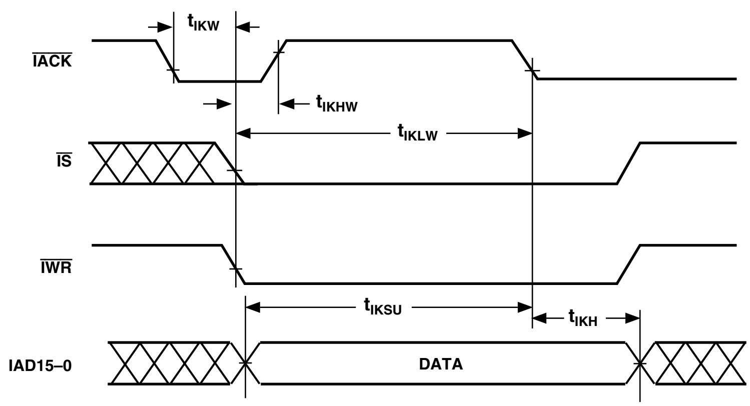


Figure 29. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle in Short Read Only Mode[1]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

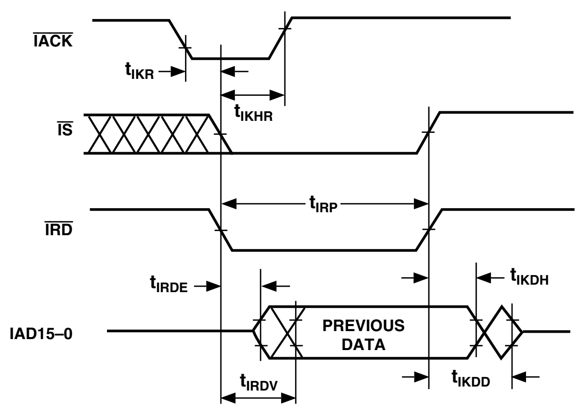


Figure 32. IDMA Read, Short Read Only Cycle

The LQFP package pinout is shown in the table below. Pin names in bold text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

LQFP Package Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A4/**IAD3**	26	$\overline{\text{IRQE}}$ + PF4	51	$\overline{\text{EBR}}$	76	D16
2	A5/**IAD4**	27	$\overline{\text{IRQL0}}$ + PF5	52	$\overline{\text{BR}}$	77	D17
3	GND	28	GND	53	$\overline{\text{EBG}}$	78	D18
4	A6/**IAD5**	29	$\overline{\text{IRQL1}}$ + PF6	54	$\overline{\text{BG}}$	79	D19
5	A7/**IAD6**	30	$\overline{\text{IRQ2}}$ + PF7	55	D0/**IAD13**	80	GND
6	A8/**IAD7**	31	DT0	56	D1/**IAD14**	81	D20
7	A9/**IAD8**	32	TFS0	57	D2/**IAD15**	82	D21
8	A10/**IAD9**	33	RFS0	58	D3/**$\overline{\text{IACK}}$**	83	D22
9	A11/**IAD10**	34	DR0	59	V_{DDINT}	84	D23
10	A12/**IAD11**	35	SCLK0	60	GND	85	FL2
11	A13/**IAD12**	36	V_{DDEXT}	61	D4/**$\overline{\text{IS}}$**	86	FL1
12	GND	37	DT1/FO	62	D5/**IAL**	87	FL0
13	CLKIN	38	TFS1/$\overline{\text{IRQ1}}$	63	D6/**$\overline{\text{IRD}}$**	88	PF3 [MODE D]
14	XTAL	39	RFS1/$\overline{\text{IRQ0}}$	64	D7/**$\overline{\text{IWR}}$**	89	PF2 [MODE C]
15	V_{DDEXT}	40	DR1/FI	65	D8	90	V_{DDEXT}
16	CLKOUT	41	GND	66	GND	91	$\overline{\text{PWD}}$
17	GND	42	SCLK1	67	V_{DDEXT}	92	GND
18	V_{DDINT}	43	$\overline{\text{ERESET}}$	68	D9	93	PF1 [MODE B]
19	$\overline{\text{WR}}$	44	$\overline{\text{RESET}}$	69	D10	94	PF0 [MODE A]
20	$\overline{\text{RD}}$	45	$\overline{\text{EMS}}$	70	D11	95	$\overline{\text{BGH}}$
21	$\overline{\text{BMS}}$	46	EE	71	GND	96	PWDACK
22	$\overline{\text{DMS}}$	47	ECLK	72	D12	97	A0
23	$\overline{\text{PMS}}$	48	ELOUT	73	D13	98	A1/**IAD0**
24	$\overline{\text{IOMS}}$	49	ELIN	74	D14	99	A2/**IAD1**
25	$\overline{\text{CMS}}$	50	$\overline{\text{EINT}}$	75	D15	100	A3/**IAD2**