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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	66MHz
Non-Volatile Memory	External
On-Chip RAM	40kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2186mbstz266r

ADSP-2186M* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Application Notes

- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-334: Digital Signal Processing Techniques
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
- EE-131: Booting the ADSP-2191/95/96 DSPs
- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs

Common-Mode Pins

Pin Name	# of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2}}$ *PF7*	1	I I/O	Edge- or Level-Sensitive Interrupt Request[1] Programmable I/O Pin
$\overline{\text{IRQL1}}$ *PF6*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQL0}}$ *PF5*	1	I I/O	Level-Sensitive Interrupt Requests[1] Programmable I/O Pin
$\overline{\text{IRQE}}$ *PF4*	1	I I/O	Edge-Sensitive Interrupt Requests[1] Programmable I/O Pin
Mode D *PF3*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode C *PF2*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode B *PF1*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
Mode A *PF0*	1	I I/O	Mode Select Input—Checked Only During $\overline{\text{RESET}}$ Programmable I/O Pin During Normal Operation
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1 $\overline{\text{IRQ1:0}}$, FI, FO	5	I/O	Serial Port I/O Pins Edge- or Level-Sensitive Interrupts, FI, FO[2]
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (2.5 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (2.5 V or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)
V_{DDINT}	4	I	Internal V_{DD} (2.5 V) Power (Mini-BGA)
V_{DDEXT}	7	I	External V_{DD} (2.5 V or 3.3 V) Power (Mini-BGA)
GND	20	I	Ground (Mini-BGA)
EZ-Port	9	I/O	For Emulation Use

NOTES
[1]Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, then the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices, or set as a programmable flag.
[2]SPORT configuration determined by the DSP System Control Register. Software configurable.

Memory Interface Pins

The ADSP-2186M processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

The following tables list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinout tables.

Full Memory Mode Pins (Mode C = 0)

Pin Name	# of Pins	I/O	Function
A13:0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23:0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Host Mode Pins (Mode C = 1)

Pin Name	# of Pins	I/O	Function
IAD15:0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access[1]
D23:8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D; Open Drain

NOTE

[1]In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

Terminating Unused Pins
The following table shows the recommendations for terminating unused pins.

Pin Terminations

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD12:0	I/O (Z)	Hi-Z	$\overline{IS}$	Float
A0	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	I		High or Low
DT1/FO	O	O		Float
$\overline{EE}$	I	I		Float
$\overline{EBR}$	I	I		Float
$\overline{EBG}$	O	O		Float
$\overline{ERESET}$	I	I		Float
$\overline{EMS}$	O	O		Float
$\overline{EINT}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

NOTES
*Hi-Z = High Impedance.
1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1, prior to enabling interrupts, and let pins float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, $\overline{RESET}$, and PF3:0/MODE D:A are not included in the table because these pins must be used.

Interrupts

The interrupt controller allows the processor to respond to the 11 possible interrupts and reset with minimum overhead. The ADSP-2186M provides four dedicated external interrupt input pins: $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, and $\overline{IRQE}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI and FO, for a total of six external interrupts. The ADSP-2186M also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power- down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$, and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2186M masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ external interrupts to be either edge- or level-sensitive. The $\overline{IRQE}$ pin is an external edge sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2186M has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2186M processor has a low power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{PWD}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{RESET}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the ADSP-2186M is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA and autobuffer cycle steals still occur.

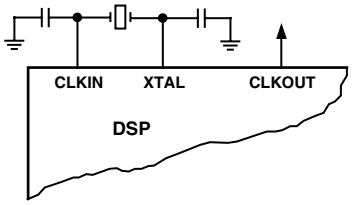


Figure 3. External Crystal Connections

RESET

The RESET signal initiates a master reset of the ADSP-2186M. The RESET signal must be asserted during the power-up sequence to assure proper initialization. RESET during initial power-up must be held long enough to allow the internal clock to stabilize. If RESET is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the RESET signal should be held low. On any subsequent resets, the RESET signal must meet the minimum pulsewidth specification, t_{RSP}.

The RESET input contains some hysteresis; however, if an RC circuit is used to generate the RESET signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When RESET is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Power Supplies

The ADSP-2186M has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply can be connected to either a 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.5 V and 3.3 V components.

MODES OF OPERATION

Setting Memory Mode

Memory Mode selection for the ADSP-2186M is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

Table II. Modes of Operation

MODE D	MODE C	MODE B	MODE A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. IACK has active pull-down. (REQUIRES ADDITIONAL HARDWARE).
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; IACK requires external pull down. (REQUIRES ADDITIONAL HARDWARE)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK requires external pull-down.[1]

NOTE
[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

Table V. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)
The ADSP-2186M has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)
The ADSP-2186M's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2186M supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)
The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

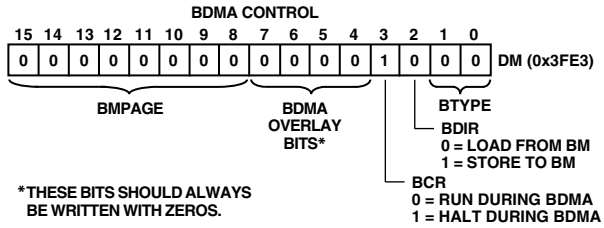


Figure 9. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table VI shows the data formats supported by the BDMA circuit.

Table VI. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. For ADSP-2186M, set to zero BDMA overlay bits in BDMA control register.

The BMWAIT field, which has four bits on ADSP-2186M, allows selection of up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2186M. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of bits 7:0 represent the IDMA overlay: bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-2186M is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-2186M's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-2186M that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-2186M to write the address onto the IAD0–14 bus into the IDMA Control Register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 31 applies for short reads. When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 32. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.

Refer to the following figures for more information on IDMA and DMA memory maps.

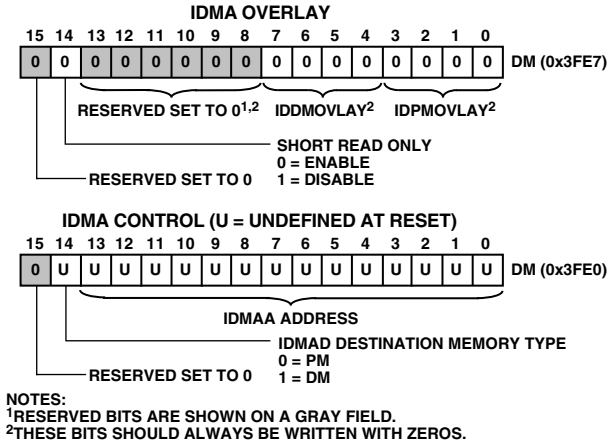
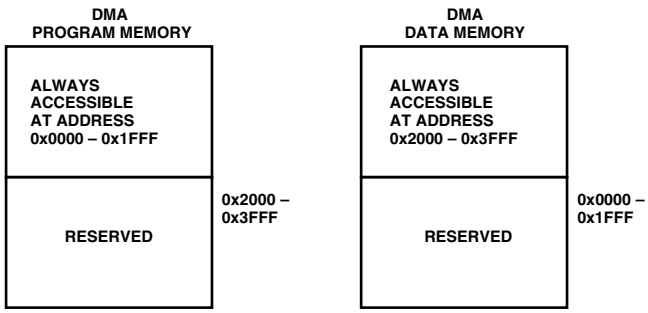


Figure 10. IDMA Control/OVLAY Registers



NOTE: IDMA AND BDMA HAVE SEPARATE DMA CONTROL REGISTERS.

Figure 11. Direct Memory Access—PM and DM Memory Maps

Bootstrap Loading (Booting)

The ADSP-2186M has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the MODE pins specify BDMA booting, the ADSP-2186M initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory.

These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte-memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-2186M. The only memory address bit provided by the processor is A0.

IDMA Port Booting
The ADSP-2186M can also boot programs through its Internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-2186M boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

Bus Request and Bus Grant
The ADSP-2186M can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2186M is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-2186M will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2186M is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2186M requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2186M deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

Flag I/O Pins
The ADSP-2186M has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2186M's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2186M has five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0–FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

Instruction Set Description
The ADSP-2186M assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2186M's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM
The ADSP-2186M has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in Setting Memory Modes), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{RESET}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 12. This circuit forces the value located on the Mode A pin to logic high; regardless of whether it is latched via the $\overline{RESET}$ or $\overline{ERESET}$ pin.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Value Min	Value Max
Internal Supply Voltage (V_{DDINT})	–0.3 V	+3.0 V
External Supply Voltage (V_{DDEXT})	–0.3 V	+4.0 V
Input Voltage[2]	–0.5 V	+4.0 V
Output Voltage Swing[3]	–0.5 V	V_{DDEXT} + 0.5 V
Operating Temperature Range	–40°C	+85°C
Storage Temperature Range	–65°C	+150°C
Lead Temperature (5 sec) LQFP		280°C

NOTES
[1]Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Applies to Bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and Input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[3]Applies to Output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2186M features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY TIMING SPECIFICATIONS

The table below shows common memory device specifications and the corresponding ADSP-2186M timing parameters, for your convenience.

Memory Device Specification	Parameter	Timing Parameter Definition[1]
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{\text{xMS}}$ Setup before $\overline{\text{WR}}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{\text{xMS}}$ Setup before $\overline{\text{WR}}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{\text{xMS}}$ Hold before $\overline{\text{WR}}$ Low
Data Setup Time	t_{DW}	Data Setup before $\overline{\text{WR}}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{\text{WR}}$ High
OE to Data Valid	t_{RDD}	$\overline{\text{RD}}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{\text{xMS}}$ to Data Valid

NOTE
[1]$\overline{\text{xMS}}$ = $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$ or $\overline{\text{IOMS}}$.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

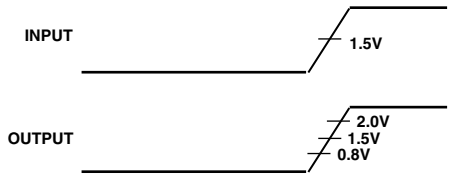


Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown Figure 19. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

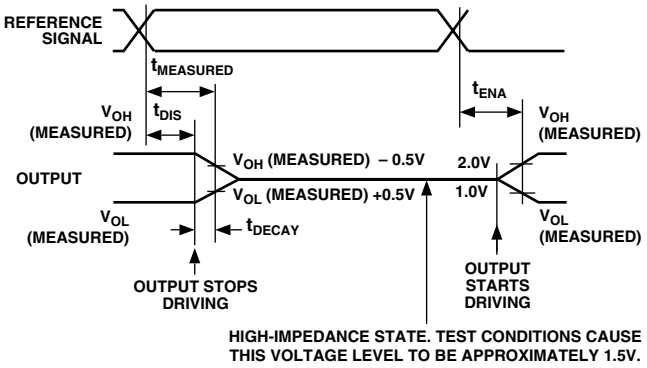


Figure 19. Output Enable/Disable

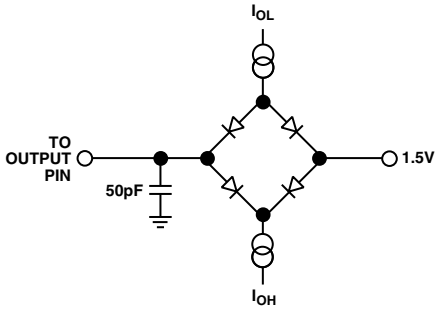


Figure 20. Equivalent Loading for AC Measurements (Including All Fixtures)

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK}$ + 10		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK}$ – 5		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK}$ + 4	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag Outputs = PFx, FL0, FL1, FL2, FO.

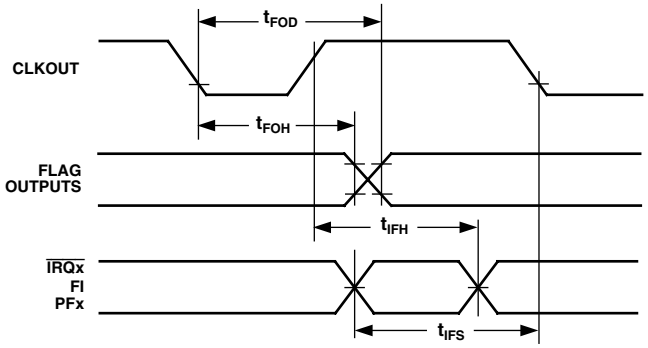


Figure 22. Interrupts and Flags

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

NOTES
w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

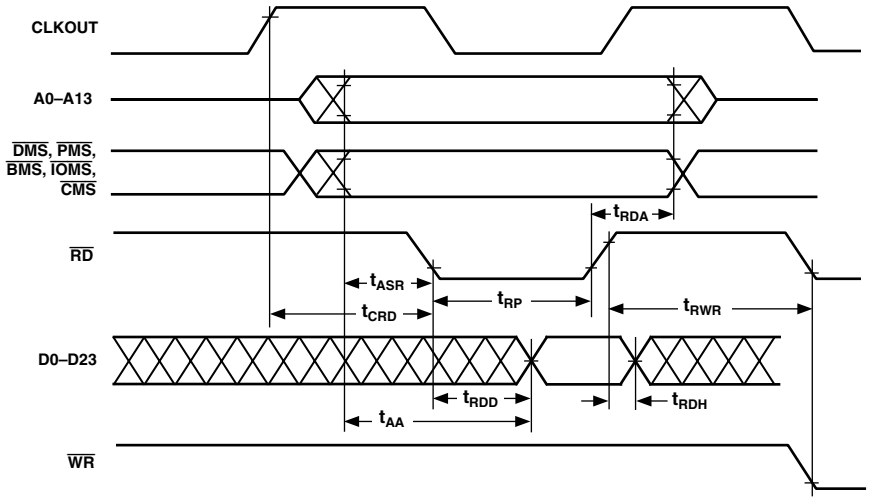


Figure 24. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 4 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 1$		ns
t_{WP}	$\overline{WR}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 3$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 2$	$0.25\ t_{CK} + 4$	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 5 + w$		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 1$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

NOTES
w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

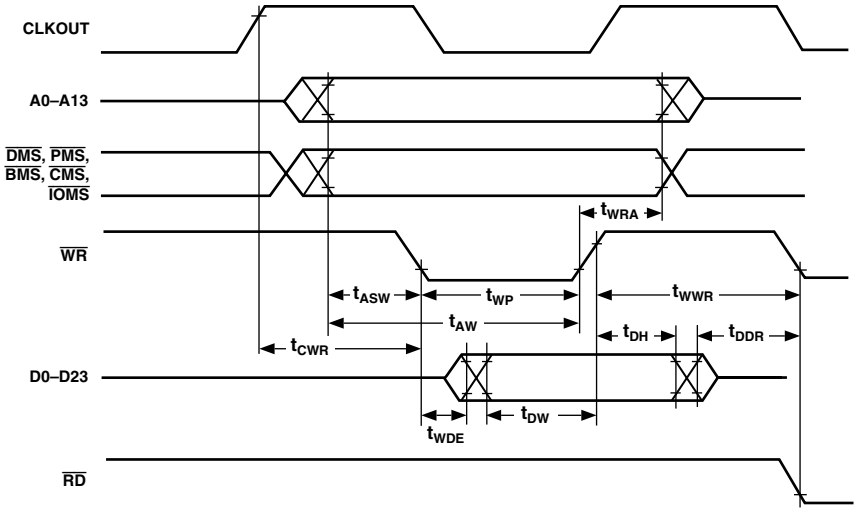


Figure 25. Memory Write

Serial Ports

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	26.6		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK}$ + 6	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		12	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		12	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		12	ns
t_{SCDD}	SCLK High to DT Disable		12	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		12	ns

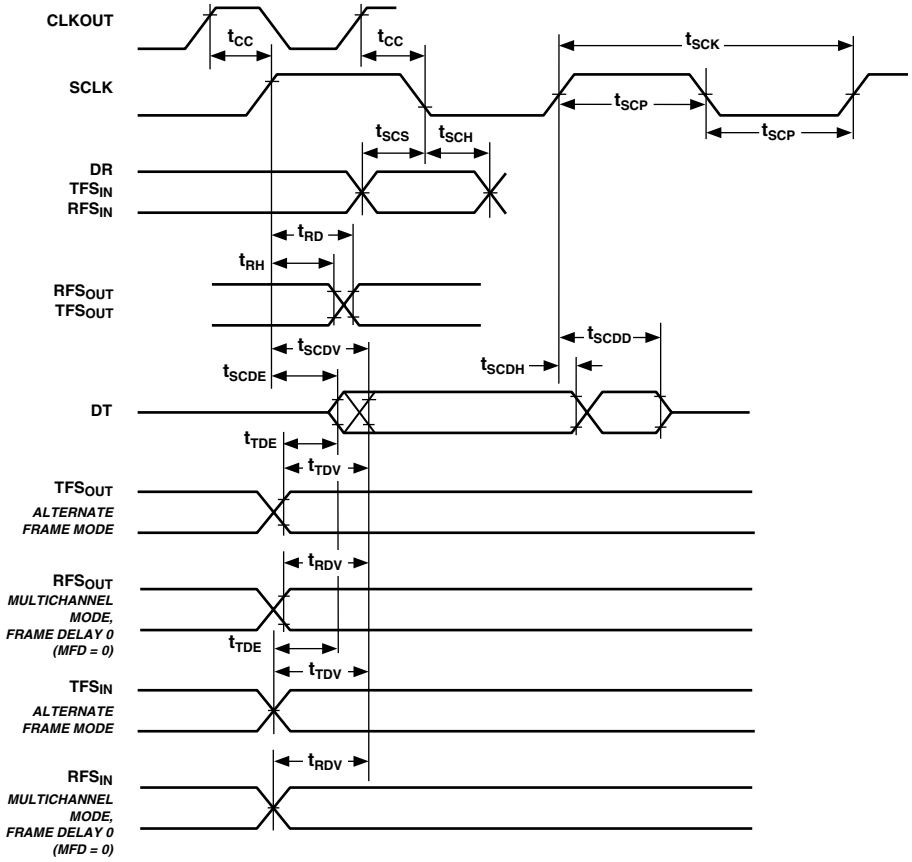


Figure 26. Serial Ports

The LQFP package pinout is shown in the table below. Pin names in bold text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of RESET.

The multiplexed pins DT1/FO, TFS1/IRQ1, RFS1/IRQ0, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

LQFP Package Pinout

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	A4/**IAD3**	26	IRQE + PF4	51	EBR	76	D16
2	A5/**IAD4**	27	IRQL0 + PF5	52	BR	77	D17
3	GND	28	GND	53	EBG	78	D18
4	A6/**IAD5**	29	IRQL1 + PF6	54	BG	79	D19
5	A7/**IAD6**	30	IRQ2 + PF7	55	D0/**IAD13**	80	GND
6	A8/**IAD7**	31	DT0	56	D1/**IAD14**	81	D20
7	A9/**IAD8**	32	TFS0	57	D2/**IAD15**	82	D21
8	A10/**IAD9**	33	RFS0	58	D3/**IACK**	83	D22
9	A11/**IAD10**	34	DR0	59	V_{DDINT}	84	D23
10	A12/**IAD11**	35	SCLK0	60	GND	85	FL2
11	A13/**IAD12**	36	V_{DDEXT}	61	D4/**IS**	86	FL1
12	GND	37	DT1/FO	62	D5/**IAL**	87	FL0
13	CLKIN	38	TFS1/IRQ1	63	D6/**IRD**	88	PF3 [MODE D]
14	XTAL	39	RFS1/IRQ0	64	D7/**IWR**	89	PF2 [MODE C]
15	V_{DDEXT}	40	DR1/FI	65	D8	90	V_{DDEXT}
16	CLKOUT	41	GND	66	GND	91	PWD
17	GND	42	SCLK1	67	V_{DDEXT}	92	GND
18	V_{DDINT}	43	ERESET	68	D9	93	PF1 [MODE B]
19	WR	44	RESET	69	D10	94	PF0 [MODE A]
20	RD	45	EMS	70	D11	95	BGH
21	BMS	46	EE	71	GND	96	PWDACK
22	DMS	47	ECLK	72	D12	97	A0
23	PMS	48	ELOUT	73	D13	98	A1/**IAD0**
24	IOMS	49	ELIN	74	D14	99	A2/**IAD1**
25	CMS	50	EINT	75	D15	100	A3/**IAD2**

144-Ball Mini-BGA Package Pinout (Bottom View)

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{PWD}$	A7/IAD6	A5/IAD4	$\overline{RD}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{BGH}$	NC	$\overline{WR}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{IWR}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{IS}$	NC	NC	D5/IAL	D6/$\overline{IRD}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{IACK}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{BG}$	RFS1/$\overline{IRQ0}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{EBG}$	$\overline{BR}$	$\overline{EBR}$	$\overline{ERESET}$	SCLK1	TFS1/$\overline{IRQ1}$	RFS0	$\overline{DMS}$	$\overline{BMS}$	NC	NC	NC	K
$\overline{EINT}$	ELOUT	ELIN	$\overline{RESET}$	GND	DR0	$\overline{PMS}$	GND	$\overline{IOMS}$	$\overline{IRQL1}$ + PF6	NC	$\overline{IRQE}$ + PF4	L
ECLK	EE	$\overline{EMS}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{CMS}$	NC	$\overline{IRQ2}$ + PF7	$\overline{IRQL0}$ + PF5	M

The Mini-BGA package pinout is shown in the table below. Pin names in **bold** text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

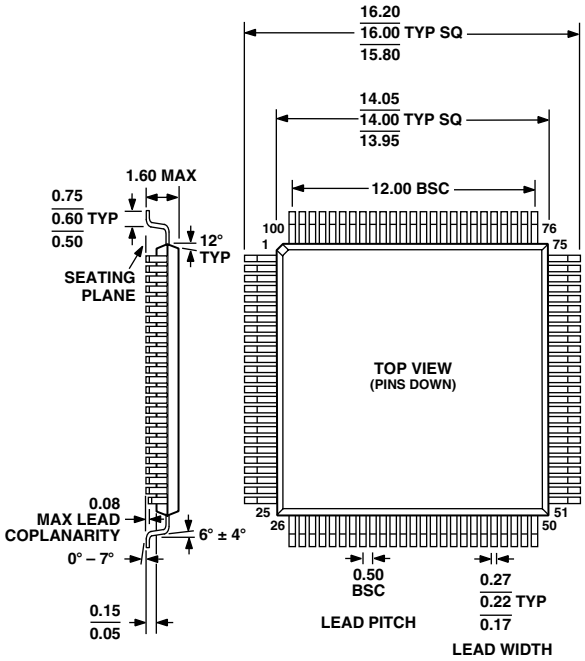
Mini-BGA Package Pinout

Ball #	Pin Name	Ball #	Pin Name	Ball #	Pin Name	Ball #	Pin Name
A01	A2/**IAD1**	D01	NC	G01	XTAL	K01	NC
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/**IAD8**	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/$\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/**$\overline{\text{IRD}}$**	K08	SCLK1
A09	NC	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/**$\overline{\text{IS}}$**	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	V_{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/**IAD2**	E02	V_{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V_{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V_{DDEXT}	E07	PF3 [MODE D]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/**$\overline{\text{IACK}}$**	L09	$\overline{\text{RESET}}$
B10	D18	E10	V_{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/**IAD5**	F02	NC	J02	V_{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	NC	M03	NC
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	V_{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	V_{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V_{DDEXT}	F07	NC	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/**$\overline{\text{IWR}}$**	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V_{DDINT}	M11	EE
C12	D14	F12	D9	J12	V_{DDINT}	M12	ECLK

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

100-Lead Metric Thin Plastic Quad Flatpack (LQFP) (ST-100)

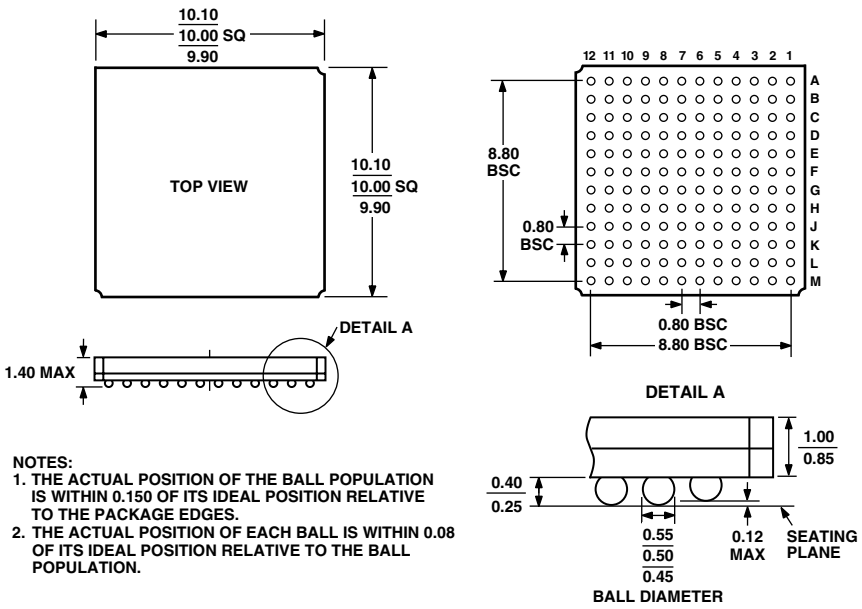


NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

144-Ball Mini-BGA
(CA-144)



NOTES:
1. THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.150 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate	Package Description*	Package Option
ADSP-2186MKST-300	0°C to 70°C	75	100-Lead LQFP	ST-100
ADSP-2186MBST-266	–40°C to +85°C	66	100-Lead LQFP	ST-100
ADSP-2186MKCA-300	0°C to 70°C	75	144-Ball Mini-BGA	CA-144
ADSP-2186MBCA-266	–40°C to +85°C	66	144-Ball Mini-BGA	CA-144

*In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously labeled TQFP packages (1.6 mm thick) are now designated as LQFP.

C02048–3.5–10/00 (rev. 0)

PRINTED IN U.S.A.