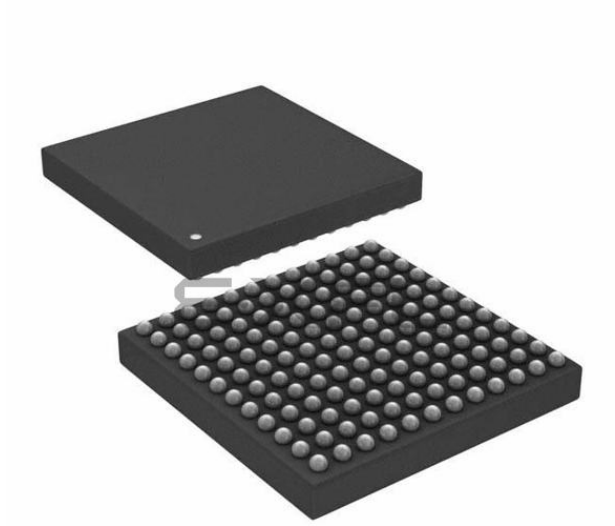

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | Fixed Point |
| Interface | Host Interface, Serial Port |
| Clock Rate | 75MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 40kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 2.50V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LFBGA |
| Supplier Device Package | 144-MiniBGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-2186mkcaz-300 |

# ADSP-2186M* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Application Notes**

- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-334: Digital Signal Processing Techniques
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
- EE-131: Booting the ADSP-2191/95/96 DSPs
- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs

- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board
- EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
- EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0++
- EE-153: ADSP-2191 Programmable PLL
- EE-154: ADSP-2191 Host Port Interface
- EE-156: Support for the H.100 protocol on the ADSP-2191
- EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-164: Advanced EPROM Boot and No-boot Scenarios with ADSP-219x DSPs
- EE-168: Using Third Overtone Crystals with the ADSP-218x DSP
- EE-17: ADSP-2187L Memory Organization
- EE-18: Choosing and Using FFTs for ADSP-21xx
- EE-188: Using C To Implement Interrupt-Driven Systems On ADSP-219x DSPs
- EE-2: Using ADSP-218x I/O Space
- EE-226: ADSP-2191 DSP Host Port Booting
- EE-227: CAN Configuration Procedure for ADSP-21992 DSPs
- EE-249: Implementing Software Overlays on ADSP-218x DSPs with VisualDSP++®
- EE-32: Language Extensions: Memory Storage Types, ASM & Inline Constructs
- EE-33: Programming The ADSP-21xx Timer In C
- EE-35: Troubleshooting your ADSP-218x EZ-ICE
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-36: ADSP-21xx Interface to the IOM-2 bus
- EE-38: ADSP-2181 IDMA Port - Cycle Steal Timing
- EE-39: Interfacing 5V Flash Memory to an ADSP-218x (Byte Programming Algorithm)
- EE-48: Converting Legacy 21xx Systems To A 218x System Design
- EE-5: ADSP-218x Full Memory Mode vs. Host Memory Mode
- EE-60: Simulating an RS-232 UART Using the Synchronous Serial Ports on the ADSP-21xx Family DSPs
- EE-64: Setting Mode Pins on Reset
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-71: Minimum Rise Time Specs for Critical Interrupt and Clock Signals on the ADSP-21x1/21x5
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-78: BDMA Usage on 100 pin ADSP-218x DSPs Configured for IDMA Use
- EE-79: EPROM Booting In Host Mode with 100 Pin 218x Processors
- EE-82: Using an ADSP-2181 DSP's IO Space to IDMA Boot Another ADSP-2181
- EE-89: Implementing A Software UART on the ADSP-2181 EZ-Kit-Lite
- EE-90: Using the 21xx C-FFT Library
- EE-96: Interfacing Two AD73311 Codecs to the ADSP-218x

**Data Sheet**

- ADSP-2186M: 16-Bit, 75 MIPS, 2.5V, 2 Serial Ports, Host Port, 40 KB RAM Data Sheet

**Evaluation Kit Manuals**

- ADSP-218x DSP family and ADSP-2192 EZ-KIT Lite® Installation Procedure -Non-USB

**Integrated Circuit Anomalies**

- ADSP-2186M Anomaly List for Revision 2.0

**Processor Manuals**

- ADSP 21xx Processors: Manuals
- ADSP-218x DSP Hardware Reference
- ADSP-218x DSP Instruction Set Reference
- Using the ADSP-2100 Family Volume 1
- Using the ADSP-2100 Family Volume 2

**Software Manuals**

- VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
- VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
- VisualDSP++ 3.5 C/C++ Compiler and Library Manual for ADSP-219x Processors
- VisualDSP++ 3.5 Component Software Engineering User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Getting Started Guide for 16-Bit Processors
- VisualDSP++ 3.5 Kernel VDK User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
- VisualDSP++ 3.5 Loader Manual for 16-Bit Processors
- VisualDSP++ 3.5 User's Guide for 16-Bit Processors

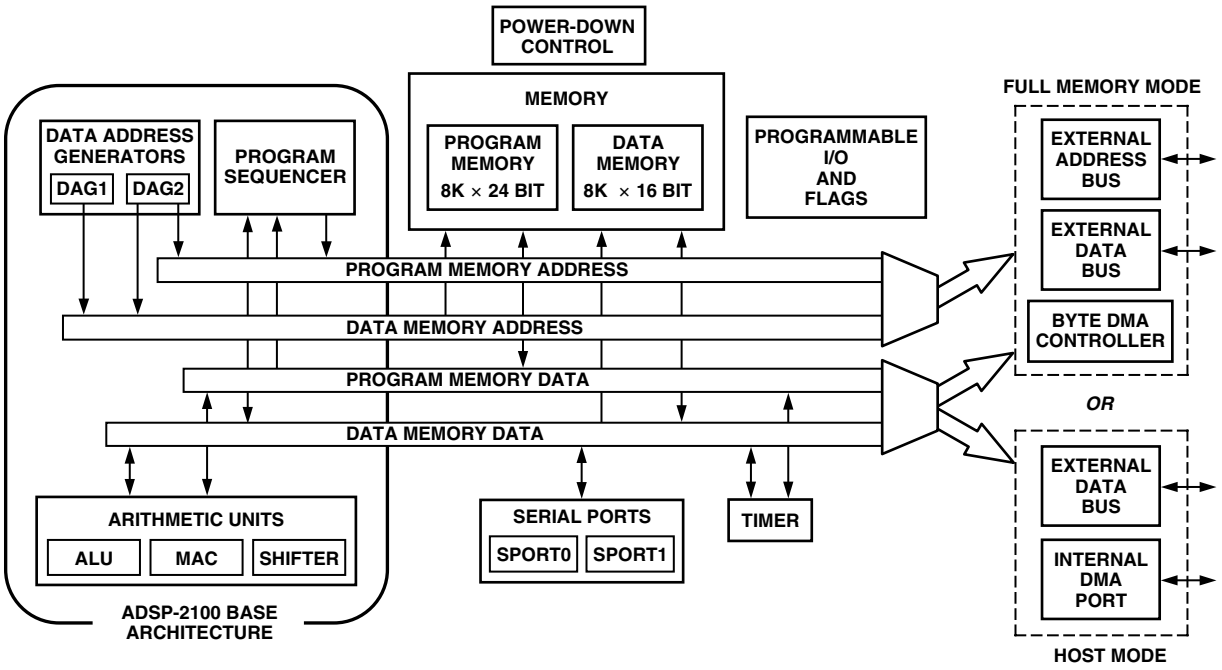



*Figure 1. Functional Block Diagram*

**ARCHITECTURE OVERVIEW**

The ADSP-2186M instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2186M assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2186M. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2186M executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2186M to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2186M can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, the ADSP-2186M may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of

**Memory Interface Pins**

The ADSP-2186M processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

The following tables list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinout tables.

**Full Memory Mode Pins (Mode C = 0)**

| Pin Name | # of Pins | I/O | Function |
|---|---|---|---|
| A13:0 | 14 | O | Address Output Pins for Program, Data, Byte, and I/O Spaces |
| D23:0 | 24 | I/O | Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.) |

**Host Mode Pins (Mode C = 1)**

| Pin Name | # of Pins | I/O | Function |
|---|---|---|---|
| IAD15:0 | 16 | I/O | IDMA Port Address/Data Bus |
| A0 | 1 | O | Address Pin for External I/O, Program, Data, or Byte Access[1] |
| D23:8 | 16 | I/O | Data I/O Pins for Program, Data, Byte, and I/O Spaces |
| $\overline{\text{IWR}}$ | 1 | I | IDMA Write Enable |
| $\overline{\text{IRD}}$ | 1 | I | IDMA Read Enable |
| IAL | 1 | I | IDMA Address Latch Pin |
| $\overline{\text{IS}}$ | 1 | I | IDMA Select |
| $\overline{\text{IACK}}$ | 1 | O | IDMA Port Acknowledge Configurable in Mode D; Open Drain |

NOTE

[1]In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

**Terminating Unused Pins**
The following table shows the recommendations for terminating unused pins.

**Pin Terminations**

| Pin Name | I/O 3-State (Z) | Reset State | Hi-Z* Caused By | Unused Configuration |
|---|---|---|---|---|
| XTAL | I | I | | Float |
| CLKOUT | O | O | | Float |
| A13:1 or | O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| IAD12:0 | I/O (Z) | Hi-Z | $\overline{IS}$ | Float |
| A0 | O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| D23:8 | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| D7 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IWR}$ | I | I | | High (Inactive) |
| D6 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IRD}$ | I | I | $\overline{BR}$, $\overline{EBR}$ | High (Inactive) |
| D5 or | I/O (Z) | Hi-Z | | Float |
| IAL | I | I | | Low (Inactive) |
| D4 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IS}$ | I | I | | High (Inactive) |
| D3 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IACK}$ | | | | Float |
| D2:0 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| IAD15:13 | I/O (Z) | Hi-Z | $\overline{IS}$ | Float |
| $\overline{PMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{DMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{BMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IOMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{CMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{RD}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{WR}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{BR}$ | I | I | | High (Inactive) |
| $\overline{BG}$ | O (Z) | O | EE | Float |
| $\overline{BGH}$ | O | O | | Float |
| $\overline{IRQ2}$/*PF7* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQL1}$/*PF6* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQL0}$/*PF5* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQE}$/*PF4* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| SCLK0 | I/O | I | | Input = High or Low, Output = Float |
| RFS0 | I/O | I | | High or Low |
| DR0 | I | I | | High or Low |
| TFS0 | I/O | I | | High or Low |
| DT0 | O | O | | Float |
| SCLK1 | I/O | I | | Input = High or Low, Output = Float |
| RFS1/$\overline{IRQ0}$ | I/O | I | | High or Low |
| DR1/FI | I | I | | High or Low |
| TFS1/$\overline{IRQ1}$ | I/O | I | | High or Low |
| DT1/FO | O | O | | Float |
| $\overline{EE}$ | I | I | | Float |
| $\overline{EBR}$ | I | I | | Float |
| $\overline{EBG}$ | O | O | | Float |
| $\overline{ERESET}$ | I | I | | Float |
| $\overline{EMS}$ | O | O | | Float |
| $\overline{EINT}$ | I | I | | Float |
| ECLK | I | I | | Float |
| ELIN | I | I | | Float |
| ELOUT | O | O | | Float |

NOTES
*Hi-Z = High Impedance.
1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1, prior to enabling interrupts, and let pins float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, $\overline{RESET}$, and PF3:0/MODE D:A are not included in the table because these pins must be used.

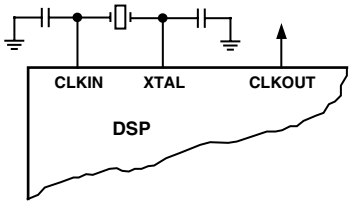



*Figure 3. External Crystal Connections*

**RESET**

The RESET signal initiates a master reset of the ADSP-2186M. The RESET signal must be asserted during the power-up sequence to assure proper initialization. RESET during initial power-up must be held long enough to allow the internal clock to stabilize. If RESET is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid $V_{DD}$ is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the RESET signal should be held low. On any subsequent resets, the RESET signal must meet the minimum pulsewidth specification, $t_{RSP}$.

The RESET input contains some hysteresis; however, if an RC circuit is used to generate the RESET signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When RESET is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

**Power Supplies**

The ADSP-2186M has separate power supply connections for the internal ($V_{DDINT}$) and external ($V_{DDEXT}$) power supplies. The internal supply must meet the 2.5 V requirement. The external supply can be connected to either a 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V, regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.5 V and 3.3 V components.

## MODES OF OPERATION

**Setting Memory Mode**

Memory Mode selection for the ADSP-2186M is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

**Passive Configuration**

Passive Configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state, and will not switch.

**Table II. Modes of Operation**

| MODE D | MODE C | MODE B | MODE A | Booting Method |
|---|---|---|---|---|
| X | 0 | 0 | 0 | BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1] |
| X | 0 | 1 | 0 | No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations. |
| 0 | 1 | 0 | 0 | BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. IACK has active pull-down. (REQUIRES ADDITIONAL HARDWARE). |
| 0 | 1 | 0 | 1 | IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK has active pull-down.[1] |
| 1 | 1 | 0 | 0 | BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; IACK requires external pull down. (REQUIRES ADDITIONAL HARDWARE) |
| 1 | 1 | 0 | 1 | IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. IACK requires external pull-down.[1] |

NOTE
[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

**Active Configuration**
Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

**$\overline{\text{IACK}}$ Configuration**
Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire OR'd."

Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire OR'd" together.

**MEMORY ARCHITECTURE**
The ADSP-2186M provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the ADSP-2186M.

**Program Memory**
**Program Memory (Full Memory Mode)** is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2186M has 8K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus.

**Program Memory (Host Mode)** allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16 bits wide only.

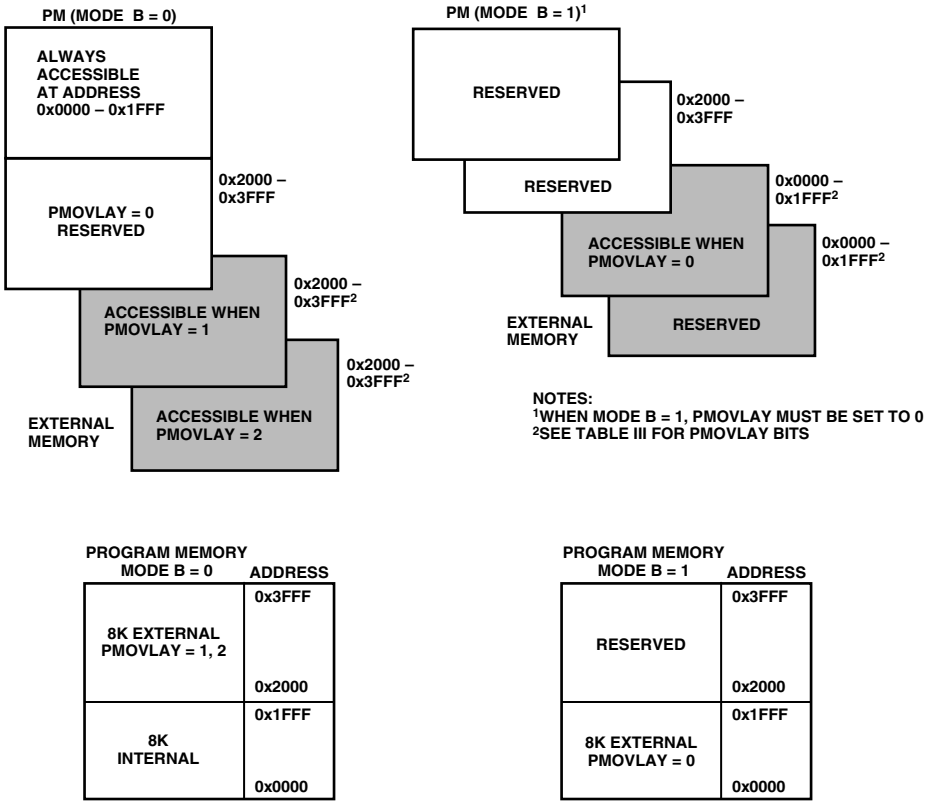



*Figure 4. Program Memory*

**Table III. PMOVLAY Bits**

| PMOVLAY | Memory | A13 | A12:0 |
|---|---|---|---|
| 0 | Reserved | Not Applicable | Not Applicable |
| 1 | External Overlay 1 | 0 | 13 LSBs of Address Between 0x2000 and 0x3FFF |
| 2 | External Overlay 2 | 1 | 13 LSBs of Address Between 0x2000 and 0x3FFF |

**Data Memory**

**Data Memory (Full Memory Mode)** is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2186M has 8K words on Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

**Data Memory (Host Mode)** allows access to all internal memory. External overlay access is limited by a single external address line (A0).

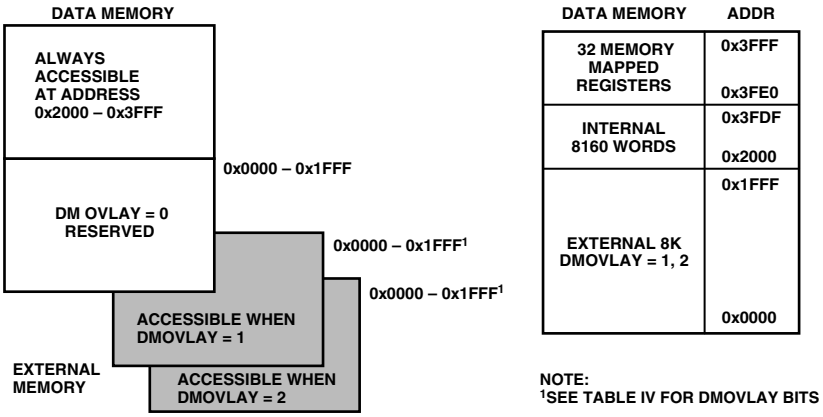



*Figure 5. Data Memory Map*

**Table IV. DMOVLAY Bits**

| DMOVLAY | Memory | A13 | A12:0 |
|---|---|---|---|
| 0 | Reserved | Not Applicable | Not Applicable |
| 1 | External Overlay 1 | 0 | 13 LSBs of Address Between 0x2000 and 0x3FFF |
| 2 | External Overlay 2 | 1 | 13 LSBs of Address Between 0x2000 and 0x3FFF |

**Memory Mapped Registers (New to the ADSP-2186M)**

The ADSP-2186M has three memory mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-2186M's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

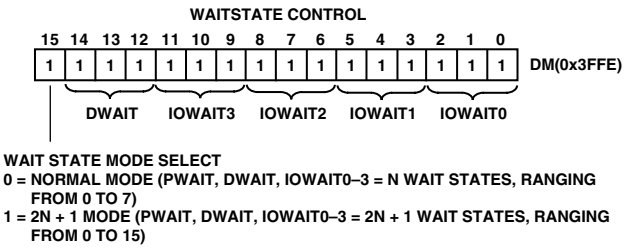



*Figure 6. Wait State Control Register*

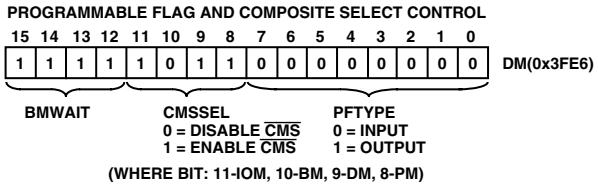



*Figure 7. Programmable Flag and Composite Control Register*

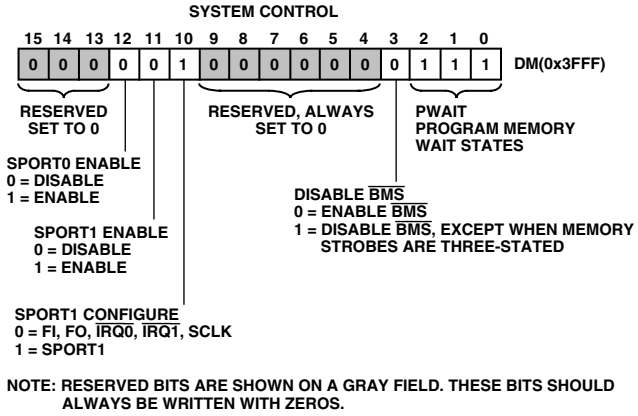



*Figure 8. System Control Register*

**I/O Space (Full Memory Mode)**

The ADSP-2186M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. For ADSP-2186M, set to zero BDMA overlay bits in BDMA control register.

The BMWAIT field, which has four bits on ADSP-2186M, allows selection of up to 15 wait states for BDMA transfers.

**Internal Memory DMA Port (IDMA Port; Host Memory Mode)**

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2186M. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of bits 7:0 represent the IDMA overlay: bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-2186M is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-2186M's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-2186M that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-2186M to write the address onto the IAD0–14 bus into the IDMA Control Register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 31 applies for short reads. When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 32. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.

Refer to the following figures for more information on IDMA and DMA memory maps.

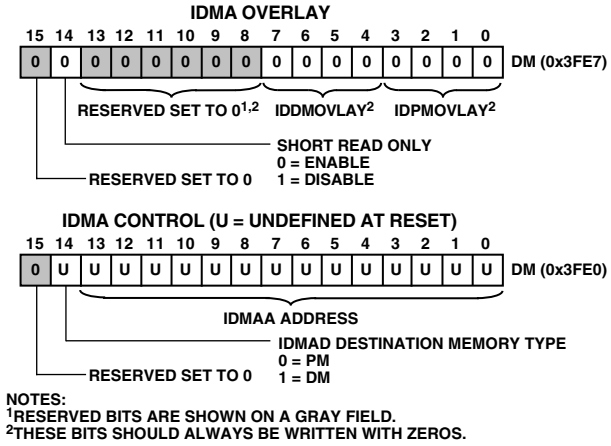
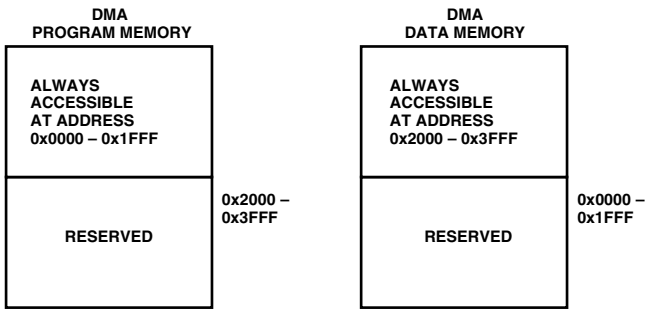



*Figure 10. IDMA Control/OVLAY Registers*




NOTE: IDMA AND BDMA HAVE SEPARATE DMA CONTROL REGISTERS.

*Figure 11. Direct Memory Access—PM and DM Memory Maps*

**Bootstrap Loading (Booting)**

The ADSP-2186M has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the MODE pins specify BDMA booting, the ADSP-2186M initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory.

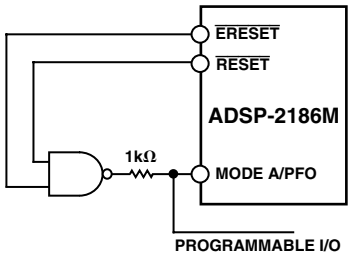



*Figure 12. Mode A Pin/EZ-ICE Circuit*

See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-2186M pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT

These ADSP-2186M pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2186M and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2186M in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

**Target Board Connector for EZ-ICE Probe**
The EZ-ICE connector (a standard pin strip header) is shown in Figure 13. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

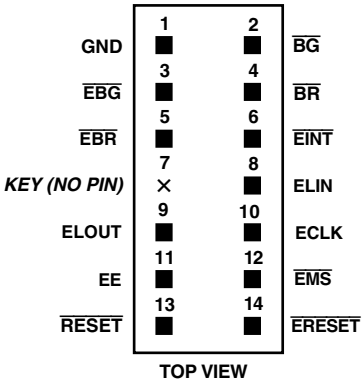



*Figure 13. Target Board Connector for EZ-ICE*

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ- ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

**Target Memory Interface**
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

**PM, DM, BM, IOM, AND CM**
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ- ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst-case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2186M ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

**Target System Interface Signals**
When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ- ICE board's DSP.

# ADSP-2186M–SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

| Parameter | K Grade Min | K Grade Max | B Grade Min | B Grade Max | Unit |
|---|---|---|---|---|---|
| $V_{DDINT}$ | 2.37 | 2.63 | 2.25 | 2.75 | V |
| $V_{DDEXT}$ | 2.37 | 3.6 | 2.25 | 3.6 | V |
| $V_{INPUT}$[1] | $V_{IL}$ = –0.3 | $V_{IH}$ = +3.6 | $V_{IL}$ = –0.3 | $V_{IH}$ = +3.6 | V |
| $T_{AMB}$ | 0 | +70 | –40 | +85 | °C |

NOTES

[1]The ADSP-2186M is 3.3 V tolerant (always accepts up to 3.6 V max $V_{IH}$), but voltage compliance (on outputs, $V_{OH}$) depends on the input $V_{DDEXT}$; because $V_{OH}$ (max) ≈ $V_{DDEXT}$ (max). This applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS

| Parameter | | Test Conditions | K/B Grades Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Hi-Level Input Voltage[1, 2] | @ $V_{DDINT}$ = max | 1.5 | | | V |
| $V_{IH}$ | Hi-Level CLKIN Voltage | @ $V_{DDINT}$ = max | 2.0 | | | V |
| $V_{IL}$ | Lo-Level Input Voltage[1, 3] | @ $V_{DDINT}$ = min | | | 0.7 | V |
| $V_{OH}$ | Hi-Level Output Voltage[1, 4, 5] | @ $V_{DDEXT}$ = min, $I_{OH}$ = –0.5 mA | 2.0 | | | V |
| | | @ $V_{DDEXT}$ = 3.0 V, $I_{OH}$ = –0.5 mA | 2.4 | | | V |
| | | @ $V_{DDEXT}$ = min, $I_{OH}$ = –100 µA[6] | $V_{DDEXT}$ – 0.3 | | | V |
| $V_{OL}$ | Lo-Level Output Voltage[1, 4, 5] | @ $V_{DDEXT}$ = min, $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_{IH}$ | Hi-Level Input Current[3] | @ $V_{DDINT}$ = max, $V_{IN}$ = 3.6 V | | | 10 | µA |
| $I_{IL}$ | Lo-Level Input Current[3] | @ $V_{DDINT}$ = max, $V_{IN}$ = 0 V | | | 10 | µA |
| $I_{OZH}$ | Three-State Leakage Current[7] | @ $V_{DDEXT}$ = max, $V_{IN}$ = 3.6 V[8] | | | 10 | µA |
| $I_{OZL}$ | Three-State Leakage Current[7] | @ $V_{DDEXT}$ = max, $V_{IN}$ = 0 V[8] | | | 10 | µA |
| $I_{DD}$ | Supply Current (Idle)[9] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 15 ns | | 9 | | mA |
| $I_{DD}$ | Supply Current (Idle)[9] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 13.3 ns | | 10 | | mA |
| $I_{DD}$ | Supply Current (Dynamic)[10] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 15 ns[11], $T_{AMB}$ = 25°C | | 35 | | mA |
| $I_{DD}$ | Supply Current (Dynamic)[10] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 13.3 ns[11], $T_{AMB}$ = 25°C | | 38 | | mA |
| $I_{DD}$ | Supply Current (Power-Down)[12] | @ $V_{DDINT}$ = 2.5, $T_{AMB}$ = 25°C in Lowest Power Mode | | 100 | | µA |
| $C_I$ | Input Pin Capacitance[3, 6] | @ $V_{IN}$ = 2.5 V, $f_{IN}$ = 1.0 MHz, $T_{AMB}$ = 25°C | | | 8 | pF |
| $C_O$ | Output Pin Capacitance[6, 7, 12, 13] | @ $V_{IN}$ = 2.5 V, $f_{IN}$ = 1.0 MHz, $T_{AMB}$ = 25°C | | | 8 | pF |

NOTES

[1] Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2] Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5] Although specified for TTL outputs, all ADSP-2186M outputs are CMOS-compatible and will drive to $V_{DDEXT}$ and GND, assuming no dc loads.

[6] Guaranteed but not tested.

[7] Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8] 0 V on $\overline{\text{BR}}$.

[9] Idle refers to ADSP-2186M state of operation during execution of IDLE instruction. Deasserted pins are driven to either $V_{DD}$ or GND.

[10] $I_{DD}$ measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[11] $V_{IN}$ = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12] See Chapter 9 of the *ADSP-2100 Family User's Manual* for details.

[13] Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Memory Write** | | | | |
| *Switching Characteristics:* | | | | |
| $t_{DW}$ | Data Setup before $\overline{WR}$ High | $0.5t_{CK} - 4 + w$ | | ns |
| $t_{DH}$ | Data Hold after $\overline{WR}$ High | $0.25t_{CK} - 1$ | | ns |
| $t_{WP}$ | $\overline{WR}$ Pulsewidth | $0.5t_{CK} - 3 + w$ | | ns |
| $t_{WDE}$ | $\overline{WR}$ Low to Data Enabled | 0 | | ns |
| $t_{ASW}$ | A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low | $0.25t_{CK} - 3$ | | ns |
| $t_{DDR}$ | Data Disable before $\overline{WR}$ or $\overline{RD}$ Low | $0.25t_{CK} - 3$ | | ns |
| $t_{CWR}$ | CLKOUT High to $\overline{WR}$ Low | $0.25t_{CK} - 2$ | $0.25\ t_{CK} + 4$ | ns |
| $t_{AW}$ | A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted | $0.75t_{CK} - 5 + w$ | | ns |
| $t_{WRA}$ | A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted | $0.25t_{CK} - 1$ | | ns |
| $t_{WWR}$ | $\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low | $0.5t_{CK} - 3$ | | ns |

NOTES
w = wait states × $t_{CK}$.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

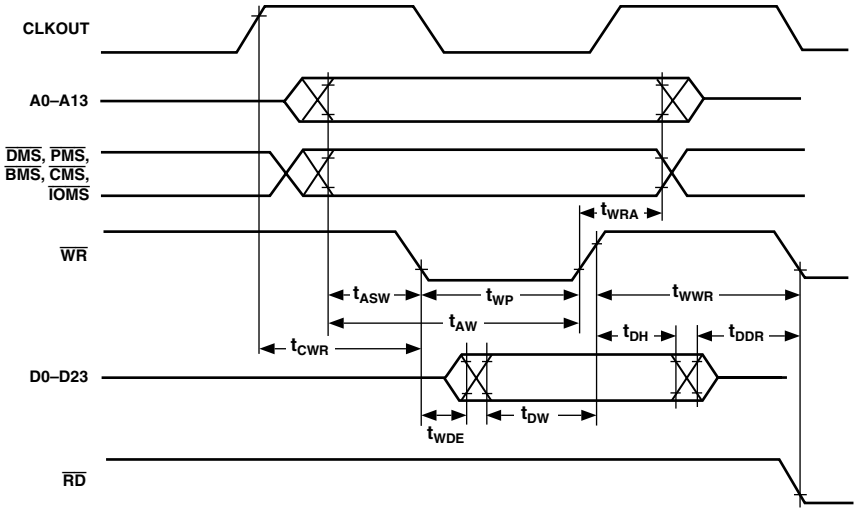



*Figure 25. Memory Write*

**Serial Ports**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Serial Ports** | | | | |
| *Timing Requirements:* | | | | |
| $t_{SCK}$ | SCLK Period | 26.6 | | ns |
| $t_{SCS}$ | DR/TFS/RFS Setup before SCLK Low | 4 | | ns |
| $t_{SCH}$ | DR/TFS/RFS Hold after SCLK Low | 7 | | ns |
| $t_{SCP}$ | SCLKIN Width | 12 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{CC}$ | CLKOUT High to SCLKOUT | $0.25t_{CK}$ | $0.25t_{CK}$ + 6 | ns |
| $t_{SCDE}$ | SCLK High to DT Enable | 0 | | ns |
| $t_{SCDV}$ | SCLK High to DT Valid | | 12 | ns |
| $t_{RH}$ | $TFS/RFS_{OUT}$ Hold after SCLK High | 0 | | ns |
| $t_{RD}$ | $TFS/RFS_{OUT}$ Delay from SCLK High | | 12 | ns |
| $t_{SCDH}$ | DT Hold after SCLK High | 0 | | ns |
| $t_{TDE}$ | TFS (Alt) to DT Enable | 0 | | ns |
| $t_{TDV}$ | TFS (Alt) to DT Valid | | 12 | ns |
| $t_{SCDD}$ | SCLK High to DT Disable | | 12 | ns |
| $t_{RDV}$ | RFS (Multichannel, Frame Delay Zero) to DT Valid | | 12 | ns |

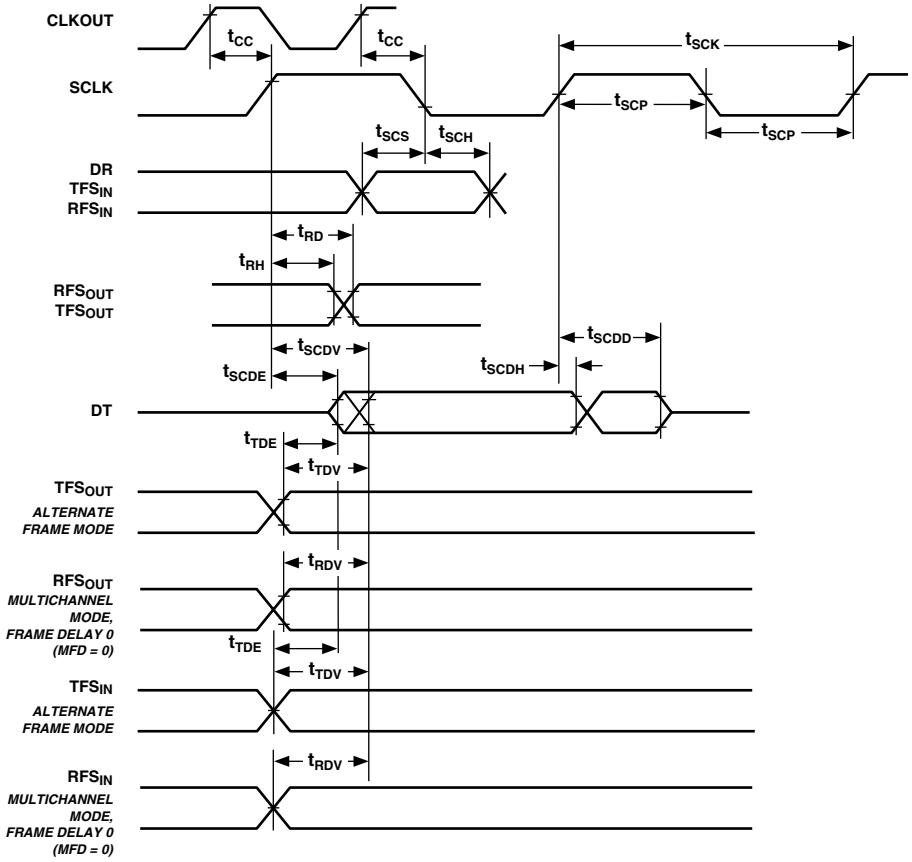



*Figure 26. Serial Ports*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Read, Short Read Cycle**[1, 2] | | | | |
| *Timing Requirements:* | | | | |
| $t_{IKR}$ | $\overline{IACK}$ Low before Start of Read[3] | 0 | | ns |
| $t_{IRP1}$ | Duration of Read (DM/PM1)[4] | 10 | $2t_{CK} - 5$ | ns |
| $t_{IRP2}$ | Duration of Read (PM2)[5] | 10 | $t_{CK} - 5$ | ns |
| *Switching Characteristics*: | | | | |
| $t_{IKHR}$ | $\overline{IACK}$ High after Start of Read[3] | | 10 | ns |
| $t_{IKDH}$ | IAD15–0 Data Hold after End of Read[6] | 0 | | ns |
| $t_{IKDD}$ | IAD15–0 Data Disabled after End of Read[6] | | 10 | ns |
| $t_{IRDE}$ | IAD15–0 Previous Data Enabled after Start of Read | 0 | | ns |
| $t_{IRDV}$ | IAD15–0 Previous Data Valid after Start of Read | | 10 | ns |

NOTES
[1]Short Read Only must be disabled in the IDMA Overlay memory mapped register.
[2]Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.
[3]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[4]DM Read or first half of PM Read.
[5]Second half of PM Read.
[6]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

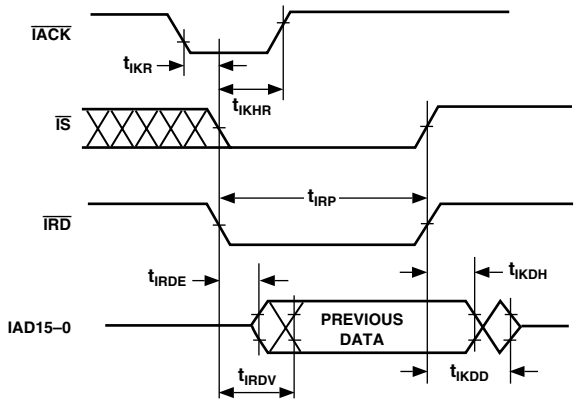



*Figure 31. IDMA Read, Short Read Cycle*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Read, Short Read Cycle in Short Read Only Mode**[1] | | | | |
| *Timing Requirements:* | | | | |
| $t_{IKR}$ | $\overline{IACK}$ Low before Start of Read[2] | 0 | | ns |
| $t_{IRP}$ | Duration of Read[3] | 10 | | ns |
| *Switching Characteristics:* | | | | |
| $t_{IKHR}$ | $\overline{IACK}$ High after Start of Read[2] | | 10 | ns |
| $t_{IKDH}$ | IAD15–0 Previous Data Hold after End of Read[3] | 0 | | ns |
| $t_{IKDD}$ | IAD15–0 Previous Data Disabled after End of Read[3] | | 10 | ns |
| $t_{IRDE}$ | IAD15–0 Previous Data Enabled after Start of Read | 0 | | ns |
| $t_{IRDV}$ | IAD15–0 Previous Data Valid after Start of Read | | 10 | ns |

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

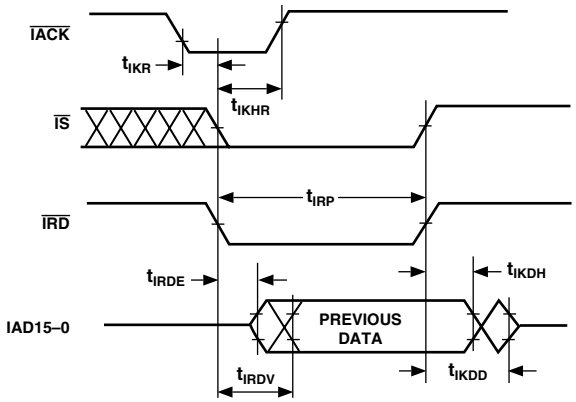
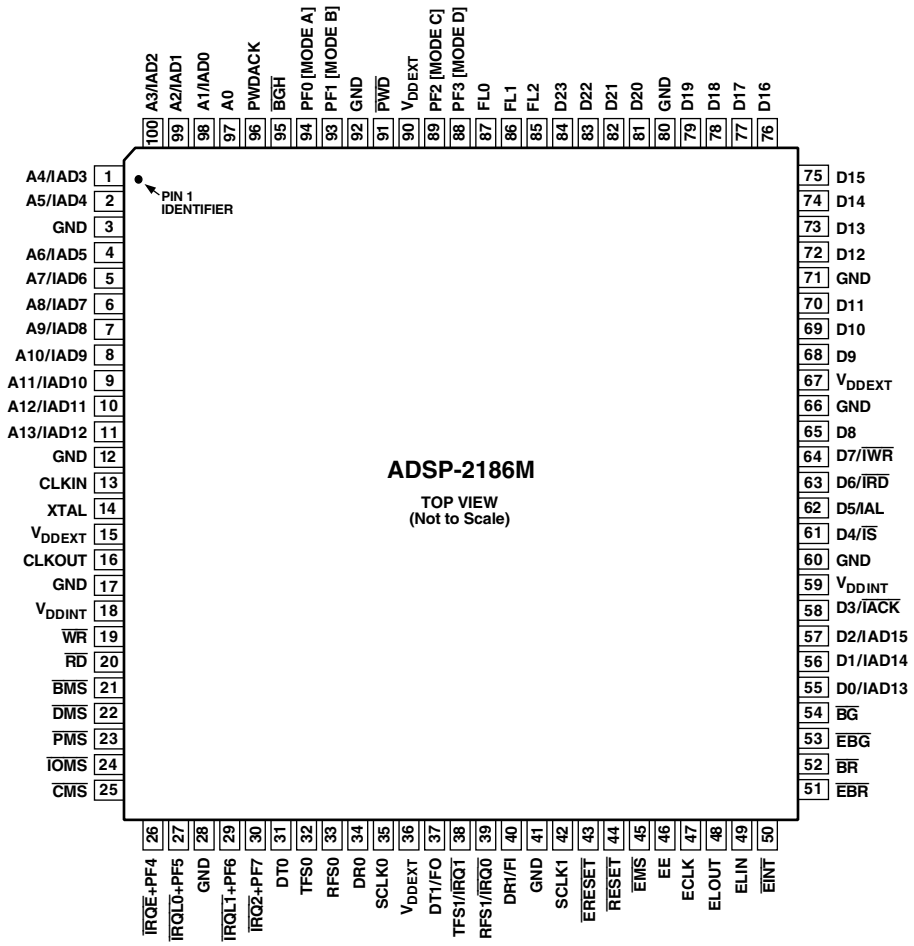



*Figure 32. IDMA Read, Short Read Only Cycle*

**100-LEAD LQFP PIN CONFIGURATION**



The LQFP package pinout is shown in the table below. Pin names in bold text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of RESET.

The multiplexed pins DT1/FO, TFS1/IRQ1, RFS1/IRQ0, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

**LQFP Package Pinout**

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | A4/**IAD3** | 26 | IRQE + PF4 | 51 | EBR | 76 | D16 |
| 2 | A5/**IAD4** | 27 | IRQL0 + PF5 | 52 | BR | 77 | D17 |
| 3 | GND | 28 | GND | 53 | EBG | 78 | D18 |
| 4 | A6/**IAD5** | 29 | IRQL1 + PF6 | 54 | BG | 79 | D19 |
| 5 | A7/**IAD6** | 30 | IRQ2 + PF7 | 55 | D0/**IAD13** | 80 | GND |
| 6 | A8/**IAD7** | 31 | DT0 | 56 | D1/**IAD14** | 81 | D20 |
| 7 | A9/**IAD8** | 32 | TFS0 | 57 | D2/**IAD15** | 82 | D21 |
| 8 | A10/**IAD9** | 33 | RFS0 | 58 | D3/**IACK** | 83 | D22 |
| 9 | A11/**IAD10** | 34 | DR0 | 59 | $V_{DDINT}$ | 84 | D23 |
| 10 | A12/**IAD11** | 35 | SCLK0 | 60 | GND | 85 | FL2 |
| 11 | A13/**IAD12** | 36 | $V_{DDEXT}$ | 61 | D4/**IS** | 86 | FL1 |
| 12 | GND | 37 | DT1/FO | 62 | D5/**IAL** | 87 | FL0 |
| 13 | CLKIN | 38 | TFS1/IRQ1 | 63 | D6/**IRD** | 88 | PF3 [MODE D] |
| 14 | XTAL | 39 | RFS1/IRQ0 | 64 | D7/**IWR** | 89 | PF2 [MODE C] |
| 15 | $V_{DDEXT}$ | 40 | DR1/FI | 65 | D8 | 90 | $V_{DDEXT}$ |
| 16 | CLKOUT | 41 | GND | 66 | GND | 91 | PWD |
| 17 | GND | 42 | SCLK1 | 67 | $V_{DDEXT}$ | 92 | GND |
| 18 | $V_{DDINT}$ | 43 | ERESET | 68 | D9 | 93 | PF1 [MODE B] |
| 19 | WR | 44 | RESET | 69 | D10 | 94 | PF0 [MODE A] |
| 20 | RD | 45 | EMS | 70 | D11 | 95 | BGH |
| 21 | BMS | 46 | EE | 71 | GND | 96 | PWDACK |
| 22 | DMS | 47 | ECLK | 72 | D12 | 97 | A0 |
| 23 | PMS | 48 | ELOUT | 73 | D13 | 98 | A1/**IAD0** |
| 24 | IOMS | 49 | ELIN | 74 | D14 | 99 | A2/**IAD1** |
| 25 | CMS | 50 | EINT | 75 | D15 | 100 | A3/**IAD2** |

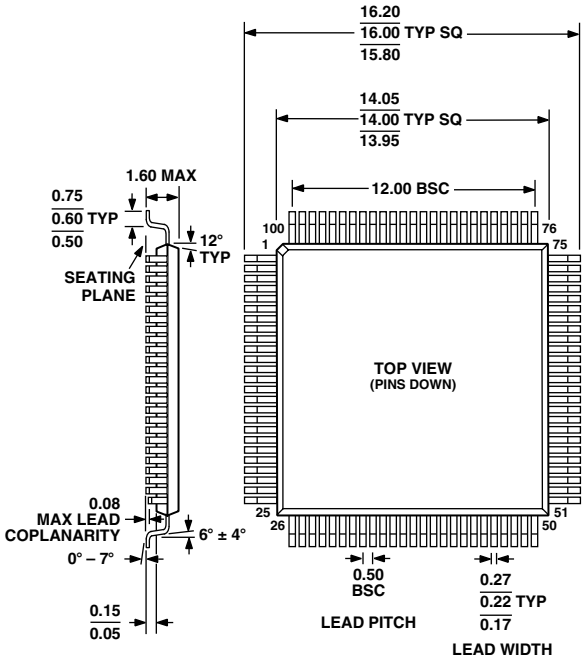
**144-Ball Mini-BGA Package Pinout (Bottom View)**

| 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GND | GND | D22 | NC | NC | NC | GND | NC | A0 | GND | A1/IAD0 | A2/IAD1 | A |
| D16 | D17 | D18 | D20 | D23 | $V_{DDEXT}$ | GND | NC | NC | GND | A3/IAD2 | A4/IAD3 | B |
| D14 | NC | D15 | D19 | D21 | $V_{DDEXT}$ | $\overline{PWD}$ | A7/IAD6 | A5/IAD4 | $\overline{RD}$ | A6/IAD5 | PWDACK | C |
| GND | NC | D12 | D13 | NC | PF2 [MODE C] | PF1 [MODE B] | A9/IAD8 | $\overline{BGH}$ | NC | $\overline{WR}$ | NC | D |
| D10 | GND | $V_{DDEXT}$ | GND | GND | PF3 [MODE D] | FL2 | PF0 [MODE A] | FL0 | A8/IAD7 | $V_{DDEXT}$ | $V_{DDEXT}$ | E |
| D9 | NC | D8 | D11 | D7/$\overline{IWR}$ | NC | NC | FL1 | A11/IAD10 | A12/IAD11 | NC | A13/IAD12 | F |
| D4/$\overline{IS}$ | NC | NC | D5/IAL | D6/$\overline{IRD}$ | NC | NC | NC | A10/IAD9 | GND | NC | XTAL | G |
| GND | NC | GND | D3/$\overline{IACK}$ | D2/IAD15 | TFS0 | DT0 | $V_{DDINT}$ | GND | GND | GND | CLKIN | H |
| $V_{DDINT}$ | $V_{DDINT}$ | D1/IAD14 | $\overline{BG}$ | RFS1/$\overline{IRQ0}$ | D0/IAD13 | SCLK0 | $V_{DDEXT}$ | $V_{DDEXT}$ | NC | $V_{DDINT}$ | CLKOUT | J |
| $\overline{EBG}$ | $\overline{BR}$ | $\overline{EBR}$ | $\overline{ERESET}$ | SCLK1 | TFS1/$\overline{IRQ1}$ | RFS0 | $\overline{DMS}$ | $\overline{BMS}$ | NC | NC | NC | K |
| $\overline{EINT}$ | ELOUT | ELIN | $\overline{RESET}$ | GND | DR0 | $\overline{PMS}$ | GND | $\overline{IOMS}$ | $\overline{IRQL1}$ + PF6 | NC | $\overline{IRQE}$ + PF4 | L |
| ECLK | EE | $\overline{EMS}$ | NC | GND | DR1/FI | DT1/FO | GND | $\overline{CMS}$ | NC | $\overline{IRQ2}$ + PF7 | $\overline{IRQL0}$ + PF5 | M |

## OUTLINE DIMENSIONS

Dimensions shown in millimeters.

### 100-Lead Metric Thin Plastic Quad Flatpack (LQFP) (ST-100)

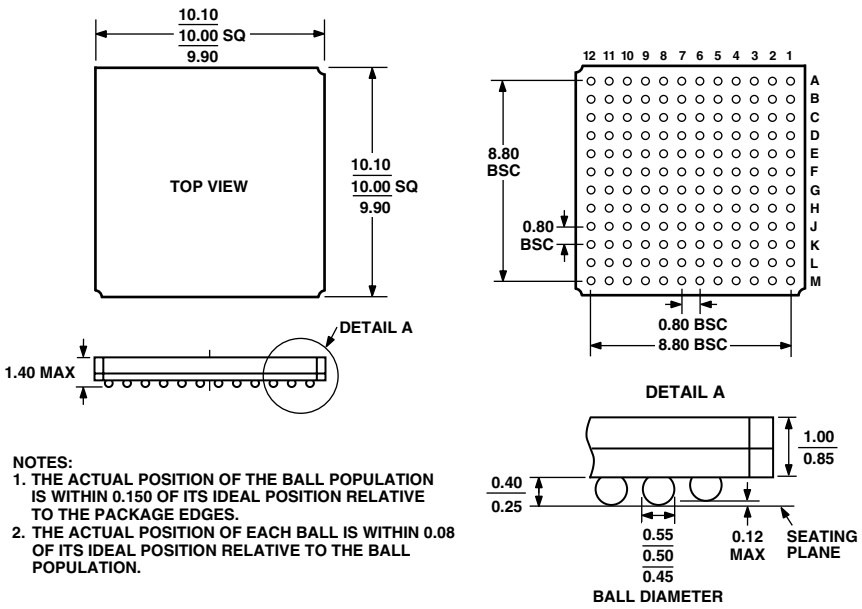



NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

## OUTLINE DIMENSIONS

Dimensions shown in millimeters.

### 144-Ball Mini-BGA
### (CA-144)




NOTES:
1. THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.150 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

## ORDERING GUIDE

| Part Number | Ambient Temperature Range | Instruction Rate | Package Description* | Package Option |
|---|---|---|---|---|
| ADSP-2186MKST-300 | 0°C to 70°C | 75 | 100-Lead LQFP | ST-100 |
| ADSP-2186MBST-266 | –40°C to +85°C | 66 | 100-Lead LQFP | ST-100 |
| ADSP-2186MKCA-300 | 0°C to 70°C | 75 | 144-Ball Mini-BGA | CA-144 |
| ADSP-2186MBCA-266 | –40°C to +85°C | 66 | 144-Ball Mini-BGA | CA-144 |

*In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously labeled TQFP packages (1.6 mm thick) are now designated as LQFP.

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