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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	75MHz
Non-Volatile Memory	External
On-Chip RAM	40kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2186mkstz-300

- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board
- EE-146: Implementing a Boot Manager for ADSP-218x Family DSPs
- EE-152: Using Software Overlays with the ADSP-219x and VisualDSP 2.0++
- EE-153: ADSP-2191 Programmable PLL
- EE-154: ADSP-2191 Host Port Interface
- EE-156: Support for the H.100 protocol on the ADSP-2191
- EE-158: ADSP-2181 EZ-Kit Lite IDMA to PC Printer Port Interface
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-164: Advanced EPROM Boot and No-boot Scenarios with ADSP-219x DSPs
- EE-168: Using Third Overtone Crystals with the ADSP-218x DSP
- EE-17: ADSP-2187L Memory Organization
- EE-18: Choosing and Using FFTs for ADSP-21xx
- EE-188: Using C To Implement Interrupt-Driven Systems On ADSP-219x DSPs
- EE-2: Using ADSP-218x I/O Space
- EE-226: ADSP-2191 DSP Host Port Booting
- EE-227: CAN Configuration Procedure for ADSP-21992 DSPs
- EE-249: Implementing Software Overlays on ADSP-218x DSPs with VisualDSP++®
- EE-32: Language Extensions: Memory Storage Types, ASM & Inline Constructs
- EE-33: Programming The ADSP-21xx Timer In C
- EE-35: Troubleshooting your ADSP-218x EZ-ICE
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-36: ADSP-21xx Interface to the IOM-2 bus
- EE-38: ADSP-2181 IDMA Port - Cycle Steal Timing
- EE-39: Interfacing 5V Flash Memory to an ADSP-218x (Byte Programming Algorithm)
- EE-48: Converting Legacy 21xx Systems To A 218x System Design
- EE-5: ADSP-218x Full Memory Mode vs. Host Memory Mode
- EE-60: Simulating an RS-232 UART Using the Synchronous Serial Ports on the ADSP-21xx Family DSPs
- EE-64: Setting Mode Pins on Reset
- EE-68: Analog Devices JTAG Emulation Technical Reference
- EE-71: Minimum Rise Time Specs for Critical Interrupt and Clock Signals on the ADSP-21x1/21x5
- EE-74: Analog Devices Serial Port Development and Troubleshooting Guide
- EE-78: BDMA Usage on 100 pin ADSP-218x DSPs Configured for IDMA Use
- EE-79: EPROM Booting In Host Mode with 100 Pin 218x Processors
- EE-82: Using an ADSP-2181 DSP's IO Space to IDMA Boot Another ADSP-2181
- EE-89: Implementing A Software UART on the ADSP-2181 EZ-Kit-Lite
- EE-90: Using the 21xx C-FFT Library
- EE-96: Interfacing Two AD73311 Codecs to the ADSP-218x

Data Sheet

- ADSP-2186M: 16-Bit, 75 MIPS, 2.5V, 2 Serial Ports, Host Port, 40 KB RAM Data Sheet

Evaluation Kit Manuals

- ADSP-218x DSP family and ADSP-2192 EZ-KIT Lite® Installation Procedure -Non-USB

Integrated Circuit Anomalies

- ADSP-2186M Anomaly List for Revision 2.0

Processor Manuals

- ADSP 21xx Processors: Manuals
- ADSP-218x DSP Hardware Reference
- ADSP-218x DSP Instruction Set Reference
- Using the ADSP-2100 Family Volume 1
- Using the ADSP-2100 Family Volume 2

Software Manuals

- VisualDSP++ 3.5 Assembler and Preprocessor Manual for ADSP-218x and ADSP-219x DSPs
- VisualDSP++ 3.5 C Compiler and Library Manual for ADSP-218x DSPs
- VisualDSP++ 3.5 C/C++ Compiler and Library Manual for ADSP-219x Processors
- VisualDSP++ 3.5 Component Software Engineering User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Getting Started Guide for 16-Bit Processors
- VisualDSP++ 3.5 Kernel VDK User's Guide for 16-Bit Processors
- VisualDSP++ 3.5 Linker and Utilities Manual for 16-Bit Processors
- VisualDSP++ 3.5 Loader Manual for 16-Bit Processors
- VisualDSP++ 3.5 User's Guide for 16-Bit Processors

SOFTWARE AND SYSTEMS REQUIREMENTS

- Software and Tools Anomalies Search

TOOLS AND SIMULATIONS

- ADSP-218xM IBIS Datafile (LQFP Package)

DESIGN RESOURCES

- ADSP-2186M Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADSP-2186M EngineerZone Discussions.

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Terminating Unused Pins
The following table shows the recommendations for terminating unused pins.

Pin Terminations

Pin Name	I/O 3-State (Z)	Reset State	Hi-Z* Caused By	Unused Configuration
XTAL	I	I		Float
CLKOUT	O	O		Float
A13:1 or	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD12:0	I/O (Z)	Hi-Z	$\overline{IS}$	Float
A0	O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23:8	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IWR}$	I	I		High (Inactive)
D6 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IRD}$	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or	I/O (Z)	Hi-Z		Float
IAL	I	I		Low (Inactive)
D4 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IS}$	I	I		High (Inactive)
D3 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IACK}$				Float
D2:0 or	I/O (Z)	Hi-Z	$\overline{BR}$, $\overline{EBR}$	Float
IAD15:13	I/O (Z)	Hi-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}$/*PF7*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL1}$/*PF6*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQL0}$/*PF5*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
$\overline{IRQE}$/*PF4*	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/$\overline{IRQ0}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/$\overline{IRQ1}$	I/O	I		High or Low
DT1/FO	O	O		Float
$\overline{EE}$	I	I		Float
$\overline{EBR}$	I	I		Float
$\overline{EBG}$	O	O		Float
$\overline{ERESET}$	I	I		Float
$\overline{EMS}$	O	O		Float
$\overline{EINT}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

NOTES
*Hi-Z = High Impedance.
1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1, prior to enabling interrupts, and let pins float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, $\overline{RESET}$, and PF3:0/MODE D:A are not included in the table because these pins must be used.

Interrupts

The interrupt controller allows the processor to respond to the 11 possible interrupts and reset with minimum overhead. The ADSP-2186M provides four dedicated external interrupt input pins: $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, and $\overline{IRQE}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI and FO, for a total of six external interrupts. The ADSP-2186M also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power- down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$, and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

Table I. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
Reset (or Power-Up with PUCR = 1)	0000 (Highest Priority)
Power-Down (Nonmaskable)	002C
$\overline{IRQ2}$	0004
$\overline{IRQL1}$	0008
$\overline{IRQL0}$	000C
SPORT0 Transmit	0010
SPORT0 Receive	0014
$\overline{IRQE}$	0018
BDMA Interrupt	001C
SPORT1 Transmit or $\overline{IRQ1}$	0020
SPORT1 Receive or $\overline{IRQ0}$	0024
Timer	0028 (Lowest Priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2186M masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ external interrupts to be either edge- or level-sensitive. The $\overline{IRQE}$ pin is an external edge sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2186M has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

The ADSP-2186M processor has a low power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{PWD}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{RESET}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

Idle

When the ADSP-2186M is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA and autobuffer cycle steals still occur.

Active Configuration
Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

$\overline{\text{IACK}}$ Configuration
Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire OR'd."

Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire OR'd" together.

MEMORY ARCHITECTURE
The ADSP-2186M provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to the following figures and tables for PM and DM memory allocations in the ADSP-2186M.

Program Memory
Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2186M has 8K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16 bits wide only.

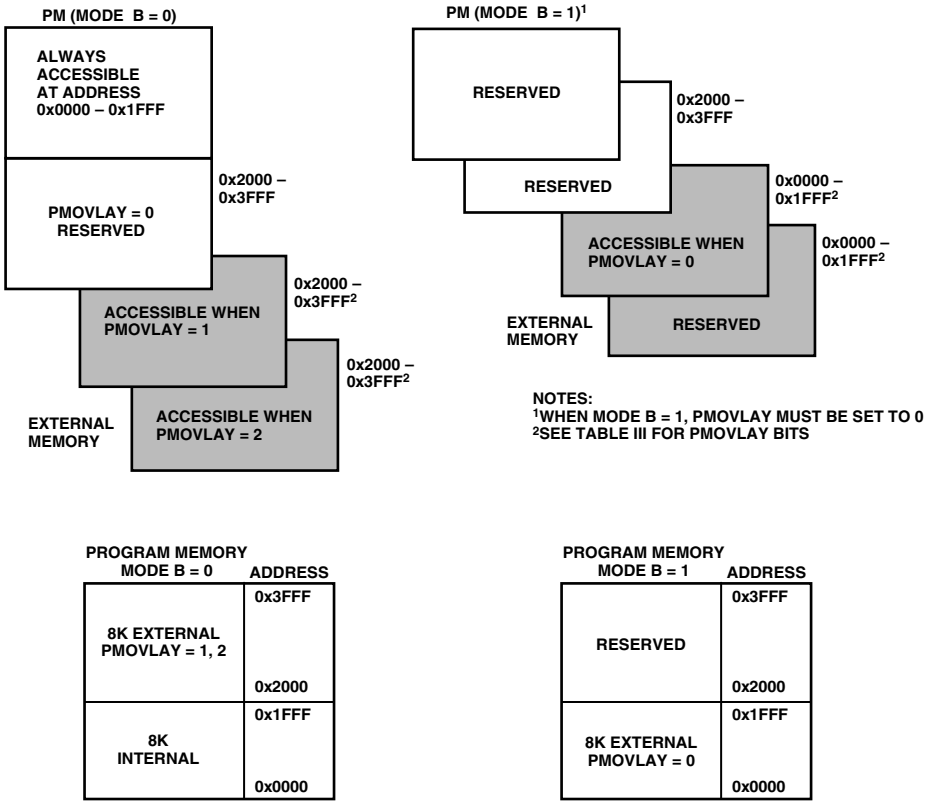


Figure 4. Program Memory

Table III. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0	Reserved	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2186M has 8K words on Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

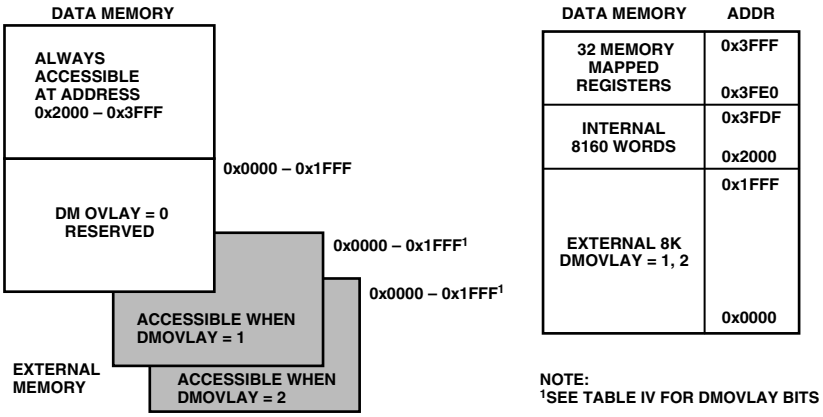


Figure 5. Data Memory Map

Table IV. DMOVLAY Bits

DMOVLAY	Memory	A13	A12:0
0	Reserved	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Memory Mapped Registers (New to the ADSP-2186M)

The ADSP-2186M has three memory mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-2186M's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

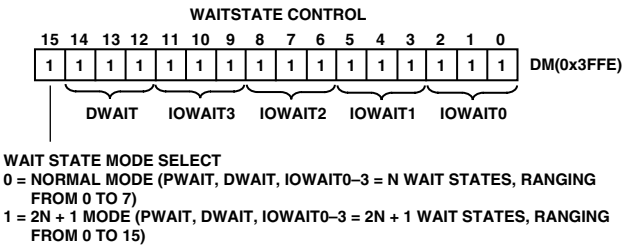


Figure 6. Wait State Control Register

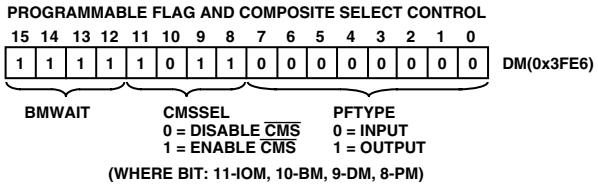


Figure 7. Programmable Flag and Composite Control Register

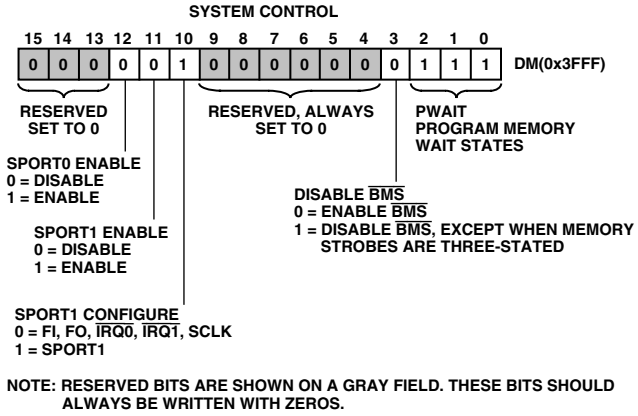


Figure 8. System Control Register

I/O Space (Full Memory Mode)

The ADSP-2186M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

Table V. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0 and Wait State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)
The ADSP-2186M has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)
The ADSP-2186M's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Byte Memory
The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2186M supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register and the wait state mode bit.

Byte Memory DMA (BDMA, Full Memory Mode)
The byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

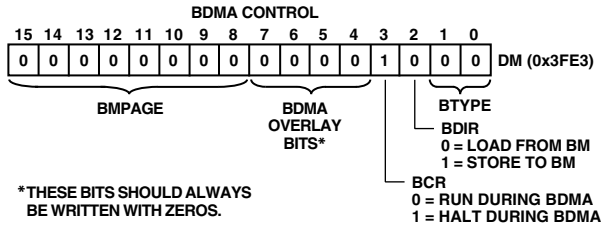


Figure 9. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table VI shows the data formats supported by the BDMA circuit.

Table VI. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. For ADSP-2186M, set to zero BDMA overlay bits in BDMA control register.

The BMWAIT field, which has four bits on ADSP-2186M, allows selection of up to 15 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2186M. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is described as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the value of bits 7:0 represent the IDMA overlay: bits 14:8 must be set to 0. If Bit 15 = 0, the value of Bits 13:0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-2186M is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-2186M's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-2186M that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-2186M to write the address onto the IAD0–14 bus into the IDMA Control Register. If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, shown below, is memory mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. When Bit 14 in 0x3FE7 is set to 1, timing in Figure 31 applies for short reads. When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in Figure 32. For ADSP-2186M, IDDMOVLAY and IDPMOVLAY bits in IDMA overlay register should be set to zero.

Refer to the following figures for more information on IDMA and DMA memory maps.

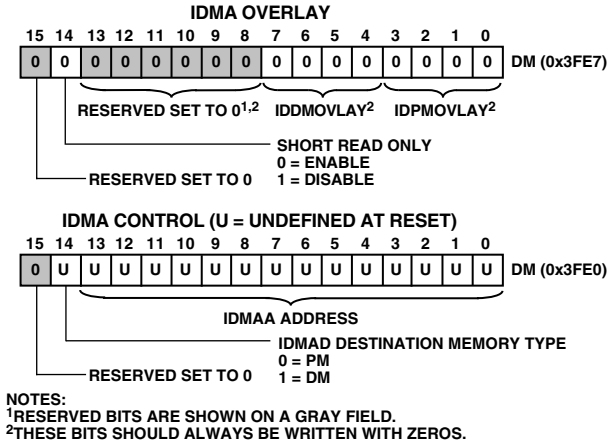
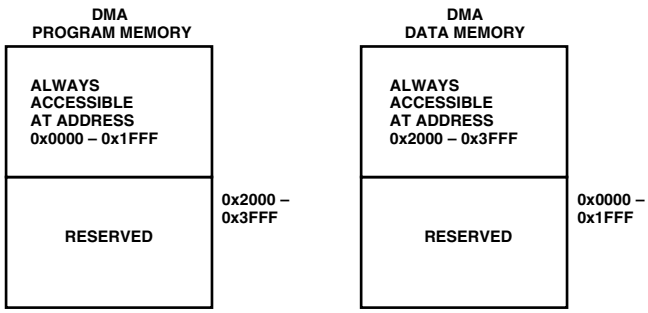


Figure 10. IDMA Control/OVLAY Registers



NOTE: IDMA AND BDMA HAVE SEPARATE DMA CONTROL REGISTERS.

Figure 11. Direct Memory Access—PM and DM Memory Maps

Bootstrap Loading (Booting)

The ADSP-2186M has two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, B, and C configuration bits.

When the MODE pins specify BDMA booting, the ADSP-2186M initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory.

ADSP-2186M–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DDINT}	2.37	2.63	2.25	2.75	V
V_{DDEXT}	2.37	3.6	2.25	3.6	V
V_{INPUT}[1]	V_{IL} = –0.3	V_{IH} = +3.6	V_{IL} = –0.3	V_{IH} = +3.6	V
T_{AMB}	0	+70	–40	+85	°C

NOTES

[1]The ADSP-2186M is 3.3 V tolerant (always accepts up to 3.6 V max V_{IH}), but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}; because V_{OH} (max) ≈ V_{DDEXT} (max). This applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	Typ	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DDINT} = max	2.0			V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.7	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.0			V
		@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
		@ V_{DDEXT} = min, I_{OH} = –100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDEXT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 2.5, t_{CK} = 15 ns		9		mA
I_{DD}	Supply Current (Idle)[9]	@ V_{DDINT} = 2.5, t_{CK} = 13.3 ns		10		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.5, t_{CK} = 15 ns[11], T_{AMB} = 25°C		35		mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.5, t_{CK} = 13.3 ns[11], T_{AMB} = 25°C		38		mA
I_{DD}	Supply Current (Power-Down)[12]	@ V_{DDINT} = 2.5, T_{AMB} = 25°C in Lowest Power Mode		100		µA
C_I	Input Pin Capacitance[3, 6]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF
C_O	Output Pin Capacitance[6, 7, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C			8	pF

NOTES

[1] Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2] Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3] Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5] Although specified for TTL outputs, all ADSP-2186M outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.

[6] Guaranteed but not tested.

[7] Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8] 0 V on $\overline{\text{BR}}$.

[9] Idle refers to ADSP-2186M state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10] I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[11] V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12] See Chapter 9 of the *ADSP-2100 Family User's Manual* for details.

[13] Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

FREQUENCY DEPENDENCY FOR TIMING SPECIFICATIONS

t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2186M uses an input clock with a frequency equal to half the instruction rate. For example, a 37.50 MHz input clock (which is equivalent to 26.6 ns) yields a 13.3 ns processor cycle (equivalent to 75 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain the specification value.

Example: t_{CKH} = 0.5 t_{CK} – 2 ns = 0.5 (15 ns) – 2 ns = 5.5 ns

ENVIRONMENTAL CONDITIONS[1]

Rating Description	Symbol	LQFP	Mini-BGA
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48°C/W	63.3°C/W
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50°C/W	70.7°C/W
Thermal Resistance (Junction-to-Case)	θ_{JC}	2°C/W	7.4°C/W

NOTE
[1]Where the Ambient Temperature Rating (T_{AMB}) is:
$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DDEXT} = 3.3 V and t_{CK} = 30 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DDEXT}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 15).

$(C \times V_{DDEXT}^2 \times f)$ is calculated for each output:

Parameters	# of Pins	× C pF	× V_{DDEXT}^2 V	× f MHz	PD mW
Address	7	10	3.3^2	16.67	12.7
Data Output, $\overline{WR}$	9	10	3.3^2	16.67	16.3
$\overline{RD}$	1	10	3.3^2	16.67	1.8
CLKOUT, $\overline{DMS}$	2	10	3.3^2	33.3	7.2
					38.0

Total power dissipation for this example is P_{INT} + 38.0 mW.

Output Drive Currents

Figure 14 shows typical I-V characteristics for the output drivers on the ADSP-2186M. The curves represent the current drive capability of the output drivers as a function of output voltage.

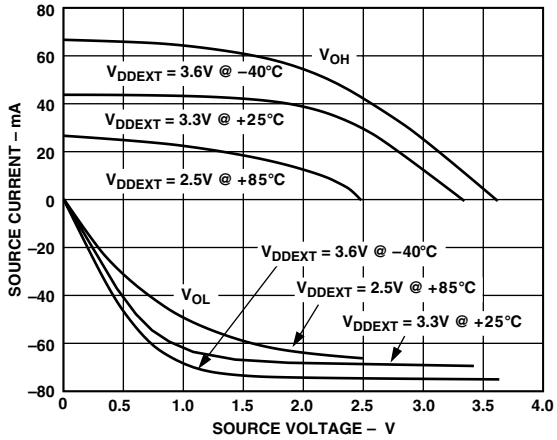


Figure 14. Typical Output Driver Characteristics

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

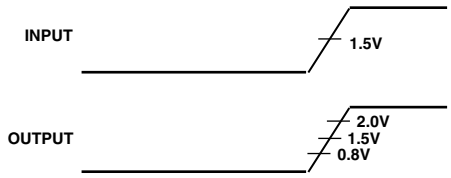


Figure 18. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown Figure 19. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

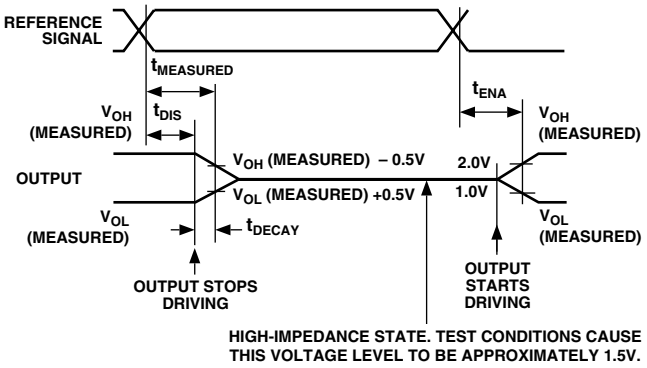


Figure 19. Output Enable/Disable

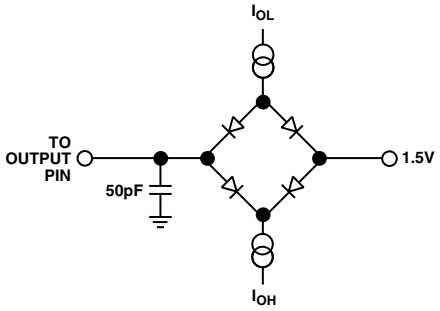


Figure 20. Equivalent Loading for AC Measurements (Including All Fixtures)

Parameter		Min	Max	Unit
Bus Request–Bus Grant				
Timing Requirements:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 10$		ns
Switching Characteristics:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK} + 8$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 3$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

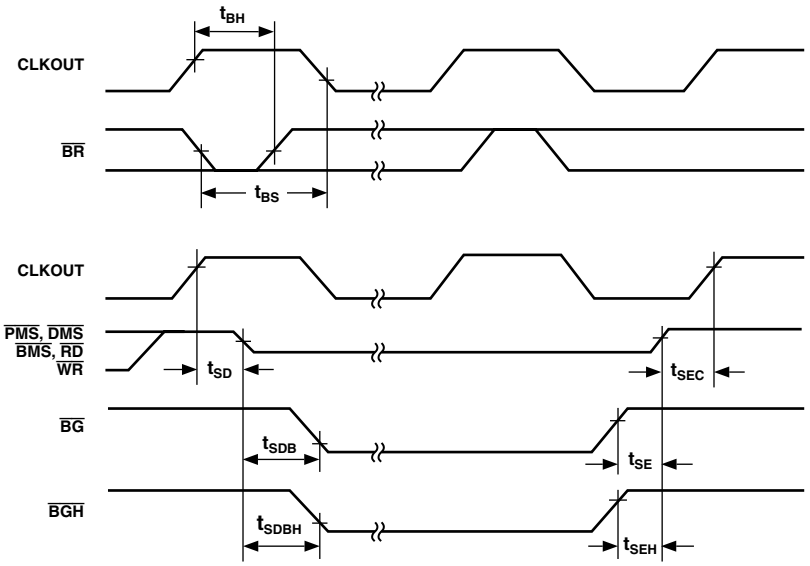


Figure 23. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 4 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 1$		ns
t_{WP}	$\overline{WR}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 3$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 2$	$0.25\ t_{CK} + 4$	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 5 + w$		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 1$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

NOTES
w = wait states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

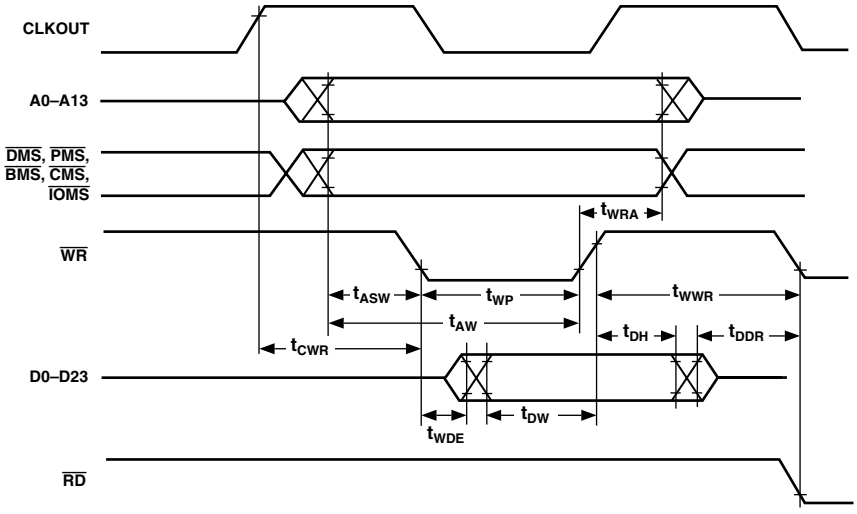


Figure 25. Memory Write

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IWP}	Duration of Write[1, 2]	10		ns
t_{IDSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	3		ns
t_{IDH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

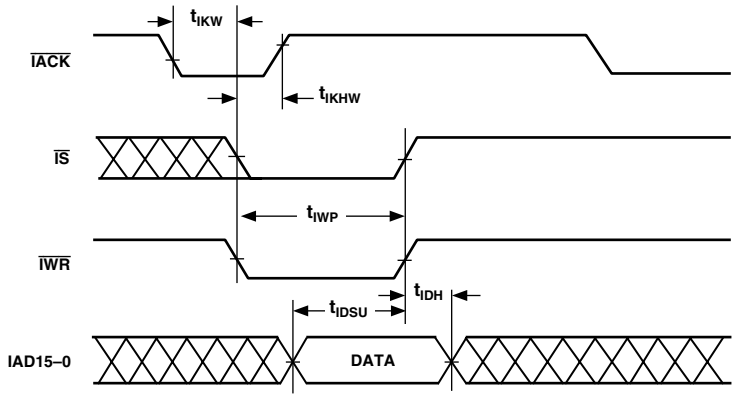


Figure 28. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	$0.5t_{CK} - 2$		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		11	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 5$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

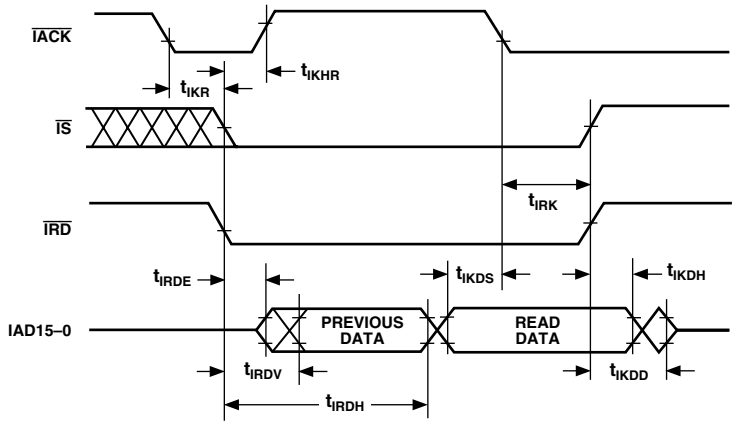


Figure 30. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle in Short Read Only Mode[1]				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[2]	0		ns
t_{IRP}	Duration of Read[3]	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[2]		10	ns
t_{IKDH}	IAD15–0 Previous Data Hold after End of Read[3]	0		ns
t_{IKDD}	IAD15–0 Previous Data Disabled after End of Read[3]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

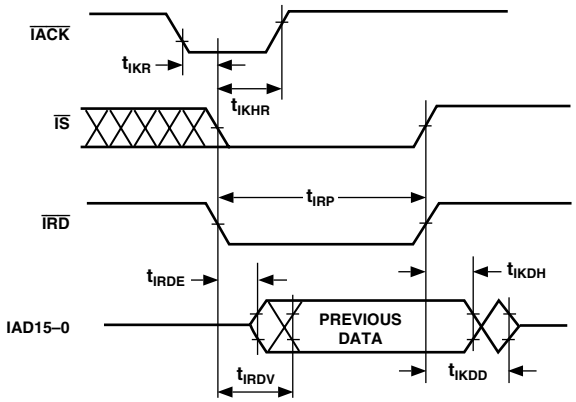


Figure 32. IDMA Read, Short Read Only Cycle

144-Ball Mini-BGA Package Pinout (Bottom View)

12	11	10	9	8	7	6	5	4	3	2	1	
GND	GND	D22	NC	NC	NC	GND	NC	A0	GND	A1/IAD0	A2/IAD1	A
D16	D17	D18	D20	D23	V_{DDEXT}	GND	NC	NC	GND	A3/IAD2	A4/IAD3	B
D14	NC	D15	D19	D21	V_{DDEXT}	$\overline{PWD}$	A7/IAD6	A5/IAD4	$\overline{RD}$	A6/IAD5	PWDACK	C
GND	NC	D12	D13	NC	PF2 [MODE C]	PF1 [MODE B]	A9/IAD8	$\overline{BGH}$	NC	$\overline{WR}$	NC	D
D10	GND	V_{DDEXT}	GND	GND	PF3 [MODE D]	FL2	PF0 [MODE A]	FL0	A8/IAD7	V_{DDEXT}	V_{DDEXT}	E
D9	NC	D8	D11	D7/$\overline{IWR}$	NC	NC	FL1	A11/IAD10	A12/IAD11	NC	A13/IAD12	F
D4/$\overline{IS}$	NC	NC	D5/IAL	D6/$\overline{IRD}$	NC	NC	NC	A10/IAD9	GND	NC	XTAL	G
GND	NC	GND	D3/$\overline{IACK}$	D2/IAD15	TFS0	DT0	V_{DDINT}	GND	GND	GND	CLKIN	H
V_{DDINT}	V_{DDINT}	D1/IAD14	$\overline{BG}$	RFS1/$\overline{IRQ0}$	D0/IAD13	SCLK0	V_{DDEXT}	V_{DDEXT}	NC	V_{DDINT}	CLKOUT	J
$\overline{EBG}$	$\overline{BR}$	$\overline{EBR}$	$\overline{ERESET}$	SCLK1	TFS1/$\overline{IRQ1}$	RFS0	$\overline{DMS}$	$\overline{BMS}$	NC	NC	NC	K
$\overline{EINT}$	ELOUT	ELIN	$\overline{RESET}$	GND	DR0	$\overline{PMS}$	GND	$\overline{IOMS}$	$\overline{IRQL1}$ + PF6	NC	$\overline{IRQE}$ + PF4	L
ECLK	EE	$\overline{EMS}$	NC	GND	DR1/FI	DT1/FO	GND	$\overline{CMS}$	NC	$\overline{IRQ2}$ + PF7	$\overline{IRQL0}$ + PF5	M

The Mini-BGA package pinout is shown in the table below. Pin names in **bold** text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

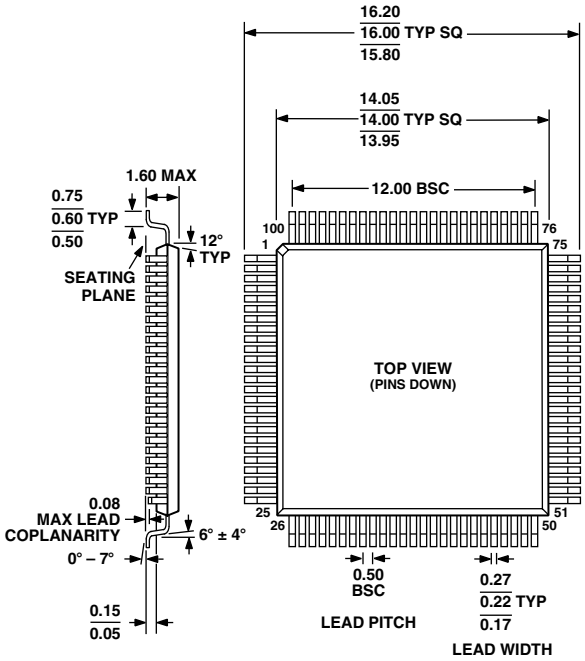
Mini-BGA Package Pinout

Ball #	Pin Name	Ball #	Pin Name	Ball #	Pin Name	Ball #	Pin Name
A01	A2/**IAD1**	D01	NC	G01	XTAL	K01	NC
A02	A1/**IAD0**	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/**IAD9**	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/**IAD8**	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/$\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/**$\overline{\text{IRD}}$**	K08	SCLK1
A09	NC	D09	D13	G09	D5/**IAL**	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/**$\overline{\text{IS}}$**	K12	$\overline{\text{EBG}}$
B01	A4/**IAD3**	E01	V_{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/**IAD2**	E02	V_{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/**IAD7**	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V_{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V_{DDEXT}	E07	PF3 [MODE D]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/**IAD15**	L08	GND
B09	D20	E09	GND	H09	D3/**$\overline{\text{IACK}}$**	L09	$\overline{\text{RESET}}$
B10	D18	E10	V_{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/**IAD12**	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/**IAD5**	F02	NC	J02	V_{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/**IAD11**	J03	NC	M03	NC
C04	A5/**IAD4**	F04	A11/**IAD10**	J04	V_{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/**IAD6**	F05	FL1	J05	V_{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V_{DDEXT}	F07	NC	J07	D0/**IAD13**	M07	DR1/FI
C08	D21	F08	D7/**$\overline{\text{IWR}}$**	J08	RFS1/$\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/**IAD14**	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V_{DDINT}	M11	EE
C12	D14	F12	D9	J12	V_{DDINT}	M12	ECLK

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

100-Lead Metric Thin Plastic Quad Flatpack (LQFP) (ST-100)

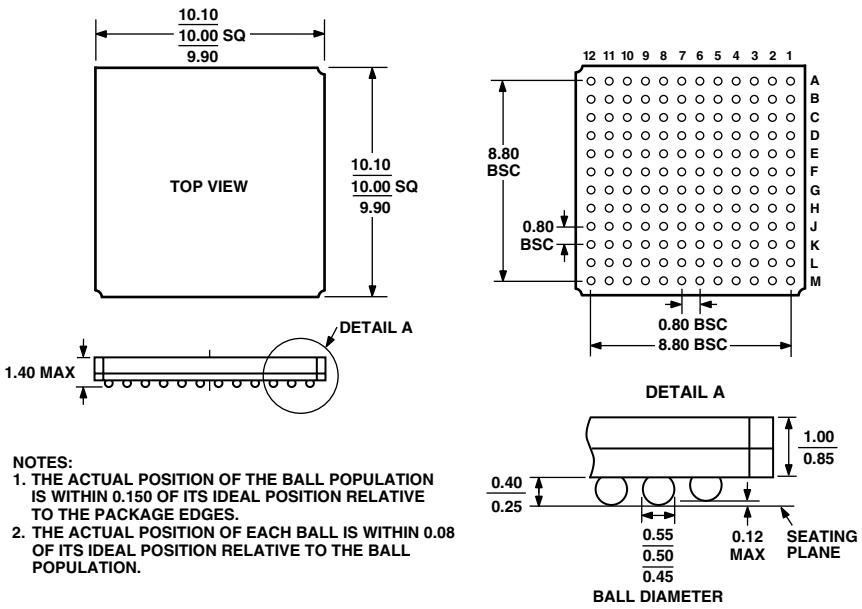


NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

OUTLINE DIMENSIONS

Dimensions shown in millimeters.

144-Ball Mini-BGA
(CA-144)



NOTES:
1. THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.150 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate	Package Description*	Package Option
ADSP-2186MKST-300	0°C to 70°C	75	100-Lead LQFP	ST-100
ADSP-2186MBST-266	–40°C to +85°C	66	100-Lead LQFP	ST-100
ADSP-2186MKCA-300	0°C to 70°C	75	144-Ball Mini-BGA	CA-144
ADSP-2186MBCA-266	–40°C to +85°C	66	144-Ball Mini-BGA	CA-144

*In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously labeled TQFP packages (1.6 mm thick) are now designated as LQFP.

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