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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	600
Number of I/O	36
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7032qi44-12">https://www.e-xfl.com/product-detail/intel/epm7032qi44-12</a>

**Table 2. MAX 7000S Device Features**

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
$t_{PD}$ (ns)	5	5	6	6	7.5	7.5
$t_{SU}$ (ns)	2.9	2.9	3.4	3.4	4.1	3.9
$t_{FSU}$ (ns)	2.5	2.5	2.5	2.5	3	3
$t_{CO1}$ (ns)	3.2	3.2	4	3.9	4.7	4.7
$f_{CNT}$ (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

## ...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

**Table 5. MAX 7000 Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

**Notes:**

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

**Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram**

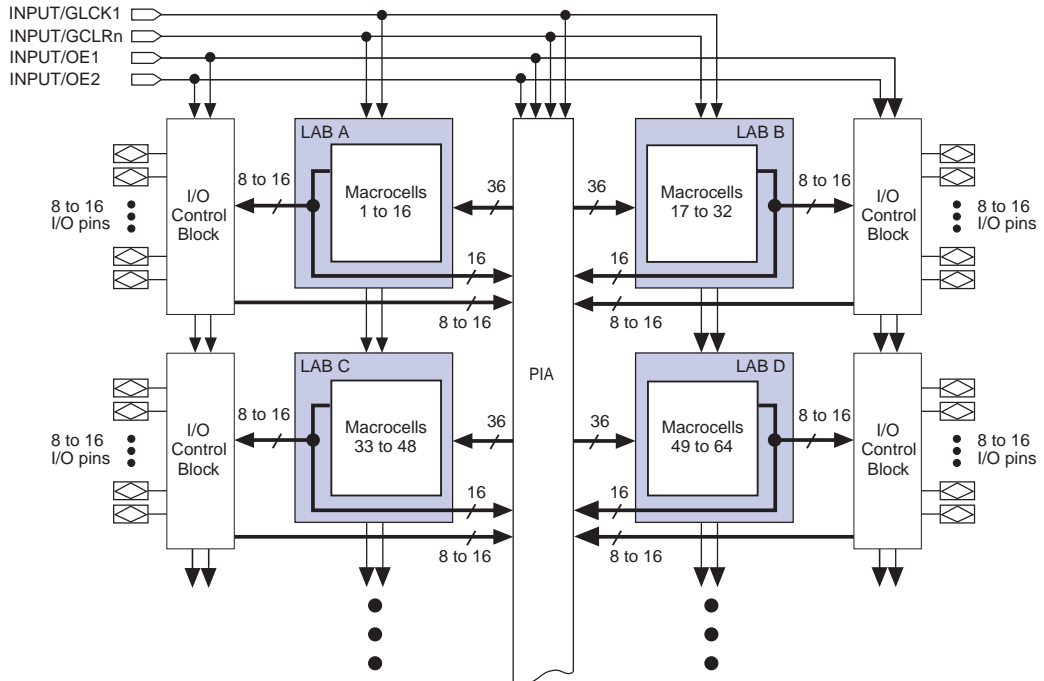
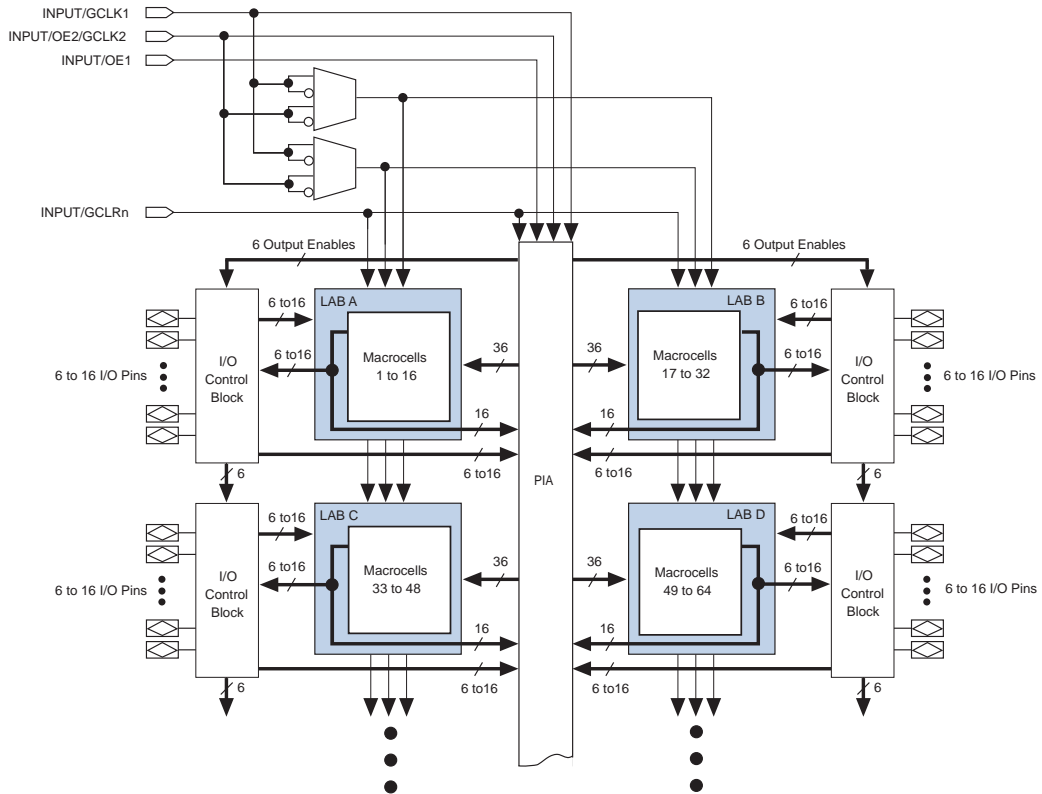


Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**



## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

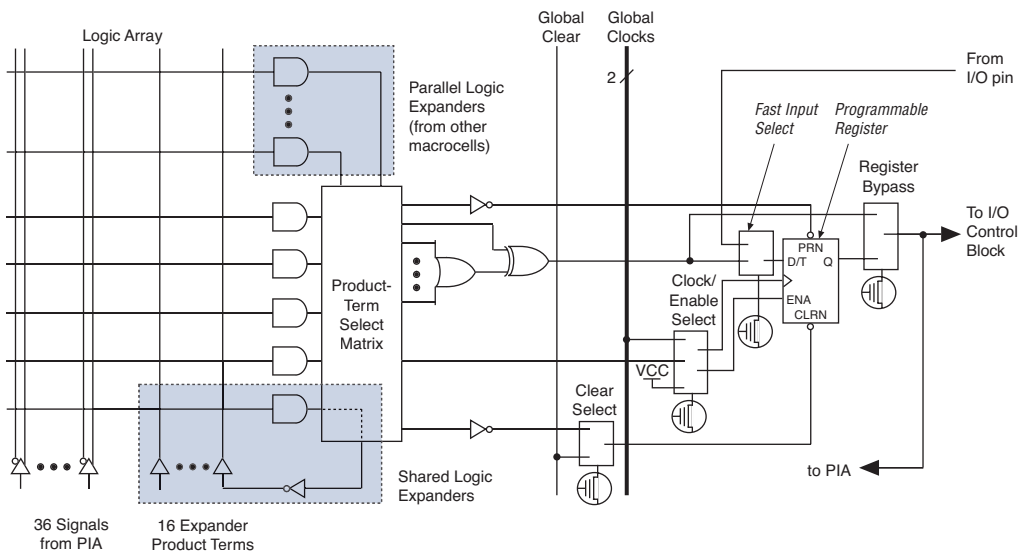
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

## Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

**Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell**

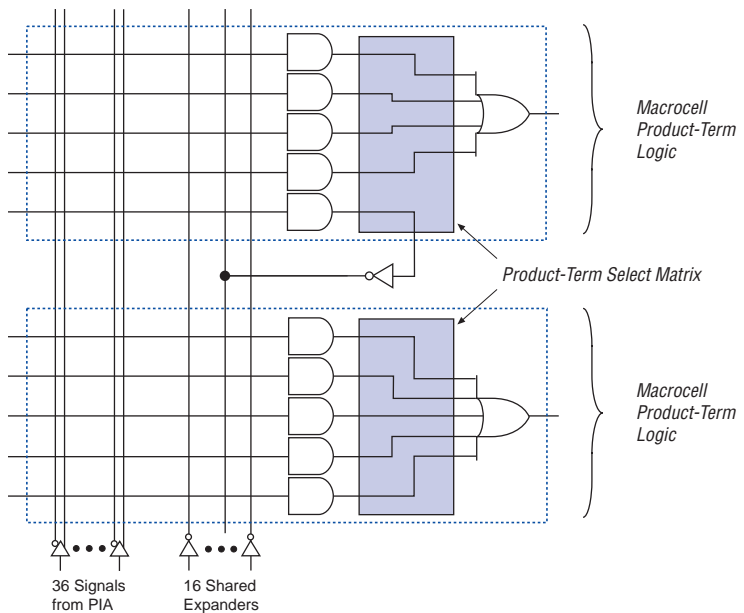


### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

**Figure 5. Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### Parallel Expanders

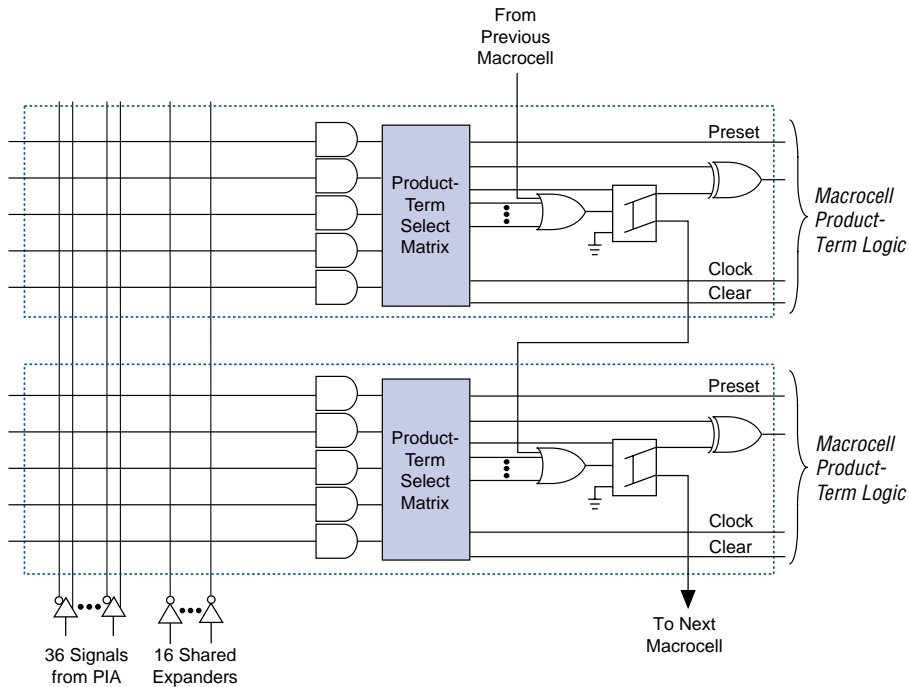
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 6. Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*

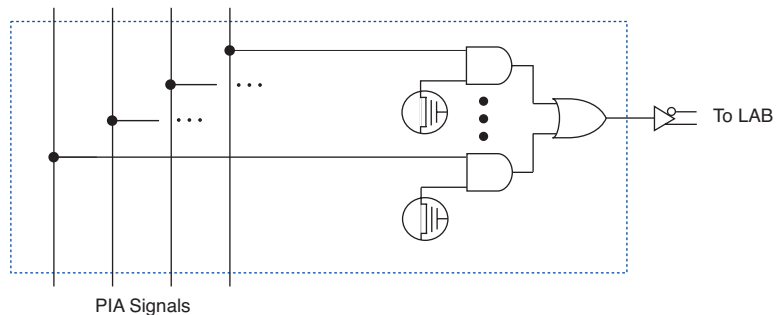




## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

**Figure 7. PIA Routing**



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000S Device*

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

### Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

## Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [Programming Hardware Manufacturers](#).

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. [Table 9](#) describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

**Table 9. MAX 7000 JTAG Instructions**

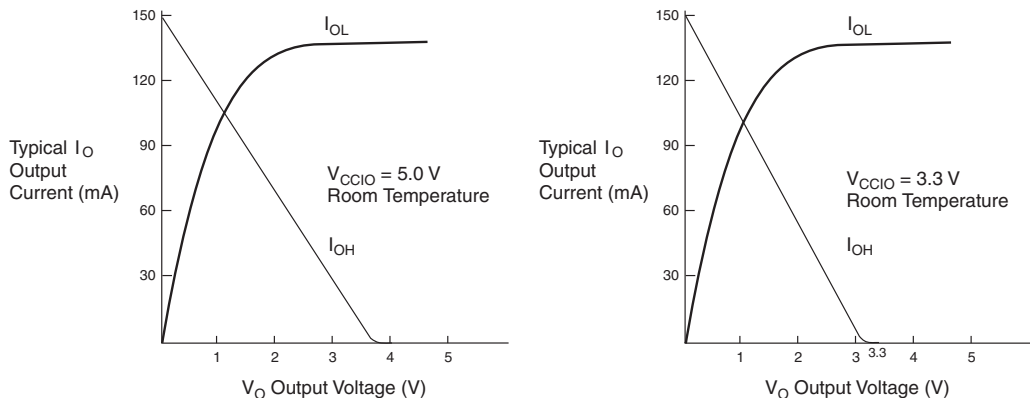
JTAG Instruction	Devices	Description
SAMPLE/PRELOAD	EPM7128S EPM7160S EPM7192S EPM7256S	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	EPM7128S EPM7160S EPM7192S EPM7256S	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ISP Instructions	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (.jam), Jam Byte-Code file (.jbc), or Serial Vector Format file (.svf) via an embedded processor or test equipment.

## Notes to tables:

- (1) See the [Operating Requirements for Altera Devices Data Sheet](#).
- (2) Minimum DC input voltage on I/O pins is  $-0.5$  V and on 4 dedicated input pins is  $-0.3$  V. During transitions, the inputs may undershoot to  $-2.0$  V or overshoot to  $7.0$  V for input currents less than  $100$  mA and periods shorter than  $20$  ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4)  $V_{CC}$  must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed  $300$   $\mu$ s. The sufficient  $V_{CCINT}$  voltage level for POR is  $4.5$  V. The device is fully initialized within the POR time after  $V_{CCINT}$  reaches the sufficient POR voltage level.
- (6)  $3.3$ -V I/O operation is not available for 44-pin packages.
- (7) The  $V_{CCISP}$  parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is  $-0.3$  V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically  $-60$   $\mu$ A.
- (13) Capacitance is measured at  $25^\circ$  C and is sample-tested only. The  $\text{OE}1$  pin has a maximum capacitance of  $20$  pF.

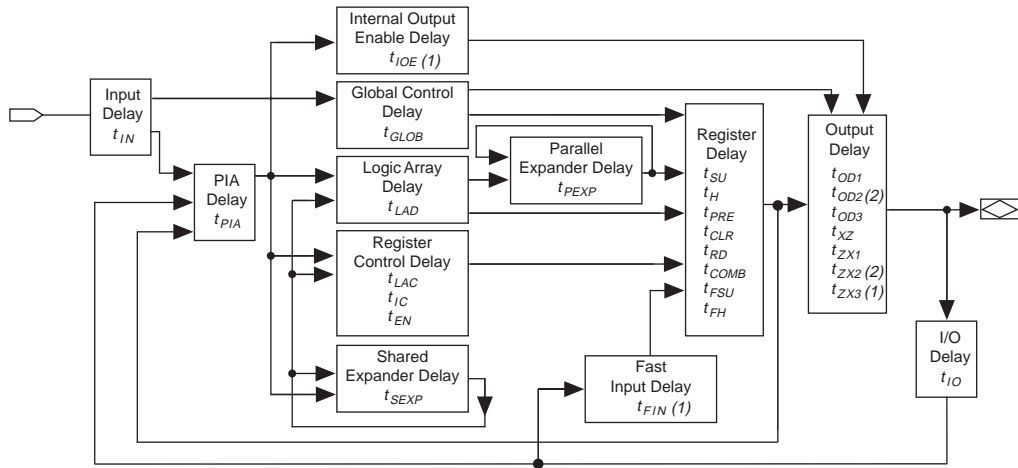
Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

**Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices**



## Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

**Figure 12. MAX 7000 Timing Model****Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).

**Table 21. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		8.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.5		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		2.0		3.0		ns
t <sub>AH</sub>	Array clock hold time		3.0		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t <sub>ACH</sub>	Array clock high time		4.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		4.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			10.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			10.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

**Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			1.0		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			1.0		2.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			7.0		7.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0	ns
$t_{LAD}$	Logic array delay			7.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
$t_{SU}$	Register setup time		1.0		4.0		ns
$t_H$	Register hold time		6.0		4.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	4.0		2.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.0		2.0		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			7.0		5.0	ns
$t_{GLOB}$	Global control delay			2.0		0.0	ns
$t_{PRE}$	Register preset time			4.0		3.0	ns
$t_{CLR}$	Register clear time			4.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		12.0	ns



**Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			2.0		2.0		3.0	ns
$t_{IO}$	I/O input pad and buffer delay			2.0		2.0		3.0	ns
$t_{FIN}$	Fast input delay	(2)		2.0		—		4.0	ns
$t_{SEXP}$	Shared expander delay			8.0		10.0		9.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0		2.0	ns
$t_{LAD}$	Logic array delay			6.0		6.0		8.0	ns
$t_{LAC}$	Logic control array delay			6.0		6.0		8.0	ns
$t_{IOE}$	Internal output enable delay	(2)		3.0		—		4.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		5.0		—		6.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		8.0		—		9.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.0		10.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		7.0		—		11.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		10.0		—		14.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		6.0		6.0		10.0	ns
$t_{SU}$	Register setup time		4.0		4.0		4.0		ns
$t_H$	Register hold time		4.0		4.0		5.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	2.0		—		4.0		ns
$t_{FH}$	Register hold time of fast input	(2)	2.0		—		3.0		ns
$t_{RD}$	Register delay			1.0		1.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.0		1.0	ns
$t_{IC}$	Array clock delay			6.0		6.0		8.0	ns
$t_{EN}$	Register enable time			6.0		6.0		8.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0		3.0	ns
$t_{PRE}$	Register preset time			4.0		4.0		4.0	ns
$t_{CLR}$	Register clear time			4.0		4.0		4.0	ns
$t_{PIA}$	PIA delay			2.0		2.0		3.0	ns
$t_{LPA}$	Low-power adder	(8)		13.0		15.0		15.0	ns

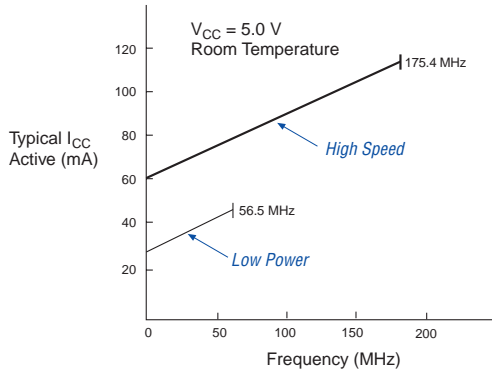
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 1 of 2)**

**EPM7032S**



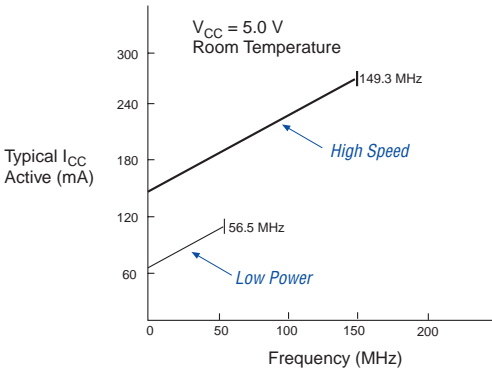
**EPM7064S**



**EPM7128S**

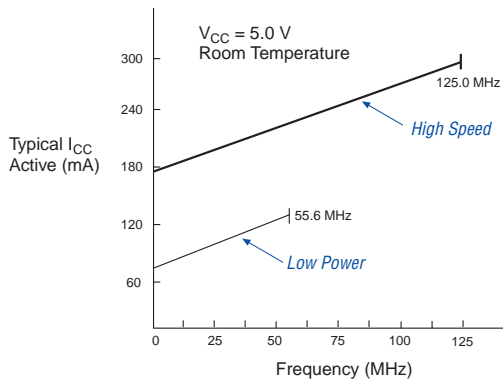


**EPM7160S**

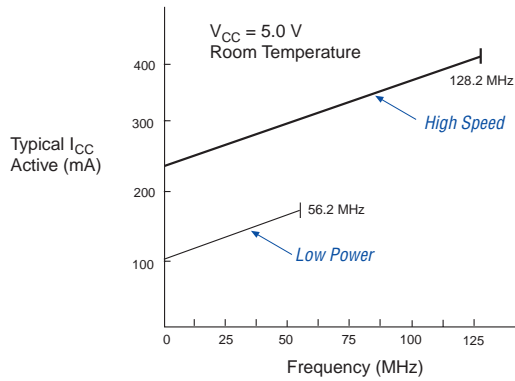


**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 2 of 2)**

EPM7192S



EPM7256S

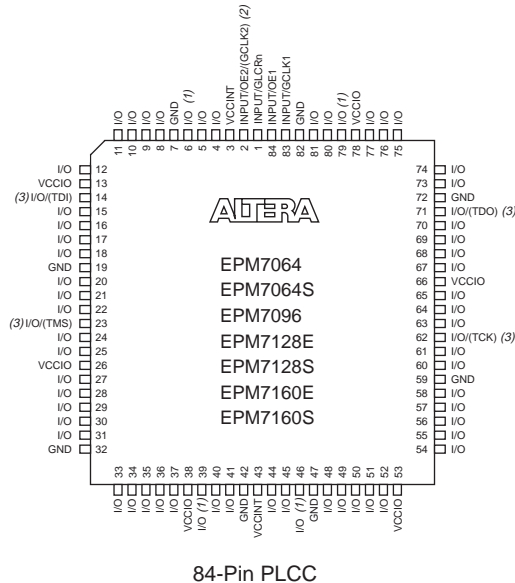


## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

**Figure 18. 84-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

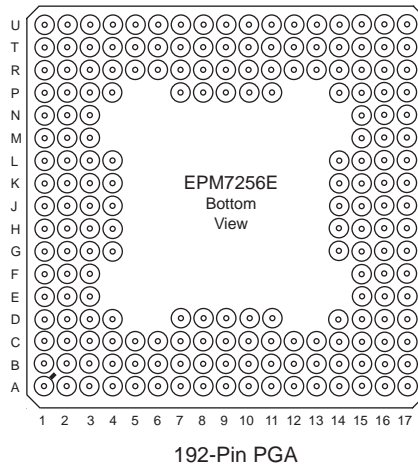


**Notes:**

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

**Figure 21. 192-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

**Figure 22. 208-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

