# Intel - EPM7032STC44-5N Datasheet

**Welcome to** E-XFL.COM

## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 2 |
| Number of Macrocells | 32 |
| Number of Gates | 600 |
| Number of I/O | 36 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7032stc44-5n |

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 3 for available speed grades.

*Table 3. MAX 7000 Speed Grades*

| Device | Speed Grade | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | -5 | -6 | -7 | -10P | -10 | -12P | -12 | -15 | -15T | -20 |
| EPM7032 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | |
| EPM7032S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7064 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7064S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7096 | | | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7128E | | | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7128S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7160E | | | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7160S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7192E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7192S | | | ✓ | | ✓ | | | ✓ | | |
| EPM7256E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7256S | | | ✓ | | ✓ | | | ✓ | | |

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-`AND`/fixed-`OR` array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported byAltera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

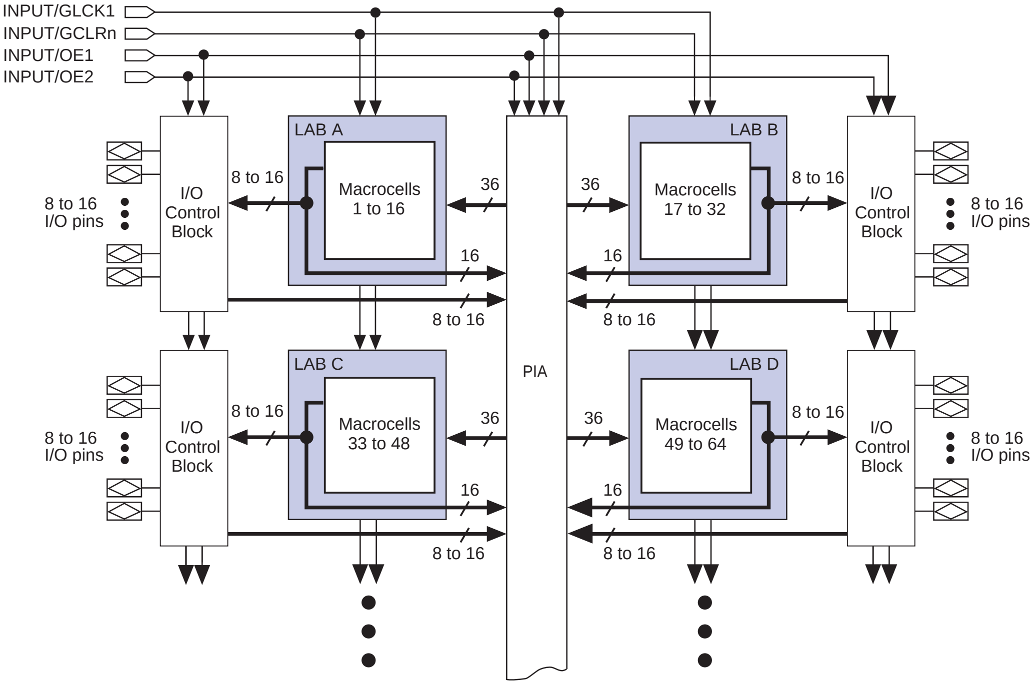
## Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

***Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram***



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

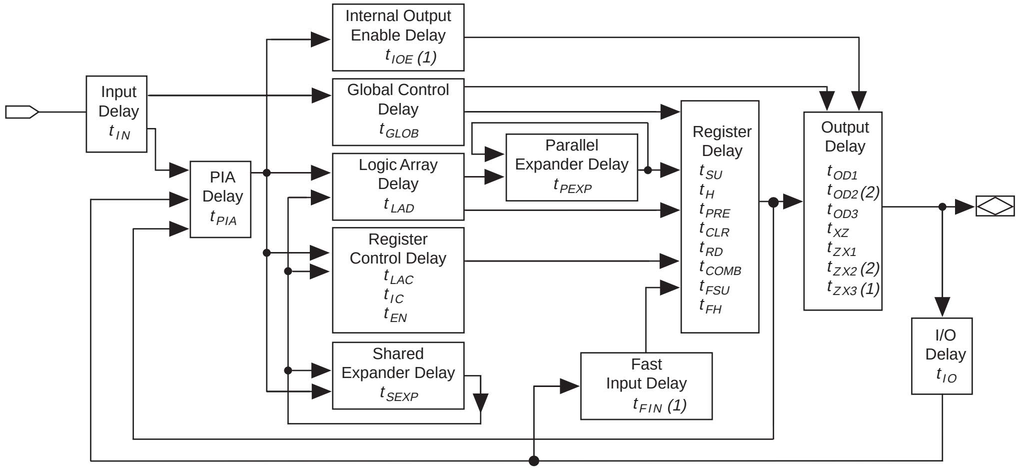
3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

**Figure 12. MAX 7000 Timing Model**



*Notes:*
(1) Only available in MAX 7000E and MAX 7000S devices.
(2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.

For more infomration, see *Application Note 94 (Understanding MAX 7000 Timing)*.

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 19. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | | 5.0 | | 6.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| $t_{CH}$ | Global clock high time | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.5 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.5 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.0 | | 2.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 3.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 200 | | 166.7 | | MHz |

***Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12)<br>MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 7.0 | | 7.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 7.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.0 | | 3.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.0 | | 4.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 5.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 6.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 4.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.0 | | 2.0 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 7.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 0.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 12.0 | ns |

**Table 25. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{SU}$ | Global clock setup time | | 11.0 | | 11.0 | | 12.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | – | | 5.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.0 | | – | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 8.0 | | 8.0 | | 12.0 | ns |
| $t_{CH}$ | Global clock high time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{CL}$ | Global clock low time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{ACH}$ | Array clock high time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 100 | | 83.3 | | 83.3 | | MHz |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This parameter applies to MAX 7000E devices only.

(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(6) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(7) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 2.9 | | 4.0 | | 5.0 | | 7.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 3.5 | | 4.3 | | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.7 | | 0.9 | | 1.1 | | 2.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.7 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.6 | | 8.2 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |

### *Table 27. EPM7032S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 250.0 | | 200.0 | | 166.7 | | 125.0 | | MHz |

### *Table 28. EPM7032S Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.2 | | 2.1 | | 2.5 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.1 | | 3.8 | | 4.6 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.9 | | 1.1 | | 1.4 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.5 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 0.8 | | 1.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.2 | | 0.3 | | 0.4 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.7 | | 0.8 | | 0.9 | | 2.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.2 | | 5.3 | | 5.4 | | 5.5 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 0.8 | | 1.0 | | 1.3 | | 2.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 1.7 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.8 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.9 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.1 | | 1.4 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.4 | | 4.2 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.4 | | 1.7 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.1 | | 1.4 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 10.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

**Table 29. EPM7064S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 2.9 | | 3.6 | | 6.0 | | 7.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 4.0 | | 4.5 | | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.7 | | 0.9 | | 3.0 | | 2.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.0 | | 3.0 | | ns |

**Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.0 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.3 | | 3.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.2 | | 3.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.9 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.3 | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 11.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 31 and 32 show the EPM7128S AC operating conditions.

**Table 31. EPM7128S External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{SU}$ | Global clock setup time | | 3.4 | | 6.0 | | 7.0 | | 11.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.5 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | | 5.0 | | 8.0 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.9 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 166.7 | | 125.0 | | 100.0 | | MHz |

**Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{H}$ | Register hold time | | 1.7 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.3 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.7 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.2 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.2 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.5 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 2.4 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

***Notes to tables:***

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

**Table 38. EPM7256S Internal Timing Parameters** *Note (1)*

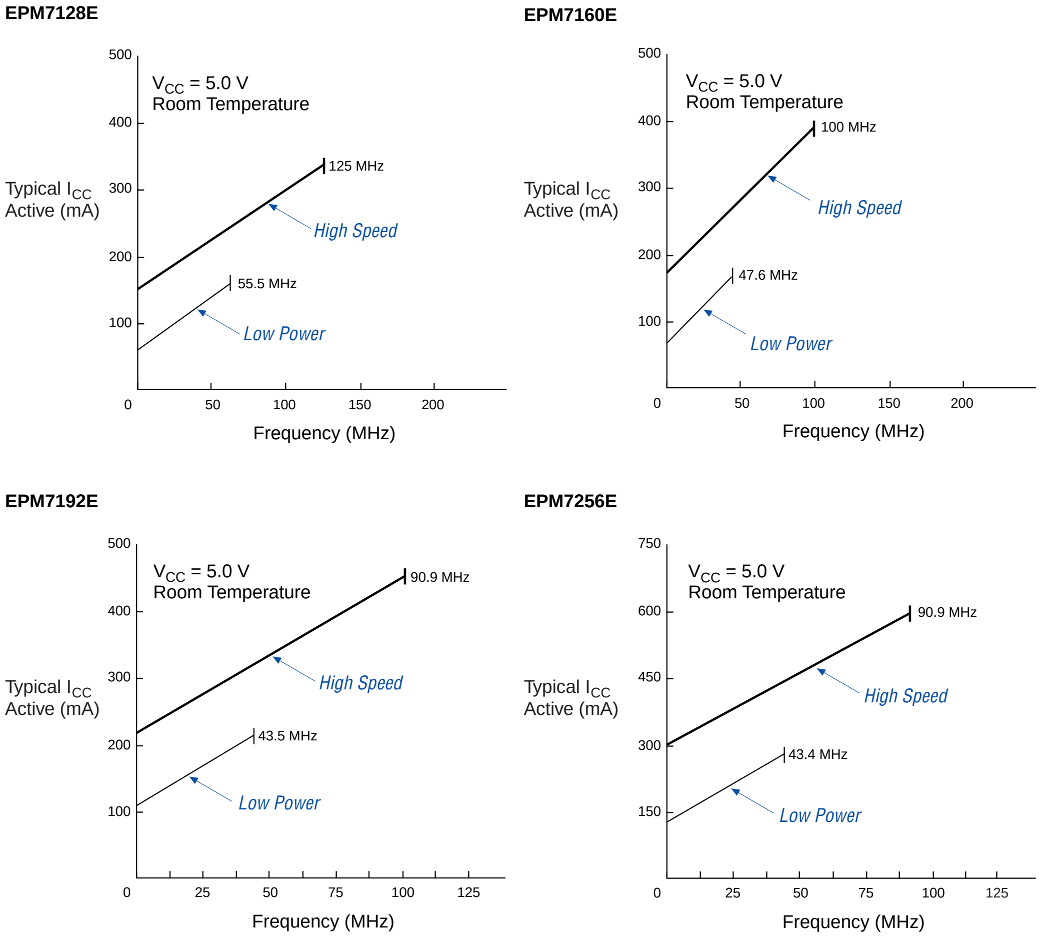
| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.4 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.9 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.8 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.5 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.1 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.6 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.4 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.9 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.8 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 3.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

*Table 39. MAX 7000 $I_{CC}$ Equation Constants*

| Device | A | B | C |
|---|---|---|---|
| EPM7032 | 1.87 | 0.52 | 0.144 |
| EPM7064 | 1.63 | 0.74 | 0.144 |
| EPM7096 | 1.63 | 0.74 | 0.144 |
| EPM7128E | 1.17 | 0.54 | 0.096 |
| EPM7160E | 1.17 | 0.54 | 0.096 |
| EPM7192E | 1.17 | 0.54 | 0.096 |
| EPM7256E | 1.17 | 0.54 | 0.096 |
| EPM7032S | 0.93 | 0.40 | 0.040 |
| EPM7064S | 0.93 | 0.40 | 0.040 |
| EPM7128S | 0.93 | 0.40 | 0.040 |
| EPM7160S | 0.93 | 0.40 | 0.040 |
| EPM7192S | 0.93 | 0.40 | 0.040 |
| EPM7256S | 0.93 | 0.40 | 0.040 |

This calculation provides an $I_{CC}$ estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

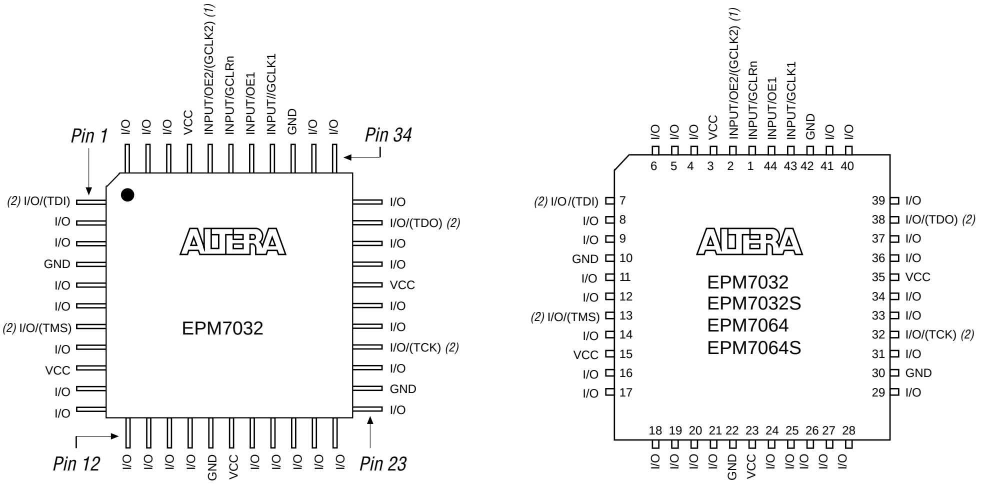
*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 2 of 2)*



Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

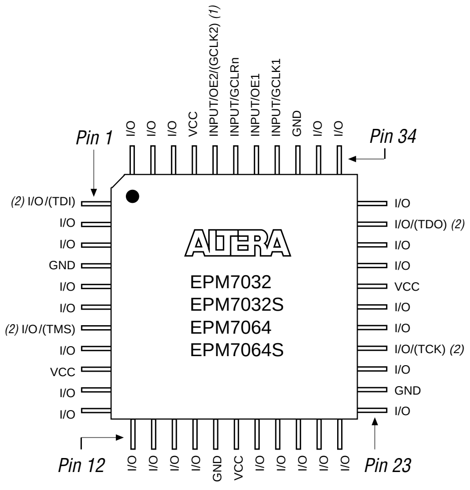
**Figure 16. 44-Pin Package Pin-Out Diagram**

*Package outlines not drawn to scale.*



44-Pin PQFP

44-Pin PLCC



44-Pin TQFP

*Notes:*

(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.

(2) JTAG ports are available in MAX 7000S devices only.

# Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

## Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

## Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

## Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on page 16.

## Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added *Note (5)* on page 28.

## Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
literature@altera.com

Copyright © 2005 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

I.S. EN ISO 9001