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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	2
Number of Macrocells	32
Number of Gates	600
Number of I/O	36
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7032stc44-7f

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68	68						
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

Notes:

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

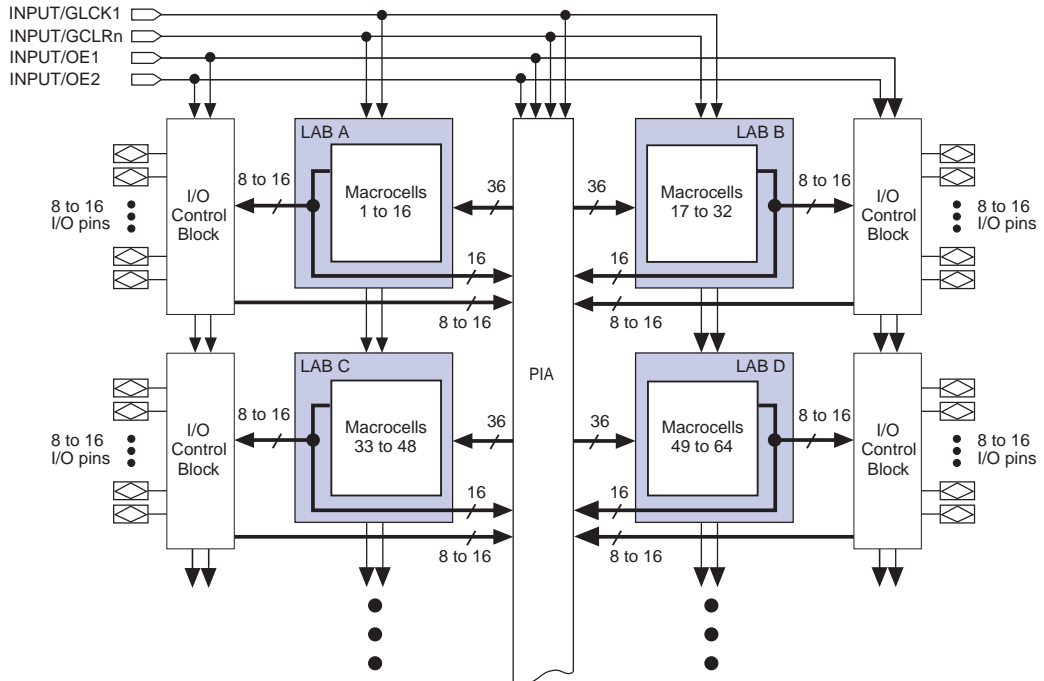
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram

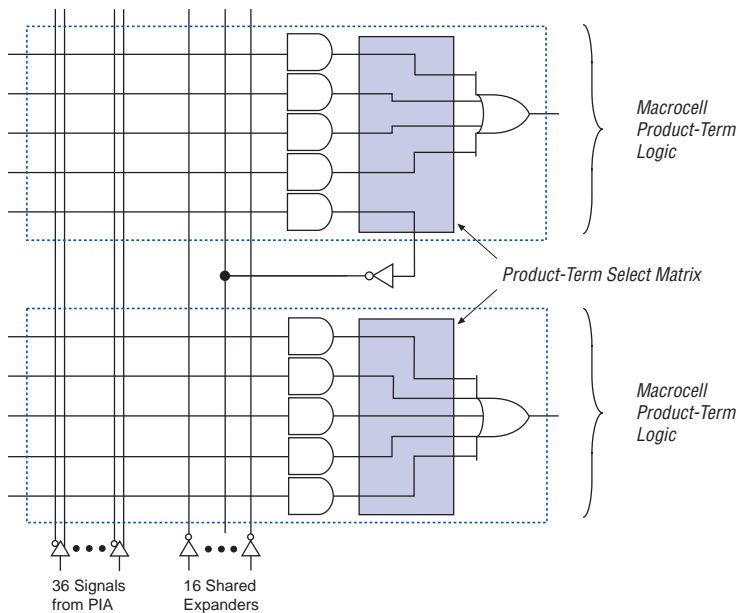


Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.

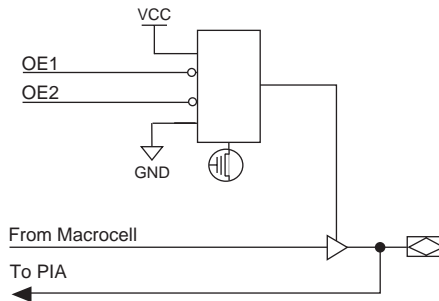


Parallel Expanders

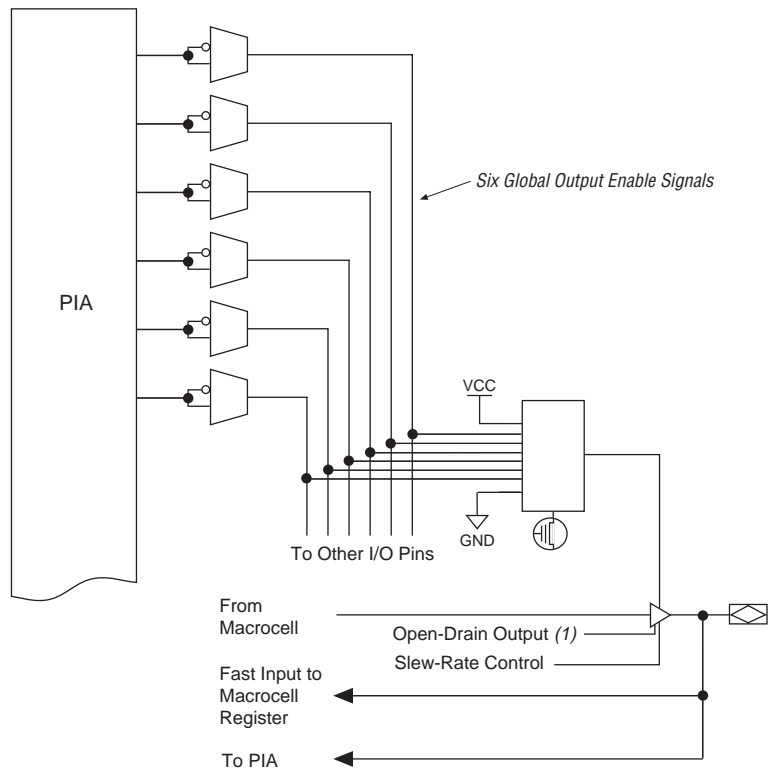
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7064 & EPM7096 Devices



MAX 7000E & MAX 7000S Devices



Note:

- (1) The open-drain output option is available only in MAX 7000S devices.



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The programming times described in [Tables 6 through 8](#) are associated with the worst-case method using the enhanced ISP algorithm.

Table 6. MAX 7000S t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

[Tables 7](#) and [8](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [*Altera Programming Hardware Data Sheet*](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [*Programming Hardware Manufacturers*](#).

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5 (8)	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V (10)	$V_{CCIO} - 0.2$		V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (11)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V (11)		0.2	V
I_I	Leakage current of dedicated input pins	$V_I = -0.5$ to 5.5 V (11)	-10	10	μ A
I_{OZ}	I/O pin tri-state output off-state current	$V_I = -0.5$ to 5.5 V (11), (12)	-40	40	μ A

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 19. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

Table 20. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade -6		Speed Grade -7		Unit
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.5	ns
t_{FIN}	Fast input delay	(2)		0.8		1.0	ns
t_{SEXP}	Shared expander delay			3.5		4.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			2.0		3.0	ns
t_{LAC}	Logic control array delay			2.0		3.0	ns
t_{OE}	Internal output enable delay	(2)				2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		2.0		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		7.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		4.0		4.0	ns
t_{SU}	Register setup time		3.0		3.0		ns
t_H	Register hold time		1.5		2.0		ns
t_{FSU}	Register setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Register hold time of fast input	(2)	0.5		0.5		ns
t_{RD}	Register delay			0.8		1.0	ns
t_{COMB}	Combinatorial delay			0.8		1.0	ns
t_{JC}	Array clock delay			2.5		3.0	ns
t_{EN}	Register enable time			2.0		3.0	ns
t_{GLOB}	Global control delay			0.8		1.0	ns
t_{PRE}	Register preset time			2.0		2.0	ns
t_{CLR}	Register clear time			2.0		2.0	ns
t_{PIA}	PIA delay			0.8		1.0	ns
t_{LPA}	Low-power adder	(8)		10.0		10.0	ns

Table 21. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{SU}	Global clock setup time		7.0		8.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		2.0		3.0		ns
t _{AH}	Array clock hold time		3.0		3.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t _{ACH}	Array clock high time		4.0		4.0		ns
t _{ACL}	Array clock low time		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			10.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t _{ACNT}	Minimum array clock period			10.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t _{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t _{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t _{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_H	Register hold time		1.7		2.0		2.0		3.0		ns

Tables 31 and 32 show the EPM7128S AC operating conditions.

Table 31. EPM7128S External Timing Parameters Note (1)											
Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t _{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Tables 37 and 38 show the EPM7256S AC operating conditions.

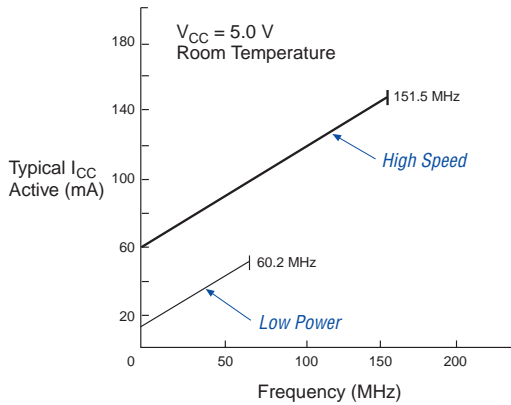
Table 37. EPM7256S External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.9		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t _{AH}	Array clock hold time		1.9		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			7.8		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			7.8		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

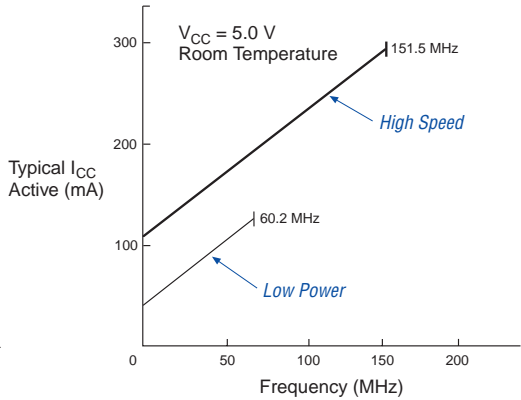
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

EPM7032



EPM7064



EPM7096

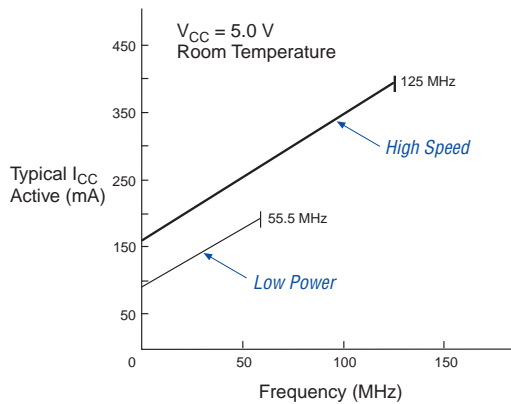


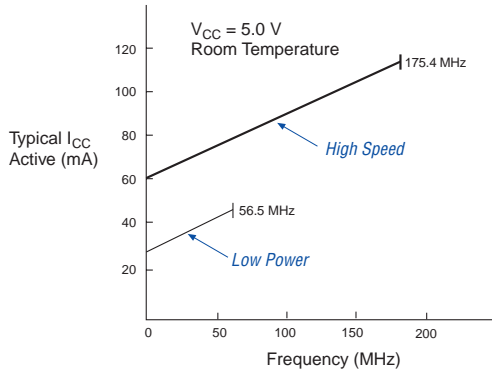
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

EPM7032S



EPM7064S



EPM7128S



EPM7160S

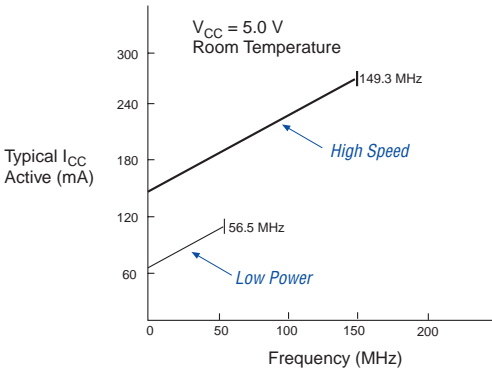
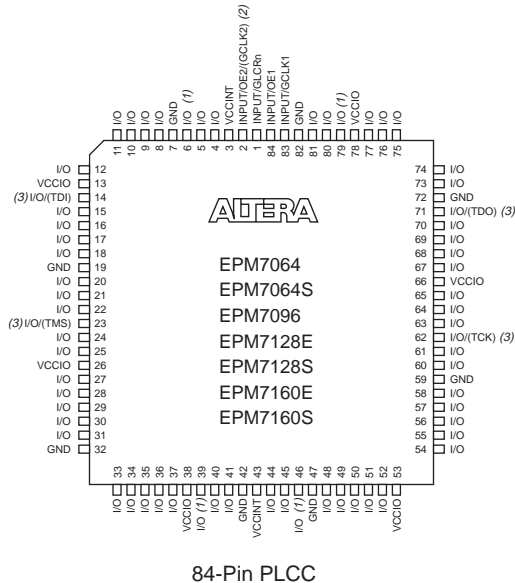


Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).



Notes: