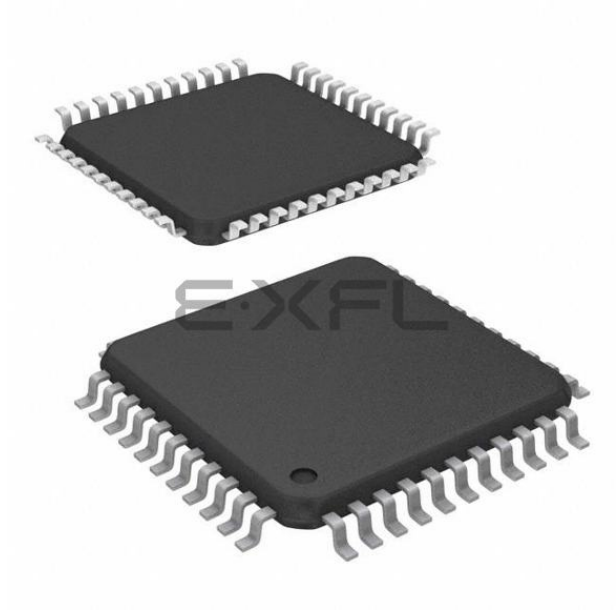

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 4.5V ~ 5.5V |
| Number of Logic Elements/Blocks | 2 |
| Number of Macrocells | 32 |
| Number of Gates | 600 |
| Number of I/O | 36 |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-TQFP |
| Supplier Device Package | 44-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7032sti44-7 |

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

*Table 5. MAX 7000 Maximum User I/O Pins* *Note (1)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84 *(2)* | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84 *(2)* | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132 *(2)* | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164 *(2)* | 164 |

*Notes:*

(1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

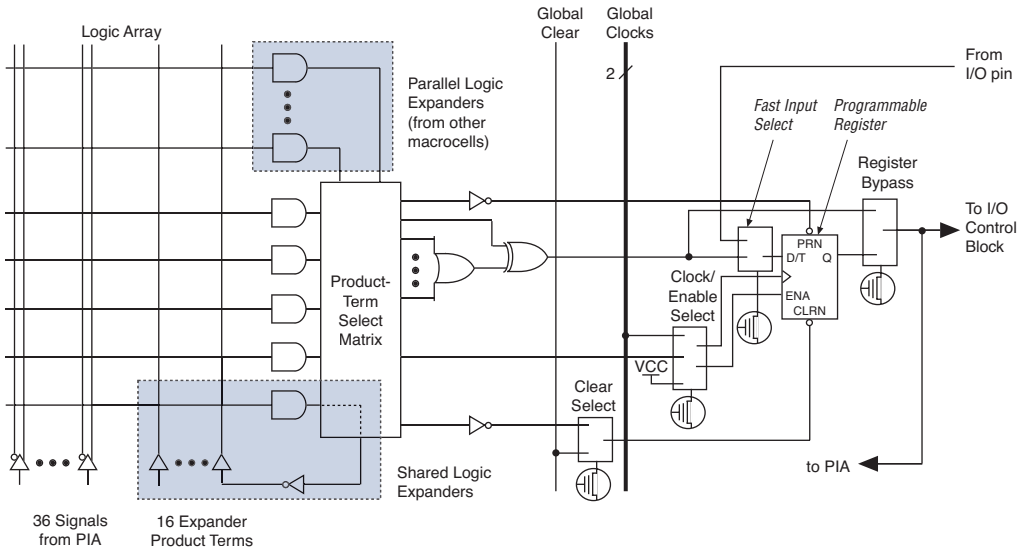
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

## Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

***Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell***

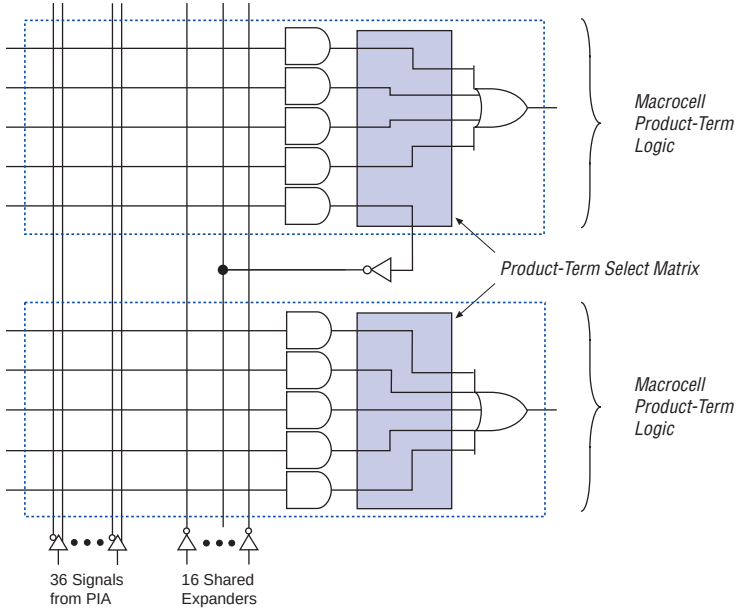


### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{SEXP}$) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

***Figure 5. Shareable Expanders***

*Shareable expanders can be shared by any or all macrocells in an LAB.*




### *Parallel Expanders*

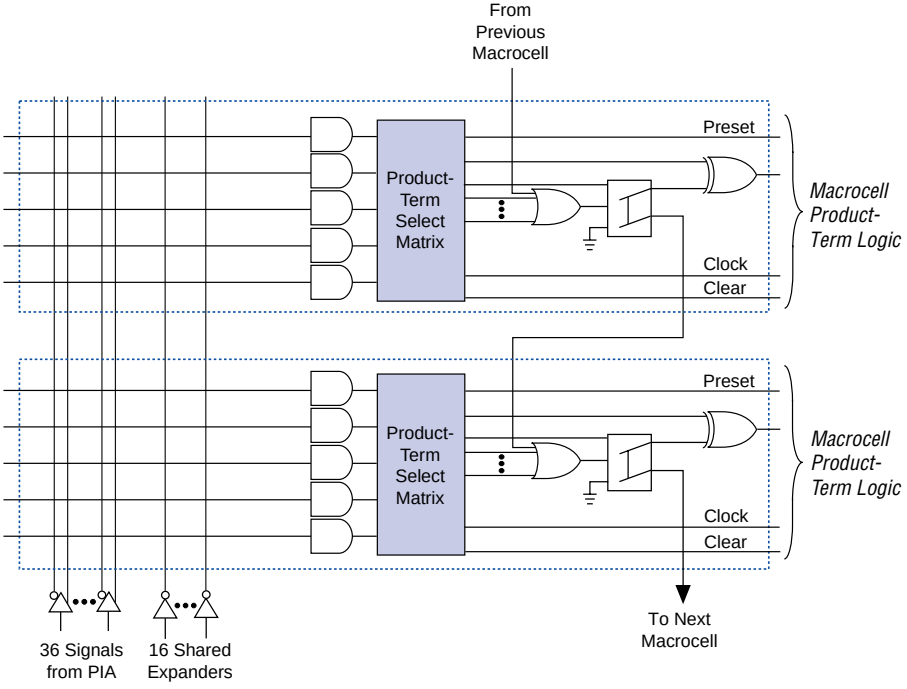
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

***Figure 6. Parallel Expanders***

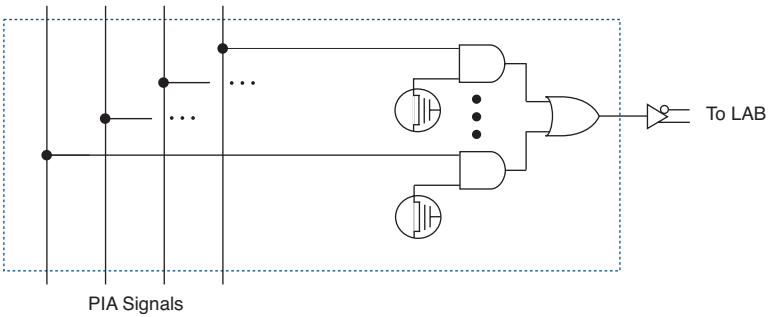
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

*Figure 7. PIA Routing*




While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When $V_{CCIO}$ is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When $V_{CCIO}$ is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

### Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

## Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see the *Programming Hardware Manufacturers*.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 9 describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

*Table 9. MAX 7000 JTAG Instructions*

| JTAG Instruction | Devices | Description |
|---|---|---|
| SAMPLE/PRELOAD | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins. |
| EXTEST | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation. |
| IDCODE | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| ISP Instructions | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (**.jam**), Jam Byte-Code file (**.jbc**), or Serial Vector Format file (**.svf**) via an embedded processor or test equipment. |

## Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

*Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings* *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP packages, under bias | | 135 | ° C |

*Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)*, *(5)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 5.0-V operation | *(3)*, *(4)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | *(3)*, *(4)*, *(6)* | 3.00 (3.00) | 3.60 (3.60) | V |
| $V_{CCISP}$ | Supply voltage during ISP | *(7)* | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | –0.5 *(8)* | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 19. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | | 5.0 | | 6.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| $t_{CH}$ | Global clock high time | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.5 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.5 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.0 | | 2.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 3.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 200 | | 166.7 | | MHz |

*Table 21. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 8.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 5.0 | | 5 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.0 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 3.0 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 4.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 4.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 4.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 10.0 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 10.0 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

*Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 2.0 | | – | | 4.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 8.0 | | 10.0 | | 9.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 3.0 | | – | | 4.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 5.0 | | – | | 6.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 8.0 | | – | | 9.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | | 10.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | – | | 11.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | – | | 14.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | | 10.0 | ns |
| $t_{SU}$ | Register setup time | | 4.0 | | 4.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 2.0 | | – | | 4.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 2.0 | | – | | 3.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{EN}$ | Register enable time | | | 6.0 | | 6.0 | | 8.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.0 | | 3.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 4.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 4.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 13.0 | | 15.0 | | 15.0 | ns |

**Table 32. EPM7128S Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.6 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.7 | | 4.0 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.4 | | 2.0 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.9 | | 2.5 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.4 | | 7.0 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 3.0 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.1 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.4 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 33 and 34 show the EPM7160S AC operating conditions.

***Table 33. EPM7160S External Timing Parameters (Part 1 of 2)*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 3.4 | | 4.2 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.9 | | 4.8 | | 5 | | 8 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.9 | | 1.1 | | 2.0 | | 4.0 | | ns |
| $\mathbf{t_{AH}}$ | Array clock hold time | | 1.7 | | 2.1 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ACO1}}$ | Array clock to output delay | C1 = 35 pF | | 6.4 | | 7.9 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{ACH}}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{ACL}}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{CPPW}}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $\mathbf{t_{ODH}}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $\mathbf{t_{CNT}}$ | Minimum global clock period | | | 6.7 | | 8.2 | | 10.0 | | 13.0 | ns |
| $\mathbf{f_{CNT}}$ | Maximum internal global clock frequency | *(4)* | 149.3 | | 122.0 | | 100.0 | | 76.9 | | MHz |

*Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.6 | | 2.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

*Table 35. EPM7192S External Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 4.1 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 1.0 | | 2.0 | | 4.0 | | ns |

*Table 35. EPM7192S External Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 3.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 7.8 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 125.0 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 125.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 125.0 | | 100.0 | | MHz |

*Table 36. EPM7192S Internal Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.2 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 4.2 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.2 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.9 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.1 | | 2.0 | | 4.0 | | ns |

*Table 38. EPM7256S Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.3 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 3.4 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.9 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.8 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.5 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 1.0 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.5 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.1 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.6 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.4 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.1 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.9 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.8 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 3.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$ in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCINT}$ value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

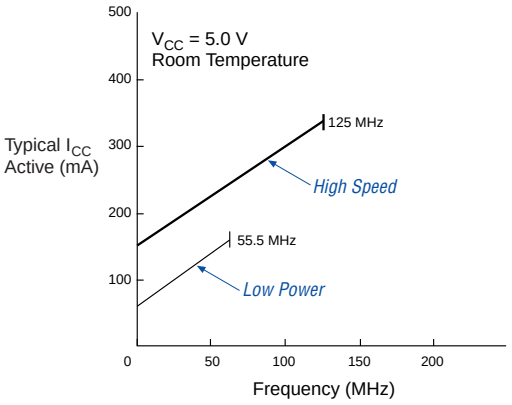
$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}}$$

The parameters in this equation are shown below:

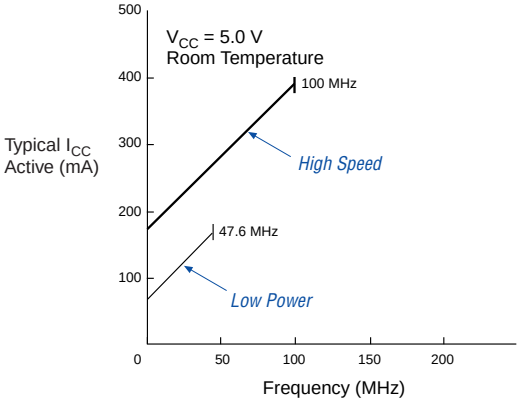
| | | |
|---|---|---|
| $MC_{TON}$ | = | Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $MC_{DEV}$ | = | Number of macrocells in the device |
| $MC_{USED}$ | = | Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $\mathbf{f_{MAX}}$ | = | Highest clock frequency to the device |
| $\mathbf{tog_{LC}}$ | = | Average ratio of logic cells toggling at each clock (typically 0.125) |
| A, B, C | = | Constants, shown in Table 39 |

*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 2 of 2)*

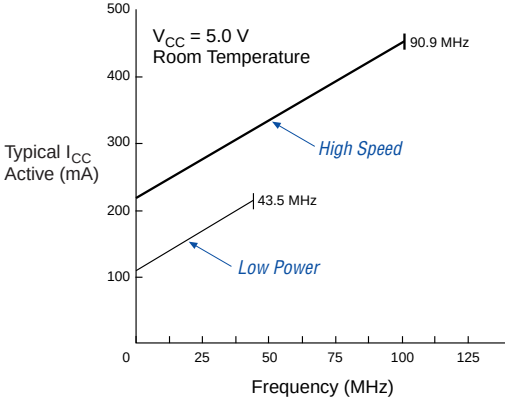
**EPM7128E**



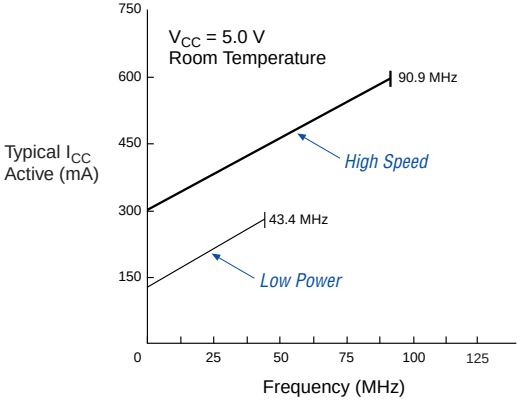

**EPM7160E**




**EPM7192E**




**EPM7256E**



# Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

## Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

## Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

## Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on page 16.

## Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added *Note (5)* on page 28.

## Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.