



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

| | |
|---------------------------------|---|
| Product Status | Obsolete |
| Programmable Type | EE PLD |
| Delay Time tpd(1) Max | 10 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | 1250 |
| Number of I/O | 36 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7064lc44-10yy |

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|----------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|-----------------|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84 (2) | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84 (2) | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132 (2) | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164 (2) | 164 |

Notes:

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

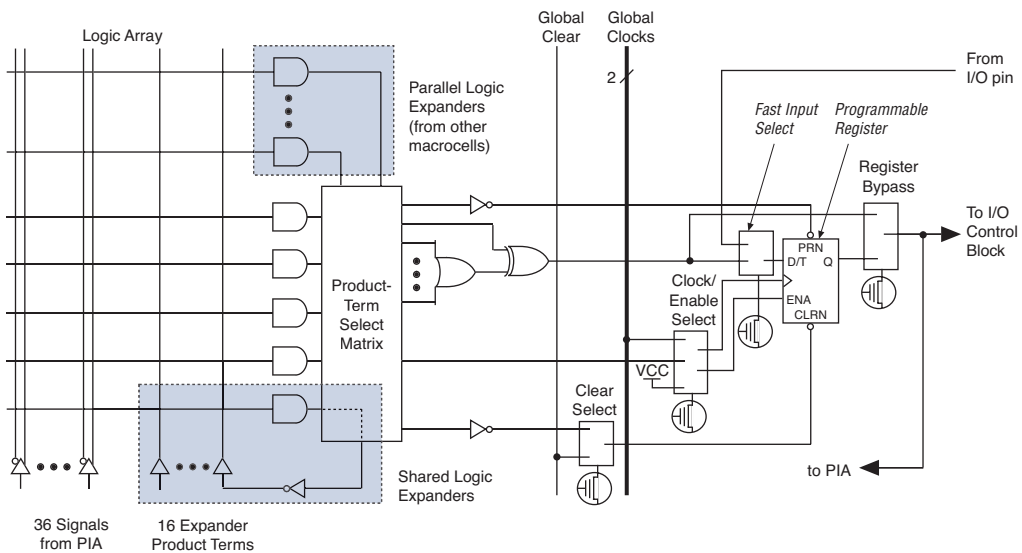
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell



Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

Expander Product Terms

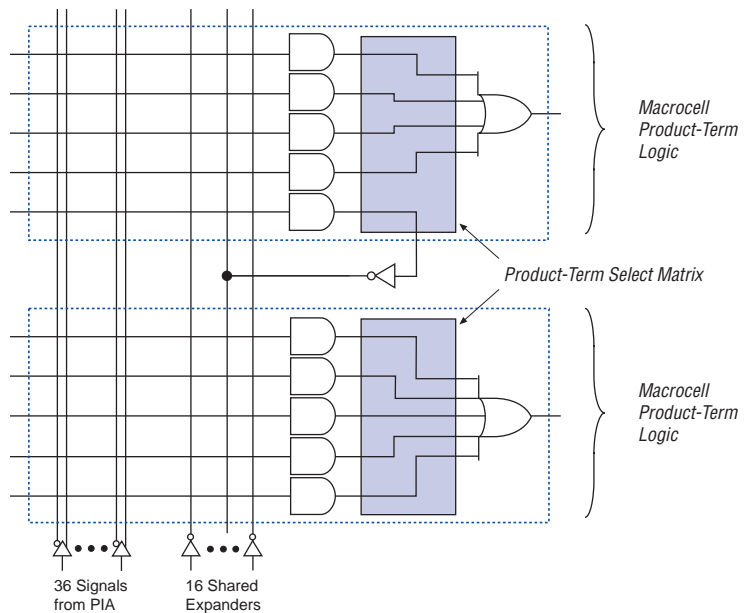
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

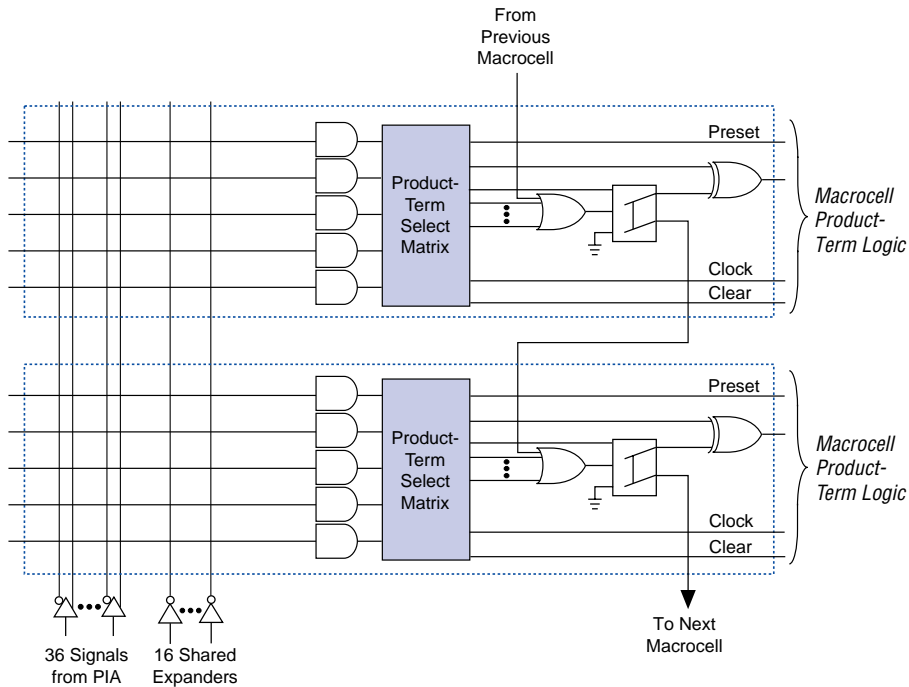
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [*Altera Programming Hardware Data Sheet*](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [*Programming Hardware Manufacturers*](#).

Design Security

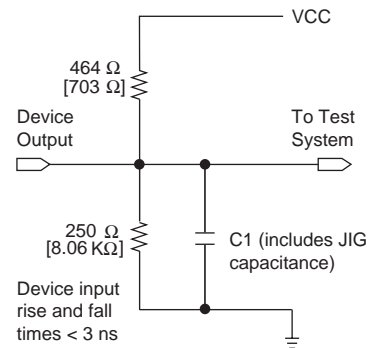
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 10](#). Test patterns can be used and then erased during early stages of the production flow.

Figure 10. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.



For detailed information and carrier dimensions, refer to the [QFP Carrier & Development Socket Data Sheet](#).



MAX 7000S devices are not shipped in carriers.

Operating Conditions

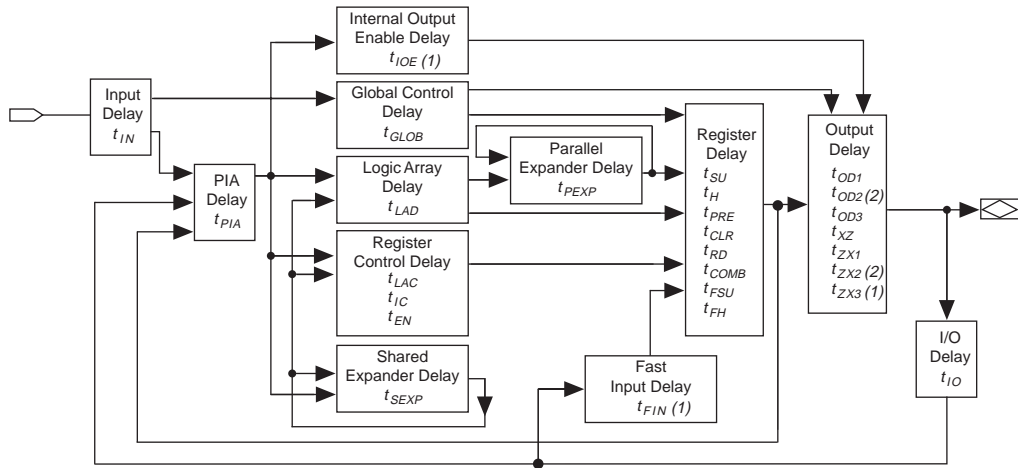
Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|----------------------------|------------------------------------|------|-----|------|
| V_{CC} | Supply voltage | With respect to ground (2) | –2.0 | 7.0 | V |
| V_I | DC input voltage | | –2.0 | 7.0 | V |
| I_{OUT} | DC output current, per pin | | –25 | 25 | mA |
| T_{STG} | Storage temperature | No bias | –65 | 150 | °C |
| T_{AMB} | Ambient temperature | Under bias | –65 | 135 | °C |
| T_J | Junction temperature | Ceramic packages, under bias | | 150 | °C |
| | | PQFP and RQFP packages, under bias | | 135 | °C |

Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------|---|--------------------|----------------|-------------------|------|
| V_{CCINT} | Supply voltage for internal logic and input buffers | (3), (4), (5) | 4.75 (4.50) | 5.25 (5.50) | V |
| V_{CCIO} | Supply voltage for output drivers, 5.0-V operation | (3), (4) | 4.75 (4.50) | 5.25 (5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | (3), (4), (6) | 3.00 (3.00) | 3.60 (3.60) | V |
| V_{CCISP} | Supply voltage during ISP | (7) | 4.75 | 5.25 | V |
| V_I | Input voltage | | –0.5 (8) | $V_{CCINT} + 0.5$ | V |
| V_O | Output voltage | | 0 | V_{CCIO} | V |
| T_A | Ambient temperature | For commercial use | 0 | 70 | °C |
| | | For industrial use | –40 | 85 | °C |
| T_J | Junction temperature | For commercial use | 0 | 90 | °C |
| | | For industrial use | –40 | 105 | °C |
| t_R | Input rise time | | | 40 | ns |
| t_F | Input fall time | | | 40 | ns |

Figure 12. MAX 7000 Timing Model**Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

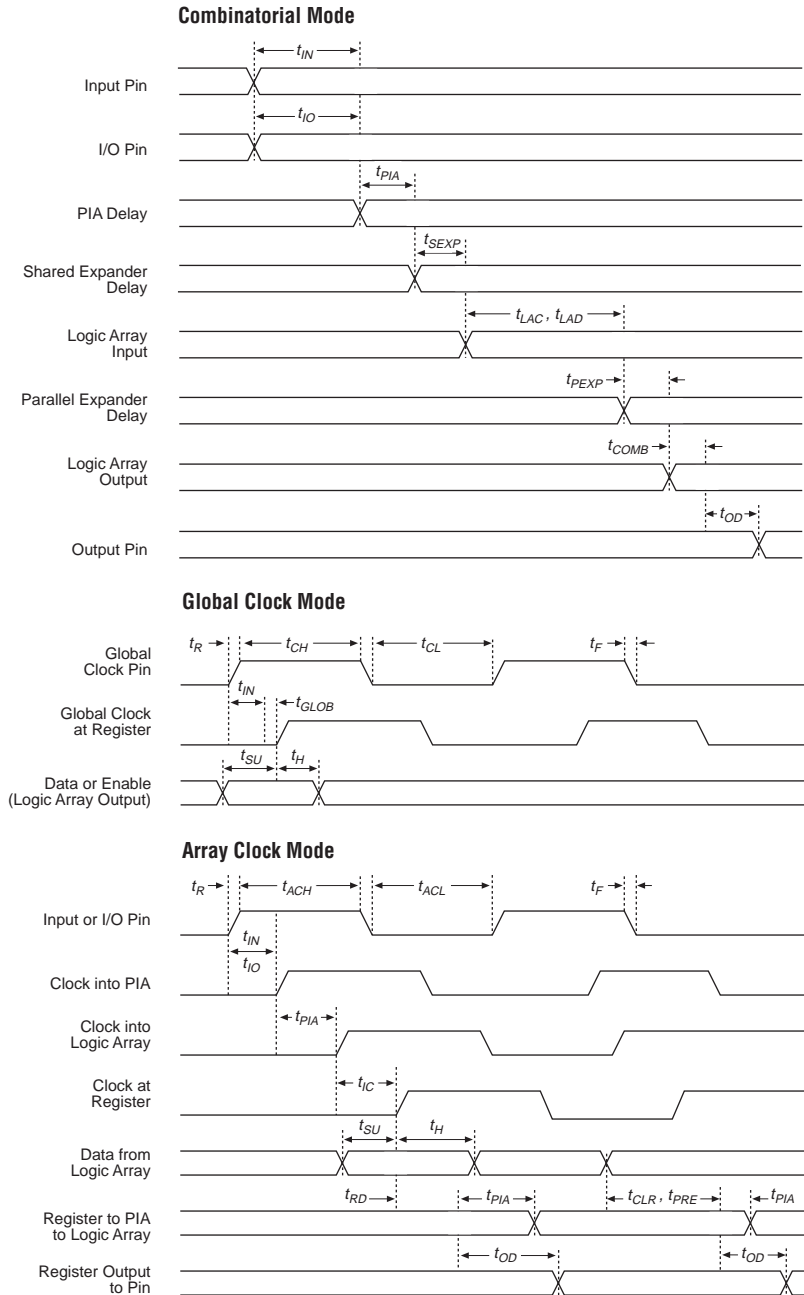
The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see *Application Note 94 (Understanding MAX 7000 Timing)*.

Figure 13. Switching Waveforms

t_R & $t_F < 3$ ns.
Inputs are driven at 3 V
for a logic high and 0 V
for a logic low. All timing
characteristics are
measured at 1.5 V.



Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 19. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|------------|--|----------------|----------------|-----|----------------|-----|------|
| | | | Min | Max | Min | Max | |
| t_{PD1} | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| t_{PD2} | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| t_{SU} | Global clock setup time | | 5.0 | | 6.0 | | ns |
| t_H | Global clock hold time | | 0.0 | | 0.0 | | ns |
| t_{FSU} | Global clock setup time of fast input | (2) | 2.5 | | 3.0 | | ns |
| t_{FH} | Global clock hold time of fast input | (2) | 0.5 | | 0.5 | | ns |
| t_{CO1} | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| t_{CH} | Global clock high time | | 2.5 | | 3.0 | | ns |
| t_{CL} | Global clock low time | | 2.5 | | 3.0 | | ns |
| t_{ASU} | Array clock setup time | | 2.5 | | 3.0 | | ns |
| t_{AH} | Array clock hold time | | 2.0 | | 2.0 | | ns |
| t_{ACO1} | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| t_{ACH} | Array clock high time | | 3.0 | | 3.0 | | ns |
| t_{ACL} | Array clock low time | | 3.0 | | 3.0 | | ns |
| t_{CPPW} | Minimum pulse width for clear and preset | (3) | 3.0 | | 3.0 | | ns |
| t_{ODH} | Output data hold time after clock | C1 = 35 pF (4) | 1.0 | | 1.0 | | ns |
| t_{CNT} | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| f_{CNT} | Maximum internal global clock frequency | (5) | 151.5 | | 125.0 | | MHz |
| t_{ACNT} | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| f_{ACNT} | Maximum internal array clock frequency | (5) | 151.5 | | 125.0 | | MHz |
| f_{MAX} | Maximum clock frequency | (6) | 200 | | 166.7 | | MHz |

Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|------------|---|------------------|------------------|------|-----------------------------------|------|------|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| t_{IN} | Input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| t_{FIN} | Fast input delay | (2) | | 1.0 | | 1.0 | ns |
| t_{SEXP} | Shared expander delay | | | 5.0 | | 5.0 | ns |
| t_{PEXP} | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| t_{LAD} | Logic array delay | | | 5.0 | | 5.0 | ns |
| t_{LAC} | Logic control array delay | | | 5.0 | | 5.0 | ns |
| t_{IOE} | Internal output enable delay | (2) | | 2.0 | | 2.0 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 1.5 | | 2.0 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF (7) | | 2.0 | | 2.5 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF (2) | | 5.5 | | 6.0 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 5.0 | | 5.0 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF (7) | | 5.5 | | 5.5 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF (2) | | 9.0 | | 9.0 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5$ pF | | 5.0 | | 5.0 | ns |
| t_{SU} | Register setup time | | 2.0 | | 3.0 | | ns |
| t_H | Register hold time | | 3.0 | | 3.0 | | ns |
| t_{FSU} | Register setup time of fast input | (2) | 3.0 | | 3.0 | | ns |
| t_{FH} | Register hold time of fast input | (2) | 0.5 | | 0.5 | | ns |
| t_{RD} | Register delay | | | 2.0 | | 1.0 | ns |
| t_{COMB} | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| t_{IC} | Array clock delay | | | 5.0 | | 5.0 | ns |
| t_{EN} | Register enable time | | | 5.0 | | 5.0 | ns |
| t_{GLOB} | Global control delay | | | 1.0 | | 1.0 | ns |
| t_{PRE} | Register preset time | | | 3.0 | | 3.0 | ns |
| t_{CLR} | Register clear time | | | 3.0 | | 3.0 | ns |
| t_{PIA} | PIA delay | | | 1.0 | | 1.0 | ns |
| t_{LPA} | Low-power adder | (8) | | 11.0 | | 11.0 | ns |

Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|------------|---|----------------|------------------|------|-----------------------------------|------|------|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| t_{IN} | Input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| t_{FIN} | Fast input delay | (2) | | 1.0 | | 1.0 | ns |
| t_{SEXP} | Shared expander delay | | | 7.0 | | 7.0 | ns |
| t_{PEXP} | Parallel expander delay | | | 1.0 | | 1.0 | ns |
| t_{LAD} | Logic array delay | | | 7.0 | | 5.0 | ns |
| t_{LAC} | Logic control array delay | | | 5.0 | | 5.0 | ns |
| t_{IOE} | Internal output enable delay | (2) | | 2.0 | | 2.0 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V | C1 = 35 pF | | 1.0 | | 3.0 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V | C1 = 35 pF (7) | | 2.0 | | 4.0 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | C1 = 35 pF (2) | | 5.0 | | 7.0 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V | C1 = 35 pF (7) | | 7.0 | | 7.0 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | C1 = 35 pF (2) | | 10.0 | | 10.0 | ns |
| t_{XZ} | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | ns |
| t_{SU} | Register setup time | | 1.0 | | 4.0 | | ns |
| t_H | Register hold time | | 6.0 | | 4.0 | | ns |
| t_{FSU} | Register setup time of fast input | (2) | 4.0 | | 2.0 | | ns |
| t_{FH} | Register hold time of fast input | (2) | 0.0 | | 2.0 | | ns |
| t_{RD} | Register delay | | | 2.0 | | 1.0 | ns |
| t_{COMB} | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| t_{IC} | Array clock delay | | | 5.0 | | 5.0 | ns |
| t_{EN} | Register enable time | | | 7.0 | | 5.0 | ns |
| t_{GLOB} | Global control delay | | | 2.0 | | 0.0 | ns |
| t_{PRE} | Register preset time | | | 4.0 | | 3.0 | ns |
| t_{CLR} | Register clear time | | | 4.0 | | 3.0 | ns |
| t_{PIA} | PIA delay | | | 1.0 | | 1.0 | ns |
| t_{LPA} | Low-power adder | (8) | | 12.0 | | 12.0 | ns |

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 33 and 34 show the EPM7160S AC operating conditions.

| Table 33. EPM7160S External Timing Parameters (Part 1 of 2) Note (1) | | | | | | | | | | | |
|---|--|----------------|-------------|-----|-------|-----|-------|------|------|------|------|
| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| tPD1 | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| tPD2 | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| tSU | Global clock setup time | | 3.4 | | 4.2 | | 7.0 | | 11.0 | | ns |
| tH | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| tFSU | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| tFH | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.0 | | ns |
| tCO1 | Global clock to output delay | C1 = 35 pF | | 3.9 | | 4.8 | | 5 | | 8 | ns |
| tCH | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| tCL | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| tASU | Array clock setup time | | 0.9 | | 1.1 | | 2.0 | | 4.0 | | ns |
| tAH | Array clock hold time | | 1.7 | | 2.1 | | 3.0 | | 4.0 | | ns |
| tACO1 | Array clock to output delay | C1 = 35 pF | | 6.4 | | 7.9 | | 10.0 | | 15.0 | ns |
| tACH | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| tACL | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| tCPPW | Minimum pulse width for clear and preset | (2) | 2.5 | | 3.0 | | 4.0 | | 6.0 | | ns |
| tODH | Output data hold time after clock | C1 = 35 pF (3) | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| tCNT | Minimum global clock period | | | 6.7 | | 8.2 | | 10.0 | | 13.0 | ns |
| fCNT | Maximum internal global clock frequency | (4) | 149.3 | | 122.0 | | 100.0 | | 76.9 | | MHz |

Table 33. EPM7160S External Timing Parameters (Part 2 of 2) *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|-------------------|--|------------|-------------|-----|-------|-----|-------|------|-------|------|------|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{ACNT} | Minimum array clock period | | | 6.7 | | 8.2 | | 10.0 | | 13.0 | ns |
| f _{ACNT} | Maximum internal array clock frequency | (4) | 149.3 | | 122.0 | | 100.0 | | 76.9 | | MHz |
| f _{MAX} | Maximum clock frequency | (5) | 166.7 | | 166.7 | | 125.0 | | 100.0 | | MHz |

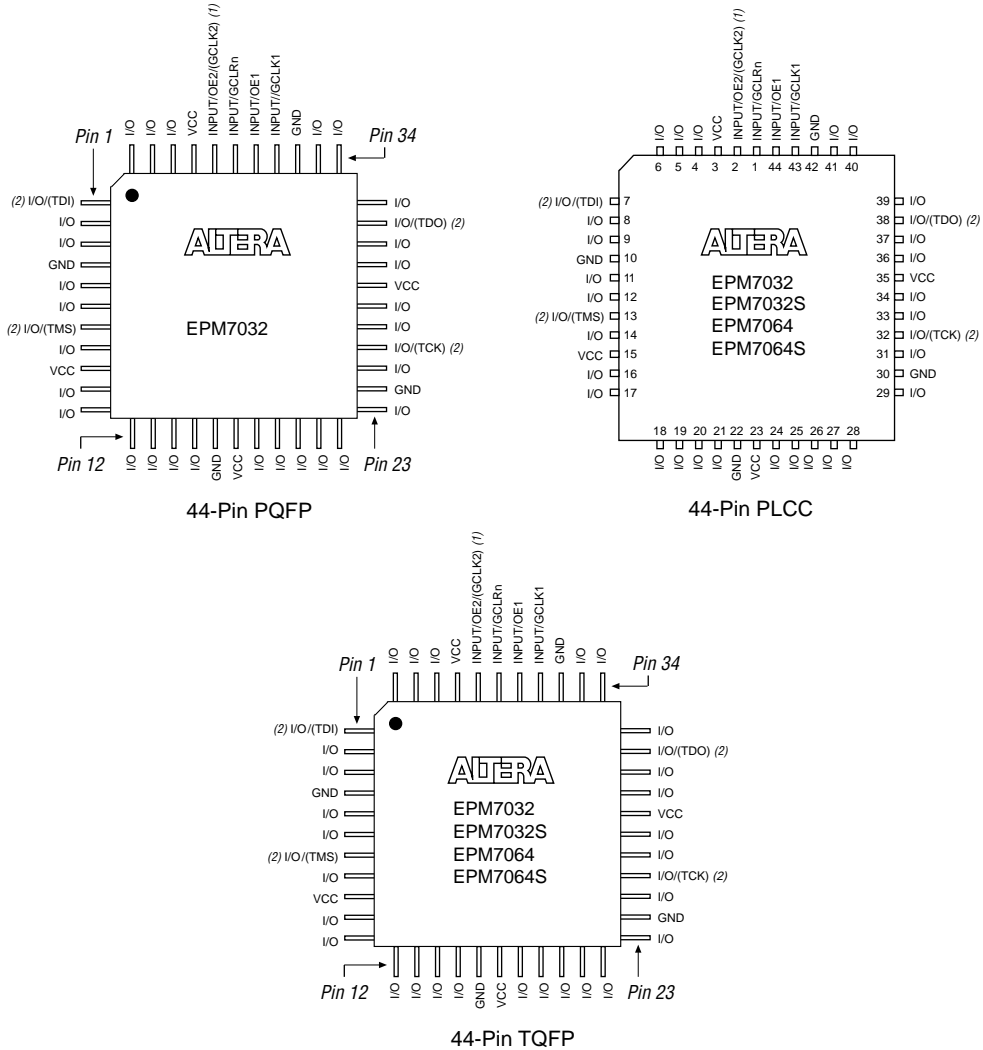
Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2) *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|------------|-----------------------------------|----------------|-------------|-----|-----|-----|-----|-----|-----|------|------|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{IN} | Input pad and buffer delay | | | 0.2 | | 0.3 | | 0.5 | | 2.0 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 0.2 | | 0.3 | | 0.5 | | 2.0 | ns |
| t_{FIN} | Fast input delay | | | 2.6 | | 3.2 | | 1.0 | | 2.0 | ns |
| t_{SEXP} | Shared expander delay | | | 3.6 | | 4.3 | | 5.0 | | 8.0 | ns |
| t_{PEXP} | Parallel expander delay | | | 1.0 | | 1.3 | | 0.8 | | 1.0 | ns |
| t_{LAD} | Logic array delay | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| t_{LAC} | Logic control array delay | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| t_{IOE} | Internal output enable delay | | | 0.7 | | 0.9 | | 2.0 | | 3.0 | ns |
| t_{OD1} | Output buffer and pad delay | C1 = 35 pF | | 0.4 | | 0.5 | | 1.5 | | 4.0 | ns |
| t_{OD2} | Output buffer and pad delay | C1 = 35 pF (6) | | 0.9 | | 1.0 | | 2.0 | | 5.0 | ns |
| t_{OD3} | Output buffer and pad delay | C1 = 35 pF | | 5.4 | | 5.5 | | 5.5 | | 8.0 | ns |
| t_{ZX1} | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| t_{ZX2} | Output buffer enable delay | C1 = 35 pF (6) | | 4.5 | | 4.5 | | 5.5 | | 7.0 | ns |
| t_{ZX3} | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 10.0 | ns |
| t_{XZ} | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| t_{SU} | Register setup time | | 1.0 | | 1.2 | | 2.0 | | 4.0 | | ns |
| t_H | Register hold time | | 1.6 | | 2.0 | | 3.0 | | 4.0 | | ns |
| t_{FSU} | Register setup time of fast input | | 1.9 | | 2.2 | | 3.0 | | 2.0 | | ns |
| t_{FH} | Register hold time of fast input | | 0.6 | | 0.8 | | 0.5 | | 1.0 | | ns |
| t_{RD} | Register delay | | | 1.3 | | 1.6 | | 2.0 | | 1.0 | ns |
| t_{COMB} | Combinatorial delay | | | 1.0 | | 1.3 | | 2.0 | | 1.0 | ns |
| t_{IC} | Array clock delay | | | 2.9 | | 3.5 | | 5.0 | | 6.0 | ns |
| t_{EN} | Register enable time | | | 2.8 | | 3.4 | | 5.0 | | 6.0 | ns |
| t_{GLOB} | Global control delay | | | 2.0 | | 2.4 | | 1.0 | | 1.0 | ns |
| t_{PRE} | Register preset time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |

Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

Figure 16. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.

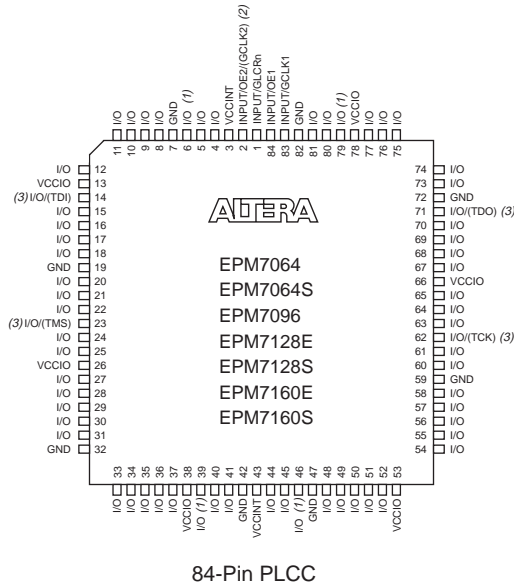


Notes:

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

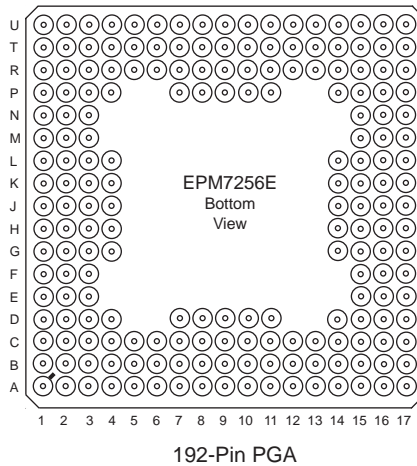


Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

Figure 21. 192-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

**Figure 22. 208-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

