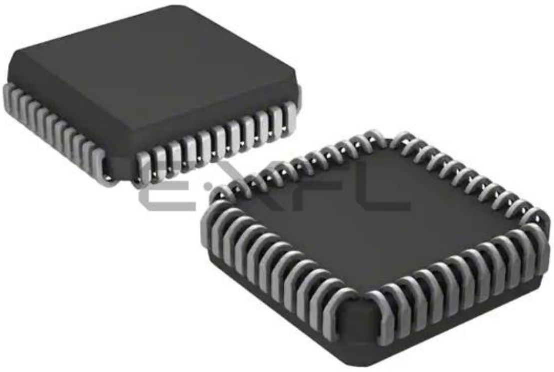
# Intel - EPM7064LC44-7YY Datasheet



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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | EE PLD |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | 1250 |
| Number of I/O | 36 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7064lc44-7yy |

*Table 2. MAX 7000S Device Features*

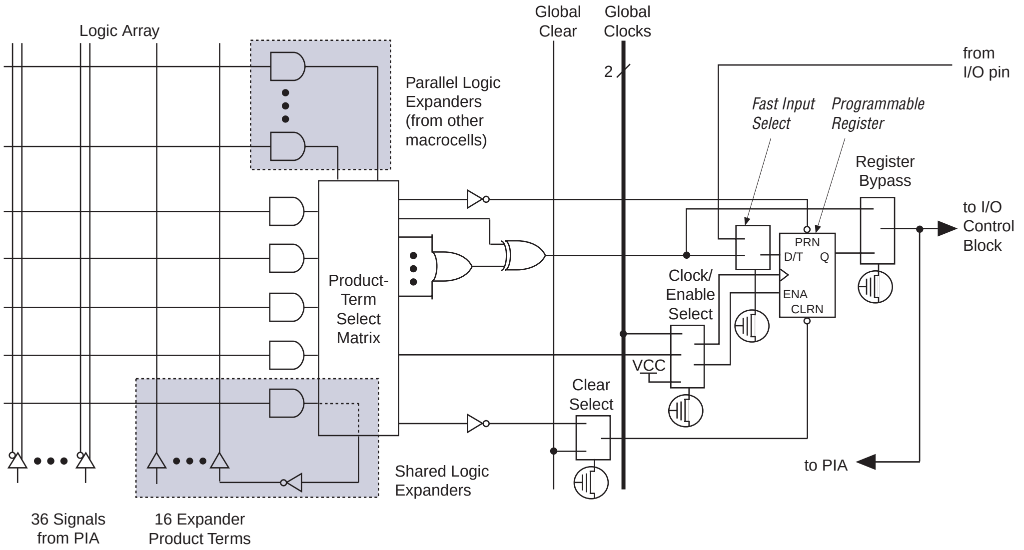
| Feature | EPM7032S | EPM7064S | EPM7128S | EPM7160S | EPM7192S | EPM7256S |
|---|---|---|---|---|---|---|
| Usable gates | 600 | 1,250 | 2,500 | 3,200 | 3,750 | 5,000 |
| Macrocells | 32 | 64 | 128 | 160 | 192 | 256 |
| Logic array blocks | 2 | 4 | 8 | 10 | 12 | 16 |
| Maximum user I/O pins | 36 | 68 | 100 | 104 | 124 | 164 |
| $t_{PD}$ (ns) | 5 | 5 | 6 | 6 | 7.5 | 7.5 |
| $t_{SU}$ (ns) | 2.9 | 2.9 | 3.4 | 3.4 | 4.1 | 3.9 |
| $t_{FSU}$ (ns) | 2.5 | 2.5 | 2.5 | 2.5 | 3 | 3 |
| $t_{CO1}$ (ns) | 3.2 | 3.2 | 4 | 3.9 | 4.7 | 4.7 |
| $f_{CNT}$ (MHz) | 175.4 | 175.4 | 147.1 | 149.3 | 125.0 | 128.2 |

## ...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

***Figure 4. MAX 7000E & MAX 7000S Device Macrocell***



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the `OR` and `XOR` gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

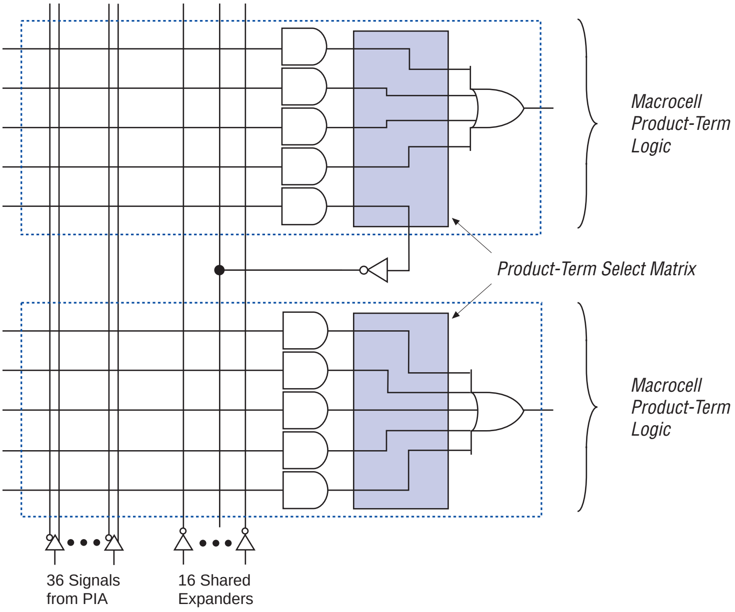
For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

### *Shareable Expanders*

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{SEXP}$) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

**Figure 5. Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### *Parallel Expanders*

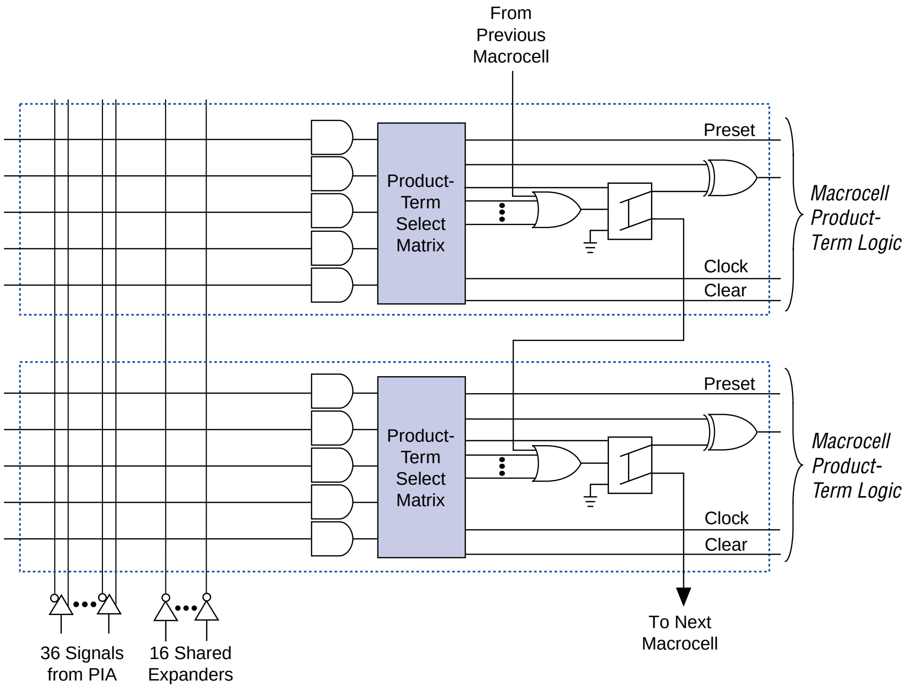
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell `OR` logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

***Figure 6. Parallel Expanders***

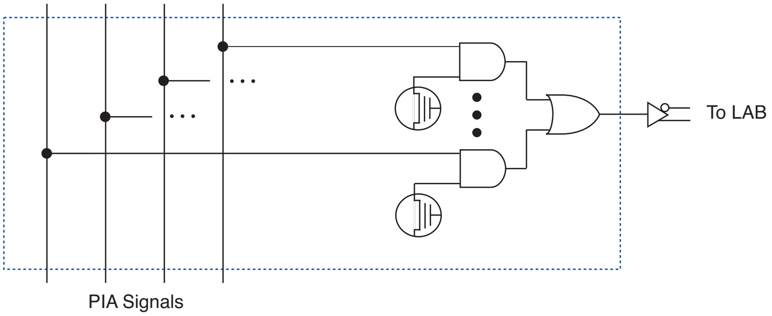
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input `AND` gate, which selects a PIA signal to drive into the LAB.

*Figure 7. PIA Routing*



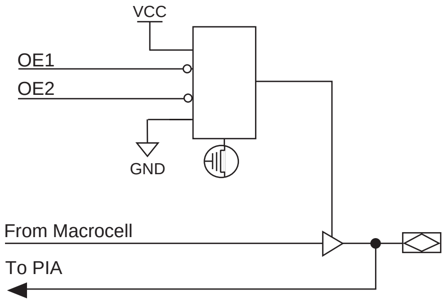
While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

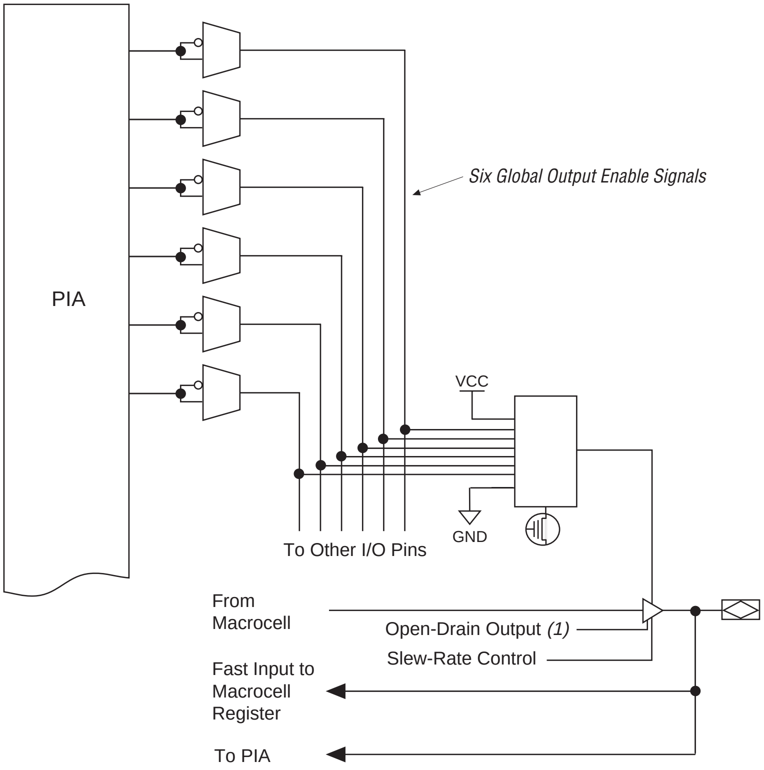
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (`OE1` and `OE2`). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

*Figure 8. I/O Control Block of MAX 7000 Devices*

**EPM7032, EPM7064 & EPM7096 Devices**



**MAX 7000E & MAX 7000S Devices**



*Note:*

(1) The open-drain output option is available only in MAX 7000S devices.

## Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

**Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to ground *(2)* | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Ceramic packages, under bias | | 150 | ° C |
| | | PQFP and RQFP packages, under bias | | 135 | ° C |

**Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3)*, *(4)*, *(5)* | 4.75<br>(4.50) | 5.25<br>(5.50) | V |
| $V_{CCIO}$ | Supply voltage for output drivers, 5.0-V operation | *(3)*, *(4)* | 4.75<br>(4.50) | 5.25<br>(5.50) | V |
| | Supply voltage for output drivers, 3.3-V operation | *(3)*, *(4)*, *(6)* | 3.00<br>(3.00) | 3.60<br>(3.60) | V |
| $V_{CCISP}$ | Supply voltage during ISP | *(7)* | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | –0.5 *(8)* | $V_{CCINT}$ + 0.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_A$ | Ambient temperature | For commercial use | 0 | 70 | ° C |
| | | For industrial use | –40 | 85 | ° C |
| $T_J$ | Junction temperature | For commercial use | 0 | 90 | ° C |
| | | For industrial use | –40 | 105 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

*Table 19. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | | 5.0 | | 6.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| $t_{CH}$ | Global clock high time | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.5 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.5 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.0 | | 2.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 3.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 200 | | 166.7 | | MHz |

**Table 21. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10)<br>MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 8.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 5.0 | | 5 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.0 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 3.0 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 4.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 4.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 4.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 10.0 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 10.0 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

***Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10)<br>MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| $t_{FIN}$ | Fast input delay | (2) | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 5.0 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 5.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | (2) | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.5 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF (7) | | 2.0 | | 2.5 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF (2) | | 5.5 | | 6.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 5.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF (7) | | 5.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF (2) | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 5.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 2.0 | | 3.0 | | ns |
| $t_{H}$ | Register hold time | | 3.0 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | (2) | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | (2) | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 5.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 3.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 3.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | (8) | | 11.0 | | 11.0 | ns |

***Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12)<br>MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 7.0 | | 7.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 7.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.0 | | 3.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.0 | | 4.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 5.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 6.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 4.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.0 | | 2.0 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 7.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 0.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 12.0 | ns |

**Table 25. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{SU}$ | Global clock setup time | | 11.0 | | 11.0 | | 12.0 | | ns |
| $t_H$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | – | | 5.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.0 | | – | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 8.0 | | 8.0 | | 12.0 | ns |
| $t_{CH}$ | Global clock high time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{CL}$ | Global clock low time | | 5.0 | | 6.0 | | 6.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 15.0 | | 15.0 | | 20.0 | ns |
| $t_{ACH}$ | Array clock high time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 6.0 | | 6.5 | | 8.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 13.0 | | 13.0 | | 16.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 76.9 | | 76.9 | | 62.5 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 100 | | 83.3 | | 83.3 | | MHz |

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.1 | | 1.4 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 10.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO} = 3.3$ V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

**Table 29. EPM7064S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 2.9 | | 3.6 | | 6.0 | | 7.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 4.0 | | 4.5 | | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.7 | | 0.9 | | 3.0 | | 2.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.0 | | 3.0 | | ns |

| Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2) Note (1) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.0 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.3 | | 3.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.2 | | 3.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.9 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 2.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.3 | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 11.0 | | 10.0 | | 11.0 | ns |

***Notes to tables:***

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

**Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.6 | | 2.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

**Table 35. EPM7192S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 4.1 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 1.0 | | 2.0 | | 4.0 | | ns |

**Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{H}$ | Register hold time | | 1.7 | | 3.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 2.3 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.7 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.2 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.2 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.1 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.5 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.7 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 2.4 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 11.0 | | 13.0 | ns |

***Notes to tables:***

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

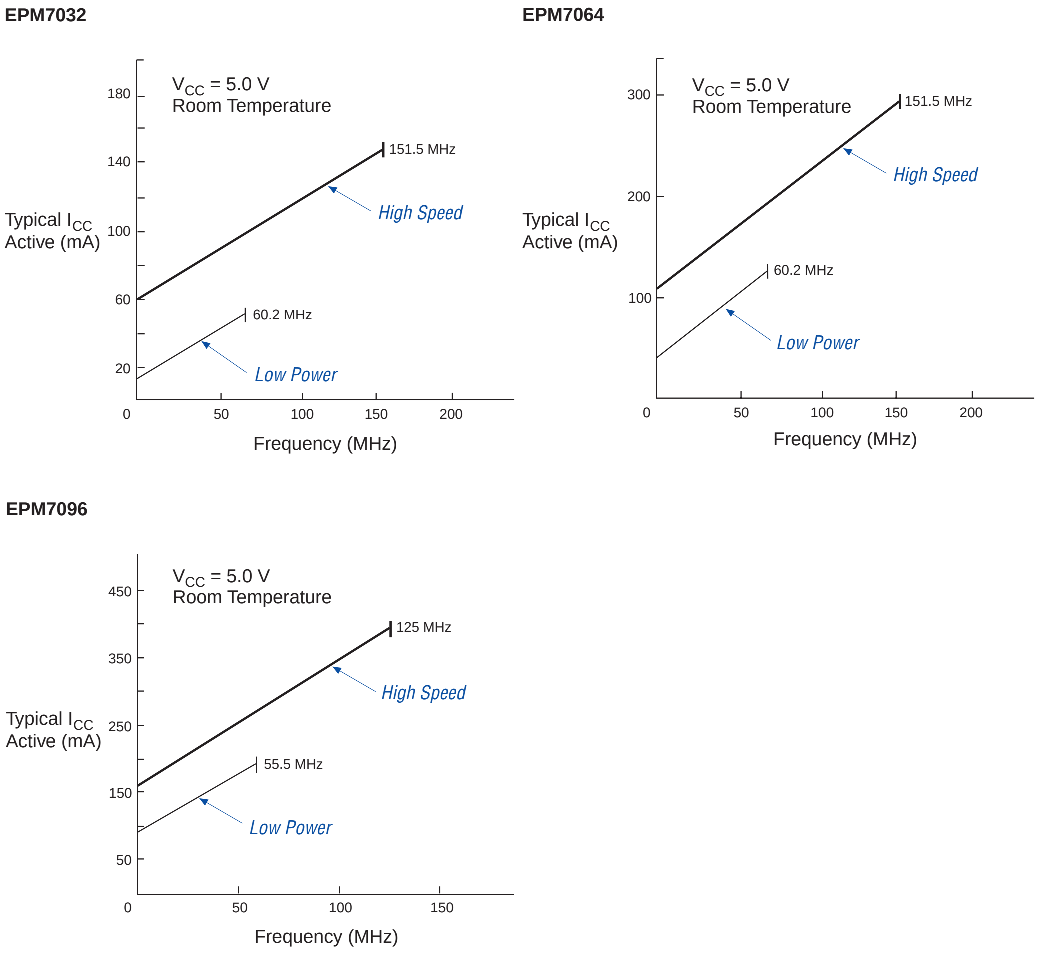
(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

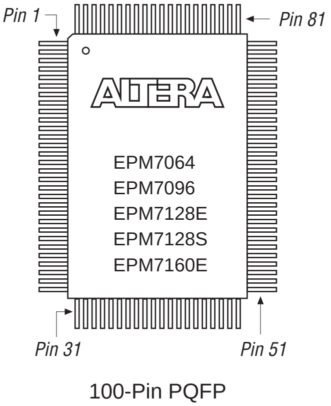
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 1 of 2)*

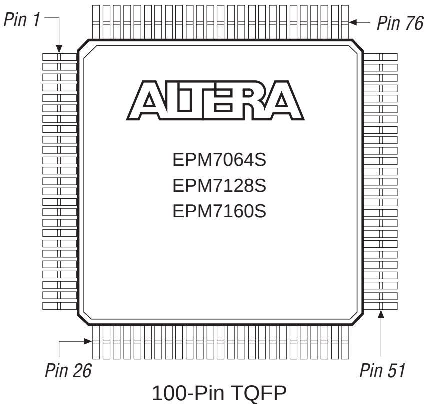


### Figure 19. 100-Pin Package Pin-Out Diagram

*Package outline not drawn to scale.*



100-Pin PQFP



100-Pin TQFP

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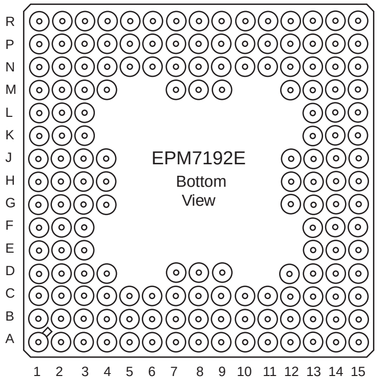
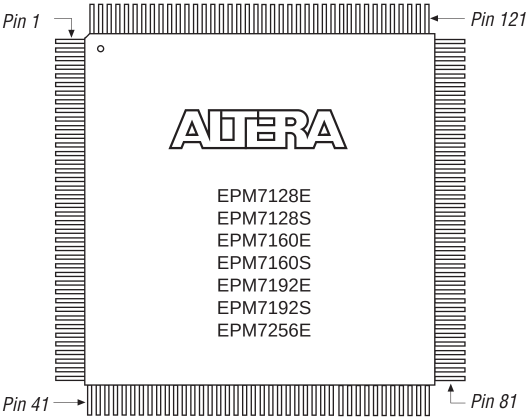
### Figure 20. 160-Pin Package Pin-Out Diagram

*Package outline not drawn to scale.*



160-Pin PGA



160-Pin PQFP

## *Notes:*

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