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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064lc84-15

Table 2. MAX 7000S Device Features

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t_{PD} (ns)	5	5	6	6	7.5	7.5
t_{SU} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f_{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification*, *Revision 2.2***. See Table 3 for available speed grades.

Table 3. MAX 7000 Speed Grades

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

Table 4. MAX 7000 Device Features

Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface *(2)*	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:

(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.

(2) The MultiVolt I/O interface is not available in 44-pin packages.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

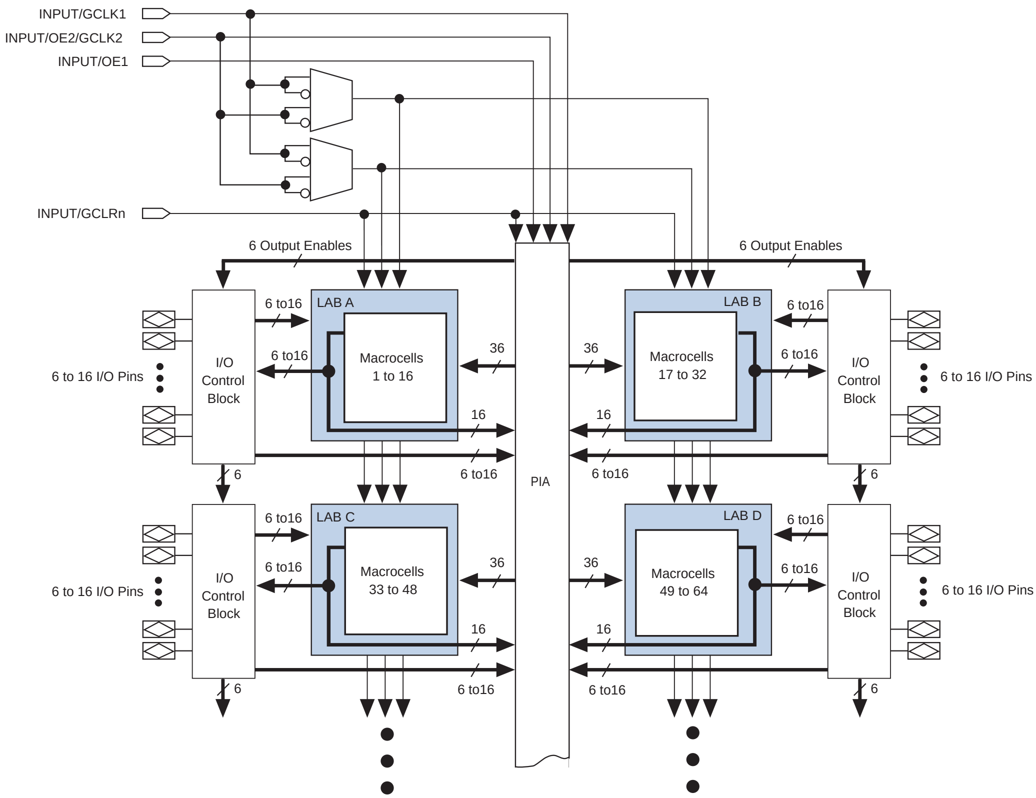
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

The programming times described in Tables 6 through 8 are associated with the worst-case method using the enhanced ISP algorithm.

Table 6. MAX 7000S t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PPULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

Tables 7 and 8 show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see the *Programming Hardware Manufacturers*.

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

Table 10. MAX 7000S Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032S	1 *(1)*
EPM7064S	1 *(1)*
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

Note:

(1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

Table 11. 32-Bit MAX 7000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

Notes:

(1) The most significant bit (MSB) is on the left.

(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Figure 9 shows the timing requirements for the JTAG signals.

Figure 9. MAX 7000 JTAG Waveforms

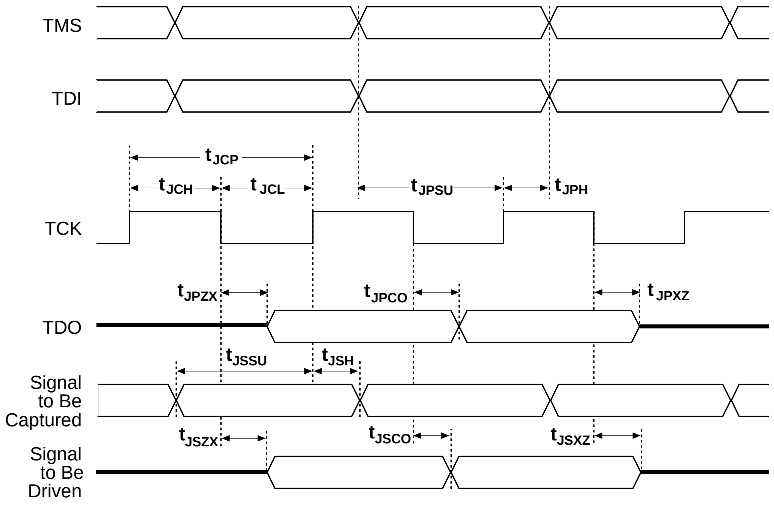


Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

Table 12. JTAG Timing Parameters & Values for MAX 7000S Devices				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

For more information, see *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

Design Security

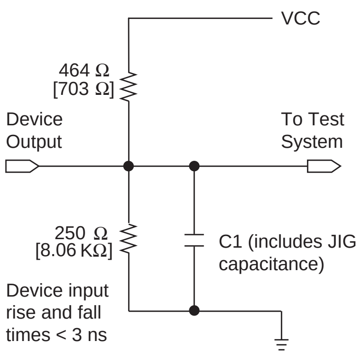
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 10. Test patterns can be used and then erased during early stages of the production flow.

Figure 10. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.

For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet*.

MAX 7000S devices are not shipped in carriers.

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5 *(8)*	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(10)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(10)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.0 V *(10)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(11)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V*(11)*		0.2	V
I_I	Leakage current of dedicated input pins	V_I = –0.5 to 5.5 V *(11)*	–10	10	μA
I_{OZ}	I/O pin tri-state output off-state current	V_I = –0.5 to 5.5 V *(11)*, *(12)*	–40	40	μA

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Dedicated input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Figure 13. Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

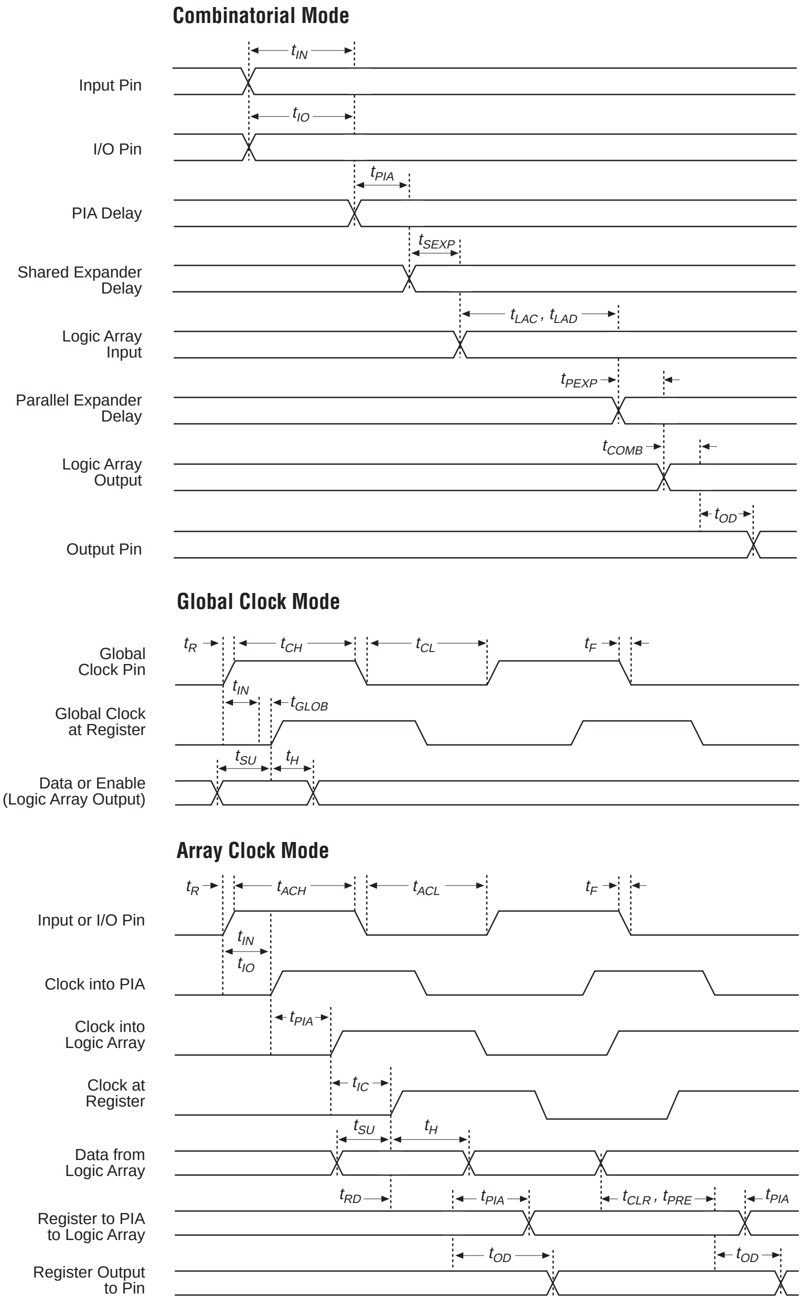


Table 25. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{SU}	Global clock setup time		11.0		11.0		12.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		–		5.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.0		–		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t_{CH}	Global clock high time		5.0		6.0		6.0		ns
t_{CL}	Global clock low time		5.0		6.0		6.0		ns
t_{ASU}	Array clock setup time		4.0		4.0		5.0		ns
t_{AH}	Array clock hold time		4.0		4.0		5.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t_{ACH}	Array clock high time		6.0		6.5		8.0		ns
t_{ACL}	Array clock low time		6.0		6.5		8.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	6.0		6.5		8.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			13.0		13.0		16.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	76.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13.0		13.0		16.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	76.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*(6)*	100		83.3		83.3		MHz

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	*(2)*		2.0		–		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	*(2)*		3.0		–		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.0		–		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		8.0		–		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		–		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		–		14.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_H	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	2.0		–		4.0		ns
t_{FH}	Register hold time of fast input	*(2)*	2.0		–		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	*(8)*		13.0		15.0		15.0	ns

Table 27. EPM7032S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
f_{ACNT}	Maximum internal array clock frequency	*(4)*	175.4		142.9		116.3		100.0		MHz
f_{MAX}	Maximum clock frequency	*(5)*	250.0		200.0		166.7		125.0		MHz

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		2.1		2.5		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.6		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		1.4		0.8	ns
t_{LAD}	Logic array delay			2.6		3.3		4.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.3		4.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		1.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		0.4		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(6)*		0.7		0.8		0.9		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		5.4		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(6)*		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		1.3		2.0		ns
t_{H}	Register hold time		1.7		2.0		2.5		3.0		ns
t_{FSU}	Register setup time of fast input		1.9		1.8		1.7		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.8		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.9		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.1		1.4		2.0	ns
t_{IC}	Array clock delay			2.7		3.4		4.2		5.0	ns
t_{EN}	Register enable time			2.6		3.3		4.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.4		1.7		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		3.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		3.0		3.0	ns

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t_{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t_{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t_{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 33. EPM7160S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACNT}	Minimum array clock period			6.7		8.2		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	149.3		122.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(5)*	166.7		166.7		125.0		100.0		MHz

Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.6		4.3		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.3		0.8		1.0	ns
t_{LAD}	Logic array delay			2.8		3.4		5.0		6.0	ns
t_{LAC}	Logic control array delay			2.8		3.4		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(6)*		0.9		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(6)*		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		1.2		2.0		4.0		ns
t_{H}	Register hold time		1.6		2.0		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
t_{RD}	Register delay			1.3		1.6		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.3		2.0		1.0	ns
t_{IC}	Array clock delay			2.9		3.5		5.0		6.0	ns
t_{EN}	Register enable time			2.8		3.4		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		2.4		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		3.0		3.0		4.0	ns

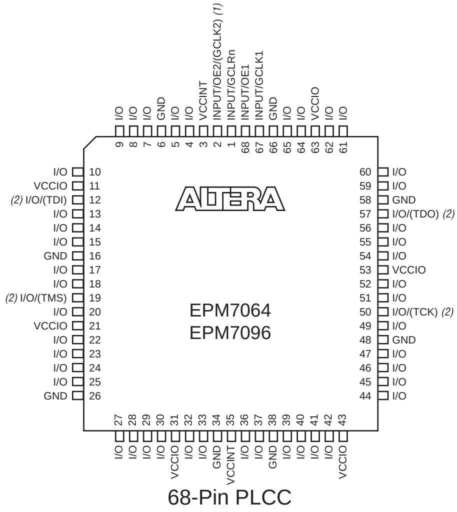
Table 39. MAX 7000 I_{CC} Equation Constants

Device	A	B	C
EPM7032	1.87	0.52	0.144
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S	0.93	0.40	0.040
EPM7064S	0.93	0.40	0.040
EPM7128S	0.93	0.40	0.040
EPM7160S	0.93	0.40	0.040
EPM7192S	0.93	0.40	0.040
EPM7256S	0.93	0.40	0.040

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.

(2) JTAG ports are available in MAX 7000S devices only.

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