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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	EE PLD
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm7064qc100-10

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

Table 4. MAX 7000 Device Features

Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface *(2)*	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:
(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

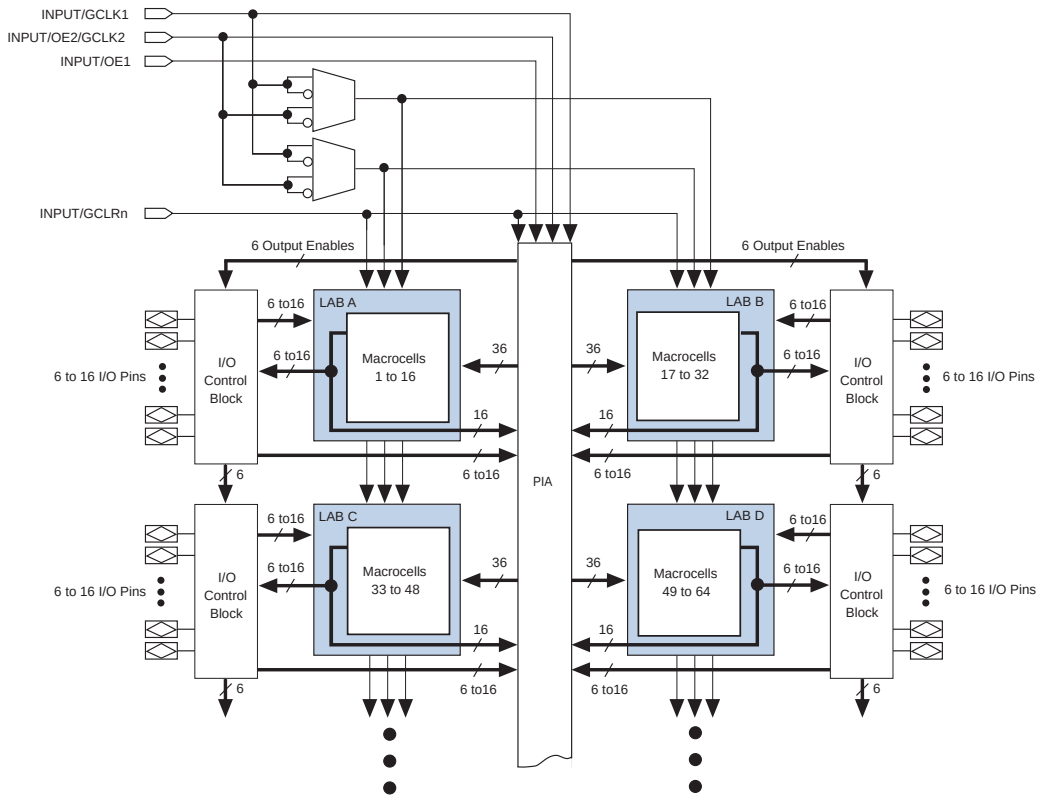
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram

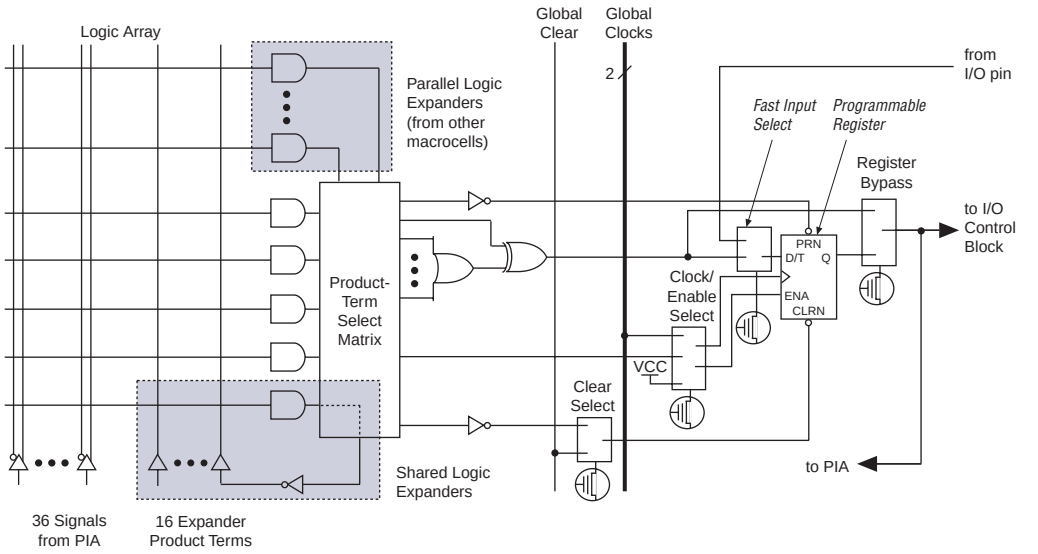


Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

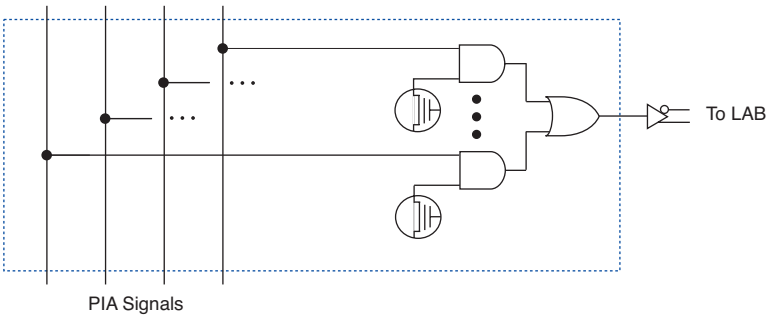
The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



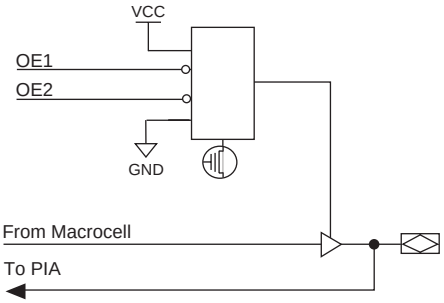
While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

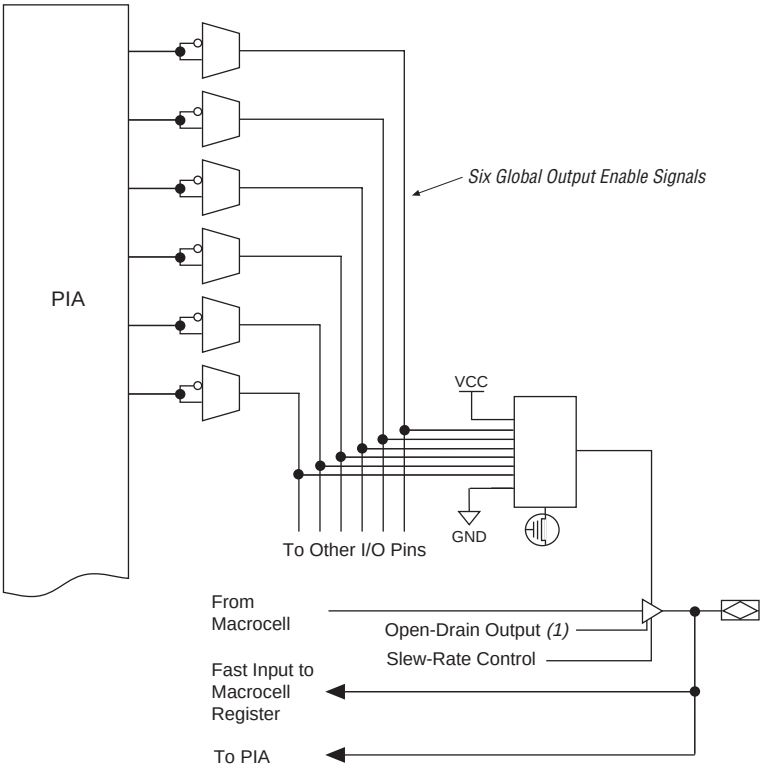
The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7064 & EPM7096 Devices



MAX 7000E & MAX 7000S Devices



Note:
(1) The open-drain output option is available only in MAX 7000S devices.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k¾.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000S Device

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

Table 10. MAX 7000S Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032S	1 *(1)*
EPM7064S	1 *(1)*
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

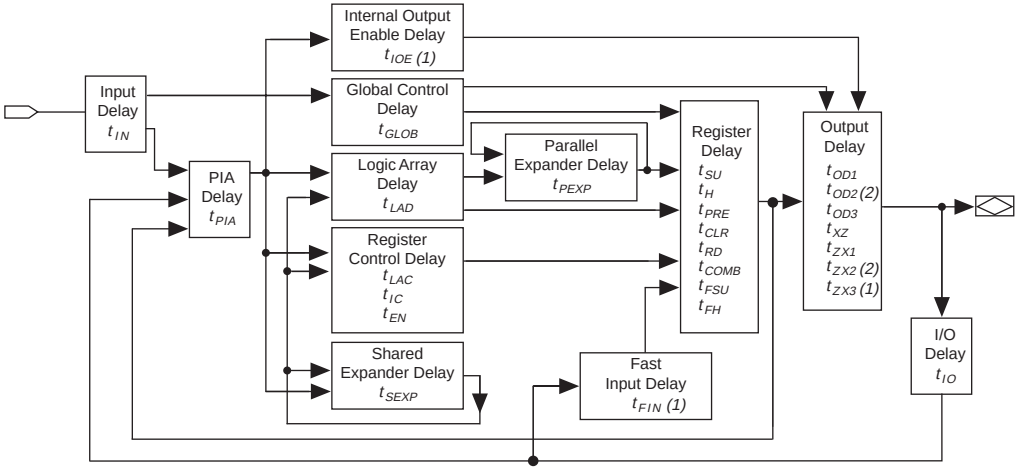
Note:
(1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

Table 11. 32-Bit MAX 7000 Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Figure 12. MAX 7000 Timing Model



Notes:
(1) Only available in MAX 7000E and MAX 7000S devices.
(2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.

For more infomration, see *Application Note 94 (Understanding MAX 7000 Timing)*.

Figure 13. Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

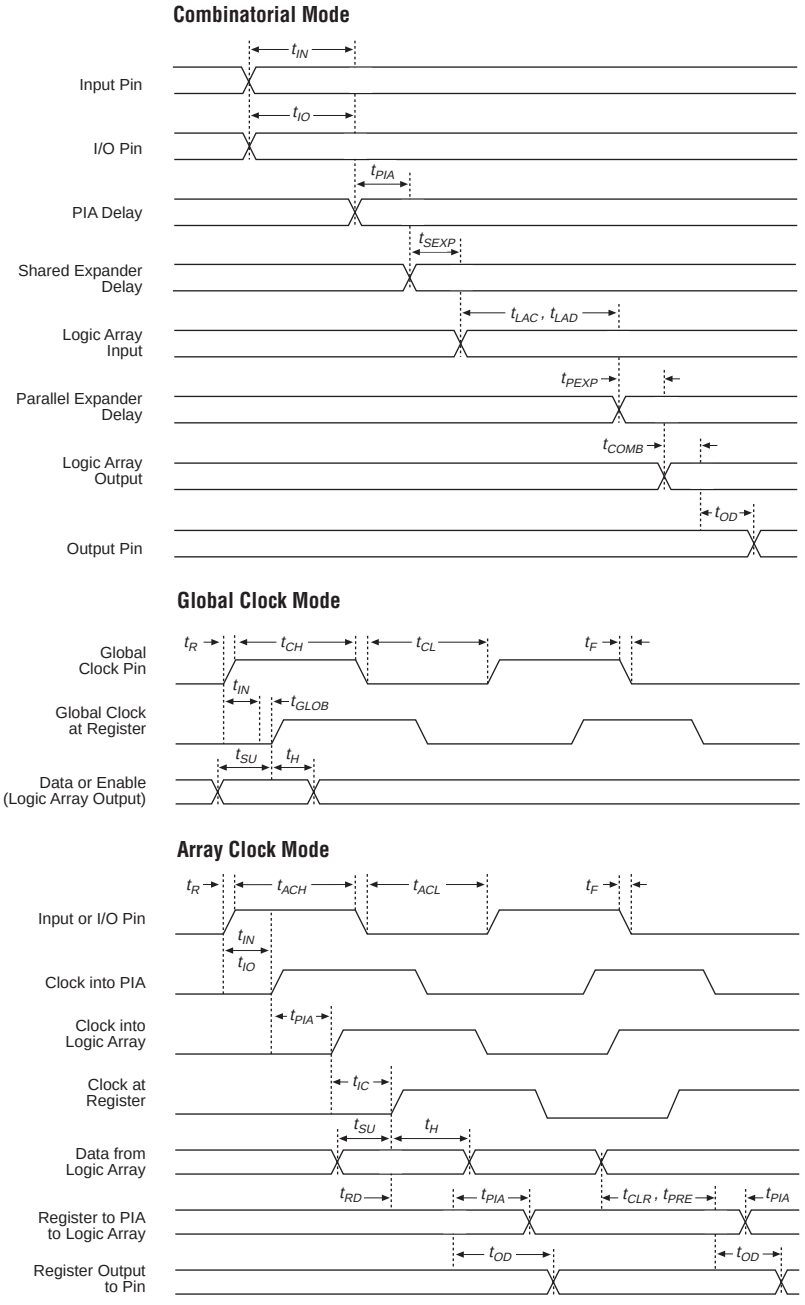


Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.5		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.5		1.0	ns
t_{FIN}	Fast input delay	*(2)*		1.0		1.0	ns
t_{SEXP}	Shared expander delay			5.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	*(2)*		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		1.5		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.0		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		5.5		6.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		5.0	ns
t_{SU}	Register setup time		2.0		3.0		ns
t_{H}	Register hold time		3.0		3.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.5		0.5		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			5.0		5.0	ns
t_{GLOB}	Global control delay			1.0		1.0	ns
t_{PRE}	Register preset time			3.0		3.0	ns
t_{CLR}	Register clear time			3.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	*(8)*		11.0		11.0	ns

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	*(2)*		2.0		–		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	*(2)*		3.0		–		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.0		–		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		8.0		–		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		–		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		–		14.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_{H}	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	2.0		–		4.0		ns
t_{FH}	Register hold time of fast input	*(2)*	2.0		–		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	*(8)*		13.0		15.0		15.0	ns

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t_{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t_{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(2)*	2.5		2.5		3.0		4.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	175.4		140.8		125.0		100.0		MHz
t_{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	175.4		140.8		125.0		100.0		MHz
f_{MAX}	Maximum clock frequency	*(5)*	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(6)*		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(6)*		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_{H}	Register hold time		1.7		2.0		2.0		3.0		ns

Tables 31 and 32 show the EPM7128S AC operating conditions.

Table 31. EPM7128S External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t_{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(2)*	3.0		3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	147.1		125.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	147.1		125.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(5)*	166.7		166.7		125.0		100.0		MHz

Table 35. EPM7192S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{AH}	Array clock hold time		1.8		3.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(2)*	3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			8.0		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	125.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			8.0		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	125.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(5)*	166.7		125.0		100.0		MHz

Table 36. EPM7192S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			4.2		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.2		0.8		1.0	ns
t_{LAD}	Logic array delay			3.1		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.1		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(6)*		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		7.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(6)*		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.1		2.0		4.0		ns

Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_H	Register hold time		1.7		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		2.3		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.7		0.5		1.0		ns
t_{RD}	Register delay			1.4		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.2		2.0		1.0	ns
t_{IC}	Array clock delay			3.2		5.0		6.0	ns
t_{EN}	Register enable time			3.1		5.0		6.0	ns
t_{GLOB}	Global control delay			2.5		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	*(7)*		2.4		1.0		2.0	ns
t_{LPA}	Low-power adder	*(8)*		10.0		11.0		13.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

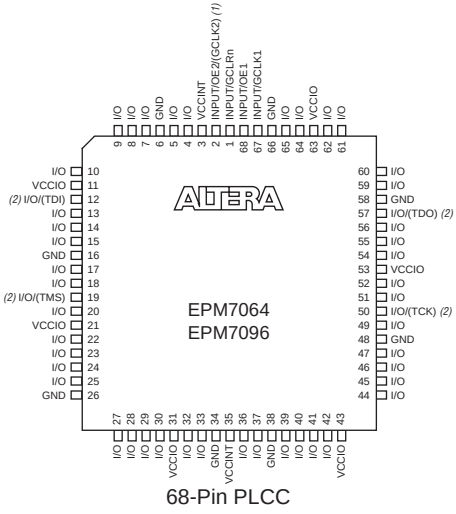
Tables 37 and 38 show the EPM7256S AC operating conditions.

Table 37. EPM7256S External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		3.9		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t_{AH}	Array clock hold time		1.9		3.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(2)*	3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(3)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			7.8		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	*(4)*	128.2		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			7.8		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(4)*	128.2		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	*(5)*	166.7		125.0		100.0		MHz

Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.

(2) JTAG ports are available in MAX 7000S devices only.

Notes: