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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

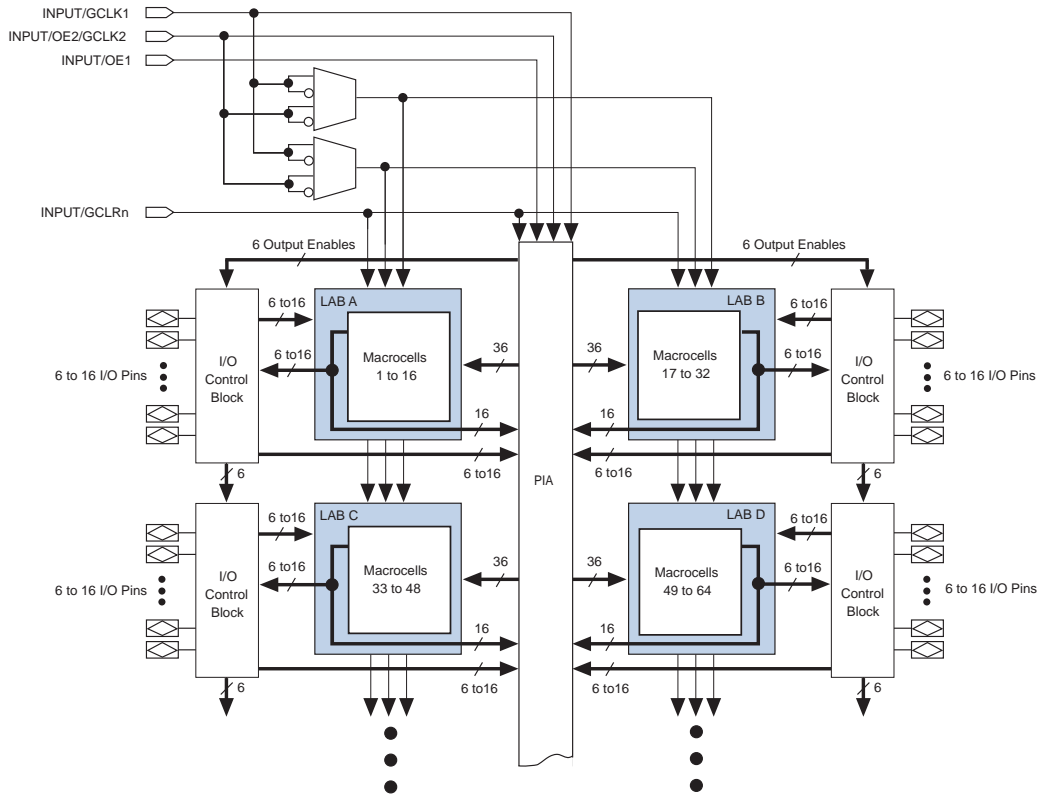
Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	36
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7064slc44-5n

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

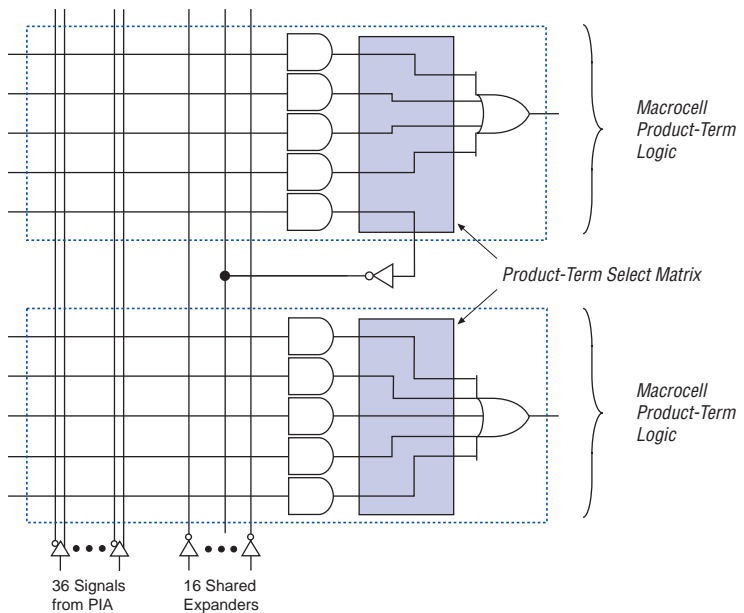
The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.

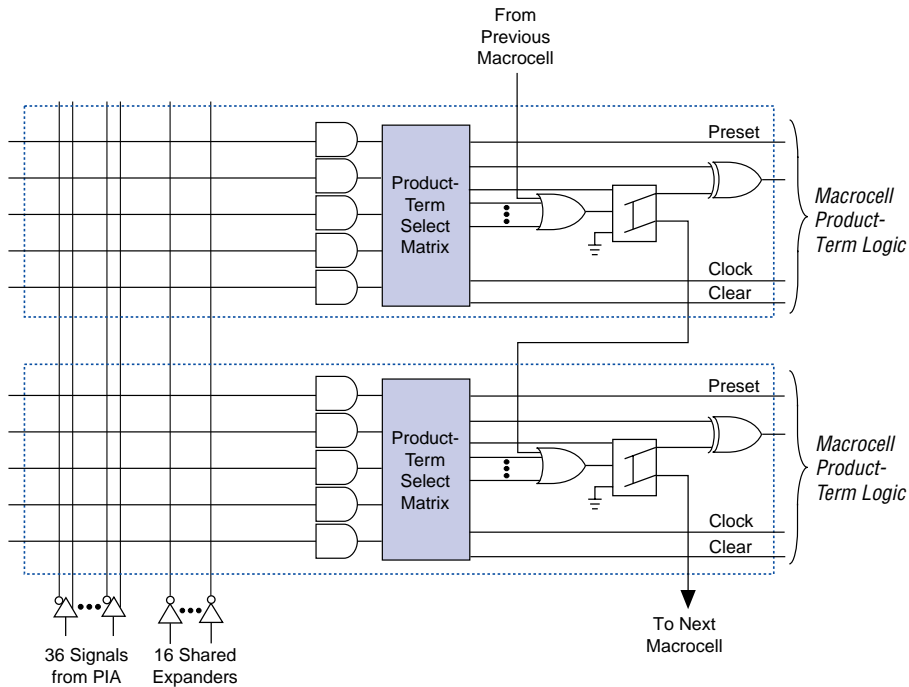
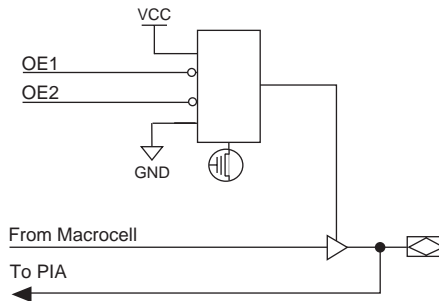
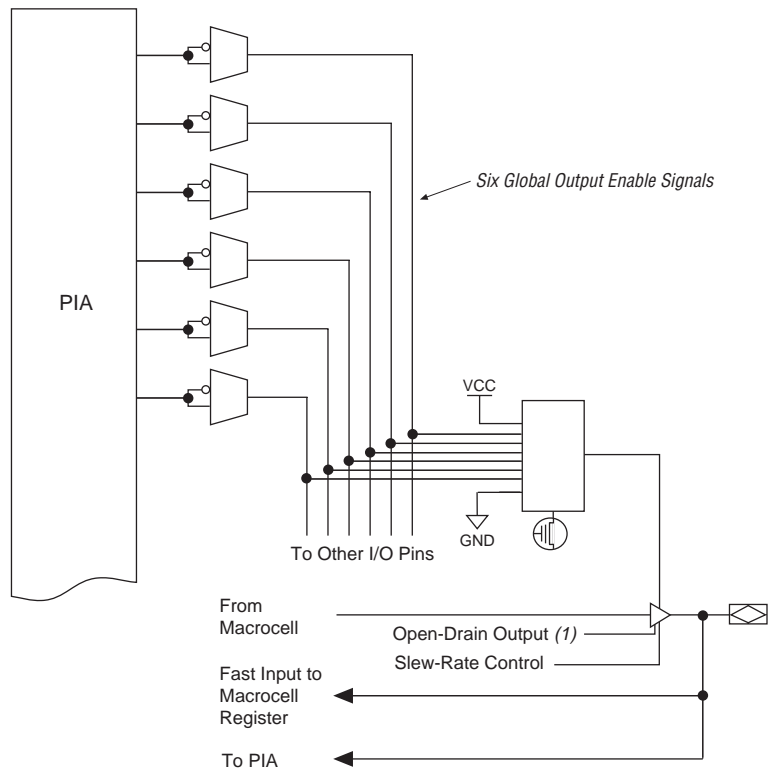


Figure 8. I/O Control Block of MAX 7000 Devices**EPM7032, EPM7064 & EPM7096 Devices****MAX 7000E & MAX 7000S Devices****Note:**

- (1) The open-drain output option is available only in MAX 7000S devices.

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , and t_{SEXP} , t_{ACL} , and t_{CPPW} parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} .

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5 (8)	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V (10)	$V_{CCIO} - 0.2$		V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (11)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V (11)		0.2	V
I_I	Leakage current of dedicated input pins	$V_I = -0.5$ to 5.5 V (11)	-10	10	μ A
I_{OZ}	I/O pin tri-state output off-state current	$V_I = -0.5$ to 5.5 V (11), (12)	-40	40	μ A

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*

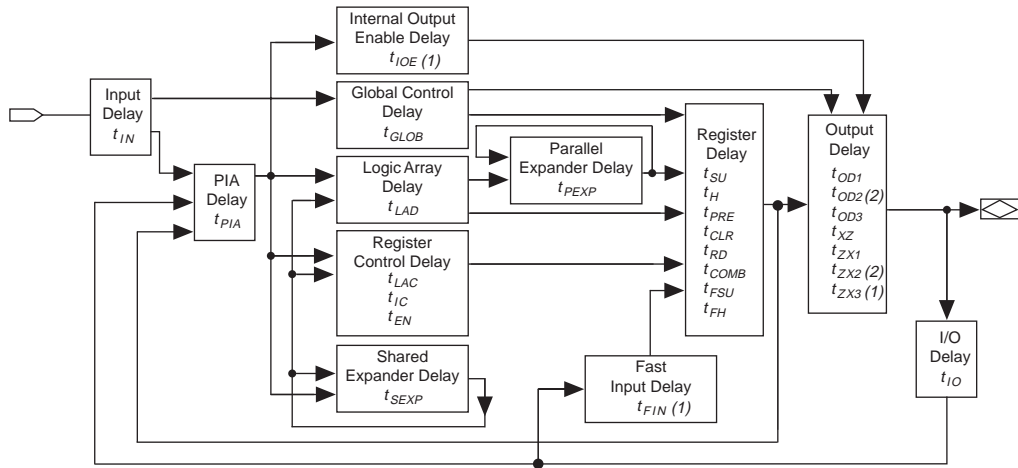
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Figure 12. MAX 7000 Timing Model**Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).

Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.5		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.5		1.0	ns
t_{FIN}	Fast input delay	(2)		1.0		1.0	ns
t_{SEXP}	Shared expander delay			5.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	(2)		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.5		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.5		6.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		5.0		5.0	ns
t_{SU}	Register setup time		2.0		3.0		ns
t_H	Register hold time		3.0		3.0		ns
t_{FSU}	Register setup time of fast input	(2)	3.0		3.0		ns
t_{FH}	Register hold time of fast input	(2)	0.5		0.5		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			5.0		5.0	ns
t_{GLOB}	Global control delay			1.0		1.0	ns
t_{PRE}	Register preset time			3.0		3.0	ns
t_{CLR}	Register clear time			3.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		11.0		11.0	ns

Table 23. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{SU}	Global clock setup time		7.0		10.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		3.0		4.0		ns
t _{AH}	Array clock hold time		4.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t _{ACH}	Array clock high time		5.0		5.0		ns
t _{ACL}	Array clock low time		5.0		5.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			11.0		11.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t _{ACNT}	Minimum array clock period			11.0		11.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 25. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t _{SU}	Global clock setup time		11.0		11.0		12.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		–		5.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.0		–		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t _{CH}	Global clock high time		5.0		6.0		6.0		ns
t _{CL}	Global clock low time		5.0		6.0		6.0		ns
t _{ASU}	Array clock setup time		4.0		4.0		5.0		ns
t _{AH}	Array clock hold time		4.0		4.0		5.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t _{ACH}	Array clock high time		6.0		6.5		8.0		ns
t _{ACL}	Array clock low time		6.0		6.5		8.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	6.0		6.5		8.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			13.0		13.0		16.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	76.9		76.9		62.5		MHz
t _{ACNT}	Minimum array clock period			13.0		13.0		16.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	76.9		76.9		62.5		MHz
f _{MAX}	Maximum clock frequency	(6)	100		83.3		83.3		MHz

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	(2)		2.0		–		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	(2)		3.0		–		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		5.0		–		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$ (2)		8.0		–		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		7.0		–		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$ (2)		10.0		–		14.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_H	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	(2)	2.0		–		4.0		ns
t_{FH}	Register hold time of fast input	(2)	2.0		–		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	(8)		13.0		15.0		15.0	ns

Tables 31 and 32 show the EPM7128S AC operating conditions.

Table 31. EPM7128S External Timing Parameters Note (1)											
Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t _{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Table 33. EPM7160S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACNT}	Minimum array clock period			6.7		8.2		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	149.3		122.0		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.6		4.3		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.3		0.8		1.0	ns
t_{LAD}	Logic array delay			2.8		3.4		5.0		6.0	ns
t_{LAC}	Logic control array delay			2.8		3.4		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.9		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		1.2		2.0		4.0		ns
t_H	Register hold time		1.6		2.0		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
t_{RD}	Register delay			1.3		1.6		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.3		2.0		1.0	ns
t_{IC}	Array clock delay			2.9		3.5		5.0		6.0	ns
t_{EN}	Register enable time			2.8		3.4		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		2.4		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		3.0		3.0		4.0	ns

Tables 37 and 38 show the EPM7256S AC operating conditions.

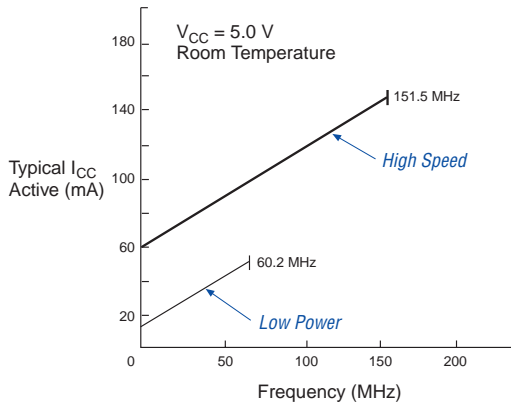
Table 37. EPM7256S External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.9		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t _{AH}	Array clock hold time		1.9		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			7.8		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			7.8		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

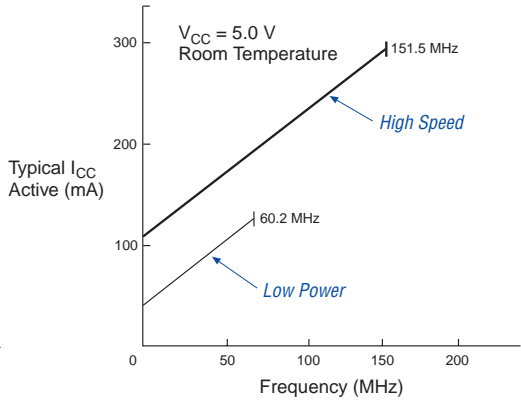
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

EPM7032



EPM7064



EPM7096

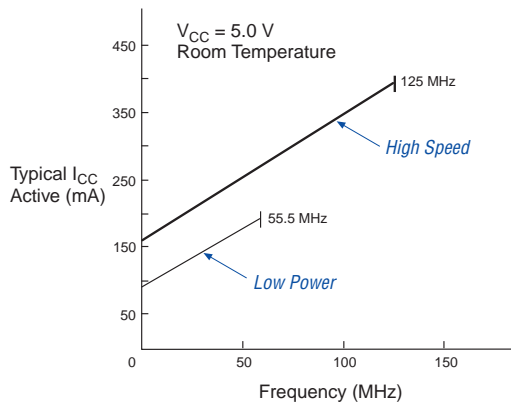
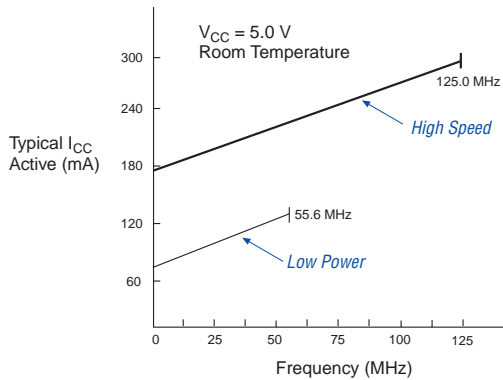
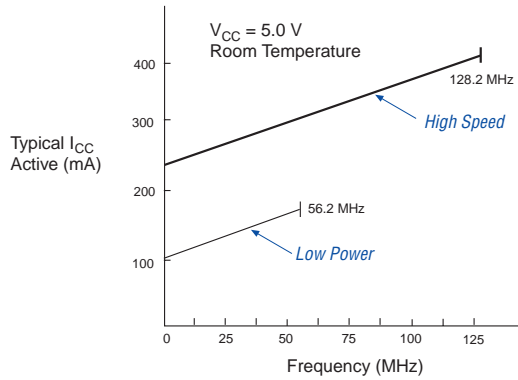


Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)

EPM7192S

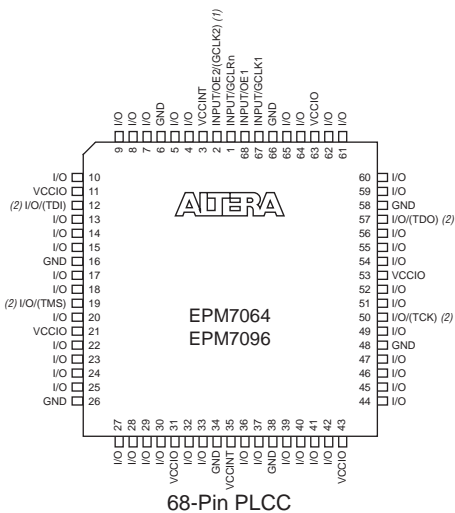


EPM7256S



Device Pin-Outs

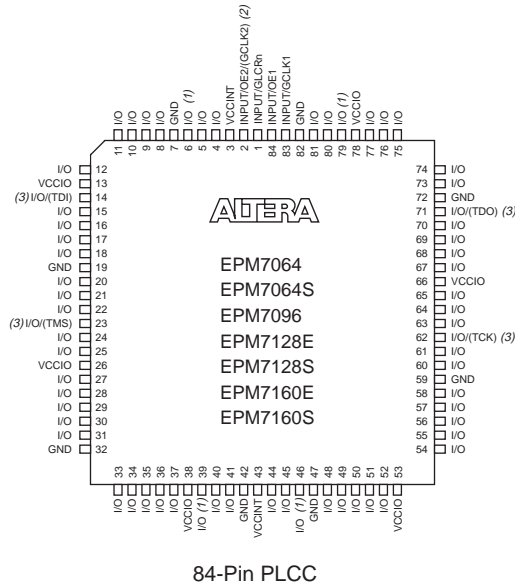
See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figure 17. 68-Pin Package Pin-Out Diagram*Package outlines not drawn to scale.***Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

Figure 19. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

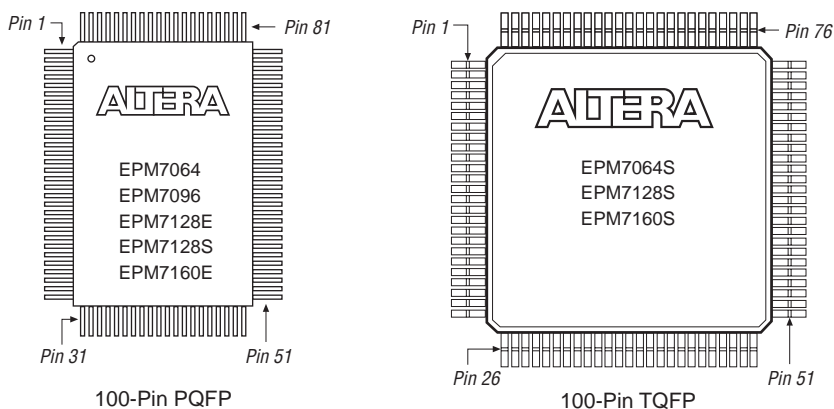
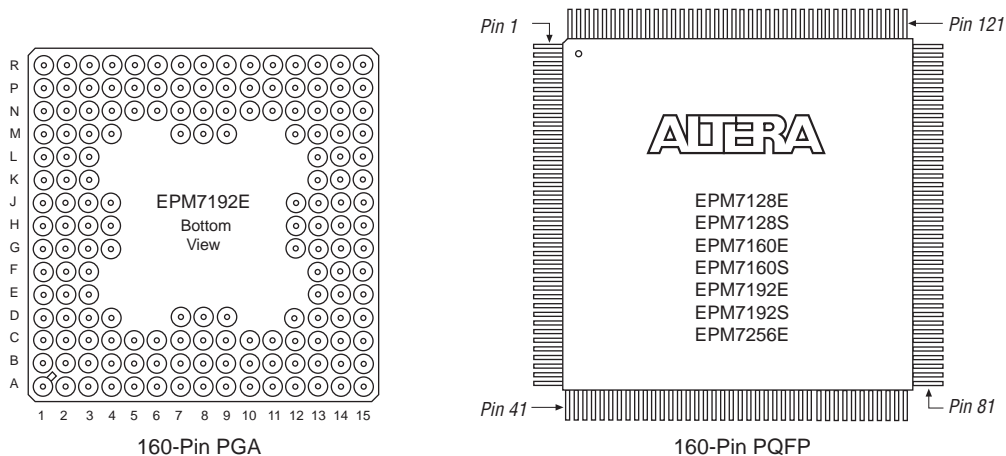


Figure 20. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.





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