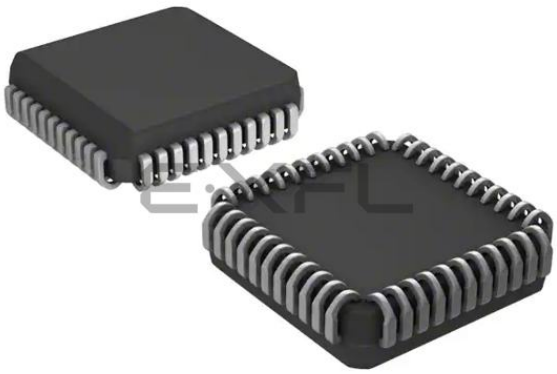

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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 7.5 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 4 |
| Number of Macrocells | 64 |
| Number of Gates | 1250 |
| Number of I/O | 36 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7064slc44-7 |

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

*Table 4. MAX 7000 Device Features*

| Feature | EPM7032 EPM7064 EPM7096 | All MAX 7000E Devices | All MAX 7000S Devices |
|---|---|---|---|
| ISP via JTAG interface | | | ✓ |
| JTAG BST circuitry | | | ✓ *(1)* |
| Open-drain output option | | | ✓ |
| Fast input registers | | ✓ | ✓ |
| Six global output enables | | ✓ | ✓ |
| Two global clocks | | ✓ | ✓ |
| Slew-rate control | | ✓ | ✓ |
| MultiVolt interface *(2)* | ✓ | ✓ | ✓ |
| Programmable register | ✓ | ✓ | ✓ |
| Parallel expanders | ✓ | ✓ | ✓ |
| Shared expanders | ✓ | ✓ | ✓ |
| Power-saving mode | ✓ | ✓ | ✓ |
| Security bit | ✓ | ✓ | ✓ |
| PCI-compliant devices available | ✓ | ✓ | ✓ |

*Notes:*
(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

## Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ($t_{LPA}$) for the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, and $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters.

## Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of `VCC` pins for internal operation and input buffers (`VCCINT`), and another set for I/O output drivers (`VCCIO`).

The `VCCINT` pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The `VCCIO` pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the `VCCIO` pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When $V_{CCIO}$ is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with $V_{CCIO}$ levels lower than 4.75 V incur a nominally greater timing delay of $t_{OD2}$ instead of $t_{OD1}$.

### Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-`OR` plane.

Figure 9 shows the timing requirements for the JTAG signals.

*Figure 9. MAX 7000 JTAG Waveforms*

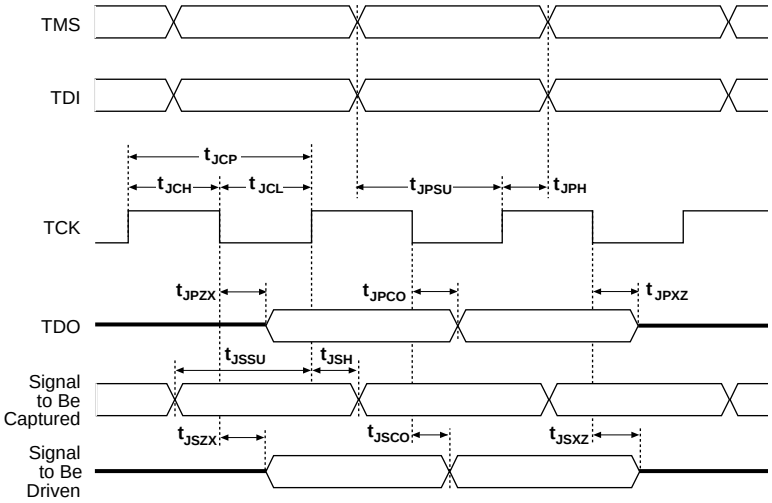



Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

*Table 12. JTAG Timing Parameters & Values for MAX 7000S Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 25 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 25 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 25 | ns |

For more information, see *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*.

*Table 15. MAX 7000 5.0-V Device DC Operating Conditions* *Note (9)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | $V_{CCINT}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 *(8)* | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 4.75 V *(10)* | 2.4 | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.0 V *(10)* | $V_{CCIO}$ – 0.2 | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 4.75 V *(11)* | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.0 V*(11)* | | 0.2 | V |
| $I_I$ | Leakage current of dedicated input pins | $V_I$ = –0.5 to 5.5 V *(11)* | –10 | 10 | µA |
| $I_{OZ}$ | I/O pin tri-state output off-state current | $V_I$ = –0.5 to 5.5 V *(11)*, *(12)* | –40 | 40 | µA |

*Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices* *Note (13)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 12 | pF |

*Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices* *Note (13)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 15 | pF |

*Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices* *Note (13)*

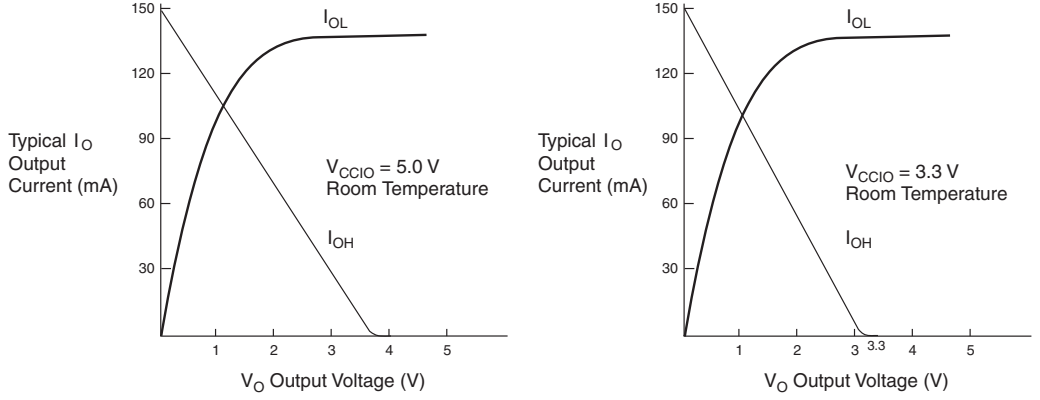
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Dedicated input pin capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{I/O}$ | I/O pin capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

*Notes to tables:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage on I/O pins is –0.5 V and on 4 dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) $V_{CC}$ must rise monotonically.
(5) The POR time for all 7000S devices does not exceed 300 µs. The sufficient $V_{CCINT}$ voltage level for POR is 4.5 V. The device is fully initialized within the POR time after $V_{CCINT}$ reaches the sufficient POR voltage level.
(6) 3.3-V I/O operation is not available for 44-pin packages.
(7) The $V_{CCISP}$ parameter applies only to MAX 7000S devices.
(8) During in-system programming, the minimum DC input voltage is –0.3 V.
(9) These values are specified under the MAX 7000 recommended operating conditions in Table 14 on page 26.
(10) The parameter is measured with 50% of the outputs each sourcing the specified current. The $I_{OH}$ parameter refers to high-level TTL or CMOS output current.
(11) The parameter is measured with 50% of the outputs each sinking the specified current. The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current.
(12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically –60 µA.
(13) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

***Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices***




## Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 12. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

### *Figure 13. Switching Waveforms*

*$t_R$ & $t_F$ < 3 ns.*
*Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.*

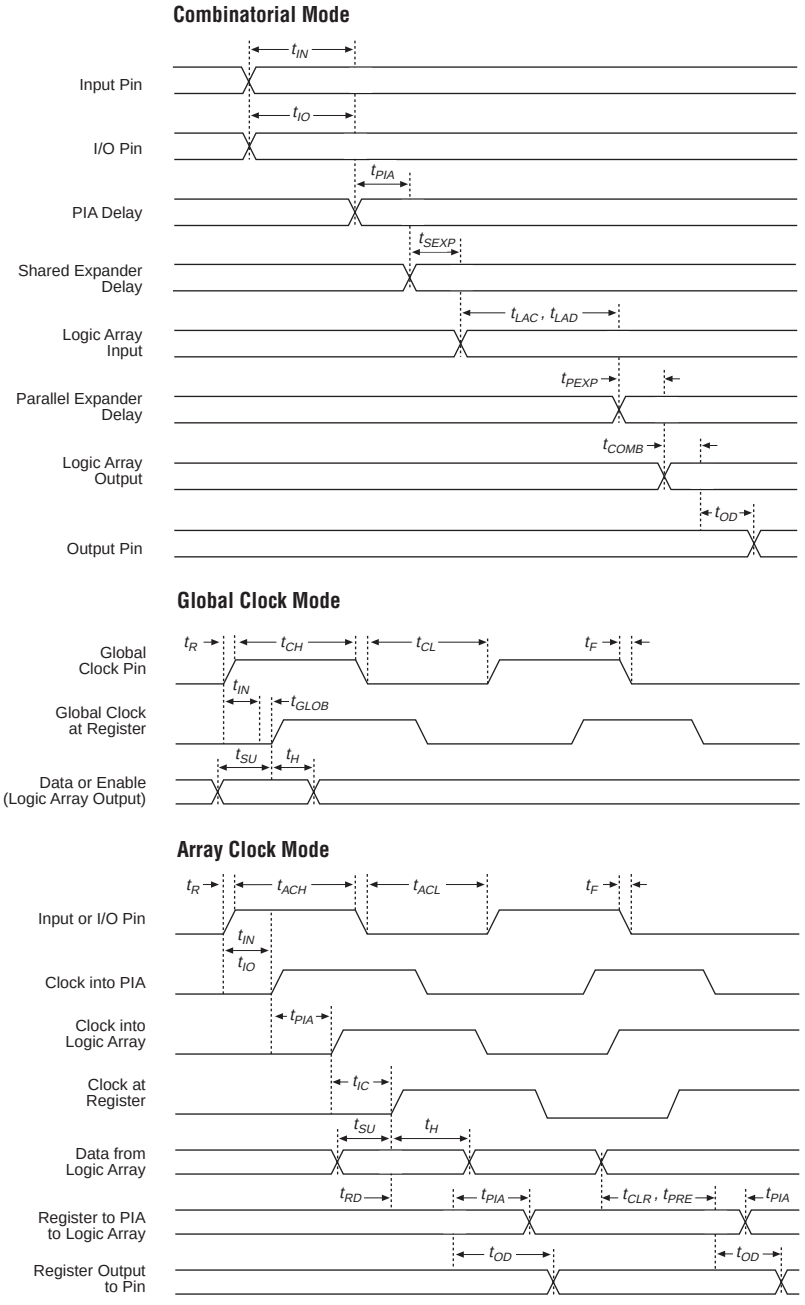


**Table 20. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade -6 | | Speed Grade -7 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.4 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.4 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 0.8 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.5 | | 4.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.0 | | 3.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.0 | | 3.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 2.0 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.5 | | 2.5 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on,<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 7.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 4.0 | | 4.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 4.5 | | 4.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | ns |
| $t_{SU}$ | Register setup time | | 3.0 | | 3.0 | | ns |
| $t_{H}$ | Register hold time | | 1.5 | | 2.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 0.8 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.8 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.5 | | 3.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.0 | | 3.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 0.8 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.0 | ns |
| $t_{PIA}$ | PIA delay | | | 0.8 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 10.0 | | 10.0 | ns |

*Table 21. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 8.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 5.0 | | 5 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.0 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 3.0 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 10.0 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 4.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 4.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 4.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 10.0 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 10.0 | | 10.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 100.0 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

*Table 23. MAX 7000 & MAX 7000E External Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{SU}$ | Global clock setup time | | 7.0 | | 10.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.0 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{CH}$ | Global clock high time | | 4.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 4.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 3.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 4.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| $t_{ACH}$ | Array clock high time | | 5.0 | | 5.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 5.0 | | 5.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 5.0 | | 5.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 11.0 | | 11.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 90.9 | | 90.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 11.0 | | 11.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 90.9 | | 90.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 125.0 | | 125.0 | | MHz |

*Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 1.0 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | *(2)* | | 1.0 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 7.0 | | 7.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.0 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 7.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | *(2)* | | 2.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 1.0 | | 3.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 2.0 | | 4.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 5.0 | | 7.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 5.0 V | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay<br>Slow slew rate = off<br>$V_{CCIO}$ = 3.3 V | C1 = 35 pF *(7)* | | 7.0 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay<br>Slow slew rate = on<br>$V_{CCIO}$ = 5.0 V or 3.3 V | C1 = 35 pF *(2)* | | 10.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 6.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | *(2)* | 4.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | *(2)* | 0.0 | | 2.0 | | ns |
| $t_{RD}$ | Register delay | | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 5.0 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 7.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 0.0 | ns |
| $t_{PRE}$ | Register preset time | | | 4.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 4.0 | | 3.0 | ns |
| $t_{PIA}$ | PIA delay | | | 1.0 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 12.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This parameter applies to MAX 7000E devices only.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(6) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(7) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

***Table 27. EPM7032S External Timing Parameters (Part 1 of 2)*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 2.9 | | 4.0 | | 5.0 | | 7.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | 0.5 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 3.5 | | 4.3 | | 5.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.7 | | 0.9 | | 1.1 | | 2.0 | | ns |
| $\mathbf{t_{AH}}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.7 | | 3.0 | | ns |
| $\mathbf{t_{ACO1}}$ | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.6 | | 8.2 | | 10.0 | ns |
| $\mathbf{t_{ACH}}$ | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ACL}}$ | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CPPW}}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ODH}}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $\mathbf{t_{CNT}}$ | Minimum global clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |
| $\mathbf{f_{CNT}}$ | Maximum internal global clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $\mathbf{t_{ACNT}}$ | Minimum array clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.1 | | 1.1 | | 1.4 | | 1.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 12.0 | | 10.0 | | 10.0 | | 11.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

**Table 29. EPM7064S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 2.9 | | 3.6 | | 6.0 | | 7.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.5 | | 0.5 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 4.0 | | 4.5 | | 5.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 0.7 | | 0.9 | | 3.0 | | 2.0 | | ns |
| $\mathbf{t_{AH}}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.0 | | 3.0 | | ns |

*Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.6 | | 2.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

*Table 35. EPM7192S External Timing Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 4.1 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 1.0 | | 2.0 | | 4.0 | | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$ in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The $P_{IO}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The $I_{CCINT}$ value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

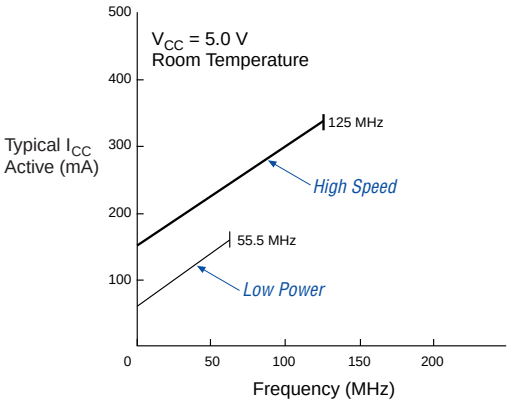
$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}}$$

The parameters in this equation are shown below:

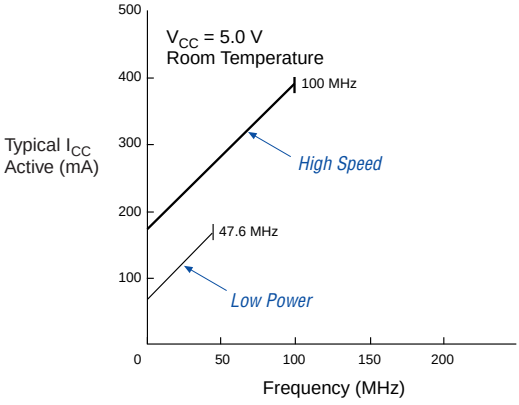
| | | |
|---|---|---|
| $MC_{TON}$ | = | Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $MC_{DEV}$ | = | Number of macrocells in the device |
| $MC_{USED}$ | = | Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (**.rpt**) |
| $\mathbf{f_{MAX}}$ | = | Highest clock frequency to the device |
| $\mathbf{tog_{LC}}$ | = | Average ratio of logic cells toggling at each clock (typically 0.125) |
| A, B, C | = | Constants, shown in Table 39 |

*Figure 14. $I_{CC}$ vs. Frequency for MAX 7000 Devices (Part 2 of 2)*

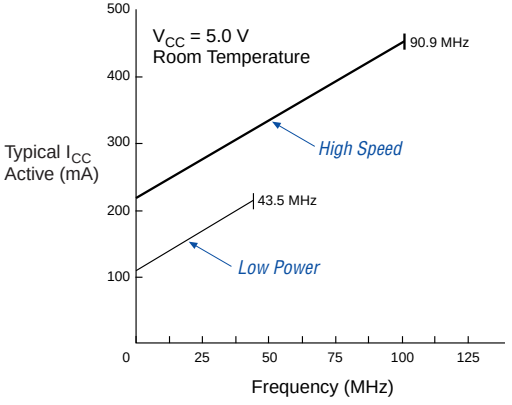
**EPM7128E**




**EPM7160E**




**EPM7192E**




**EPM7256E**

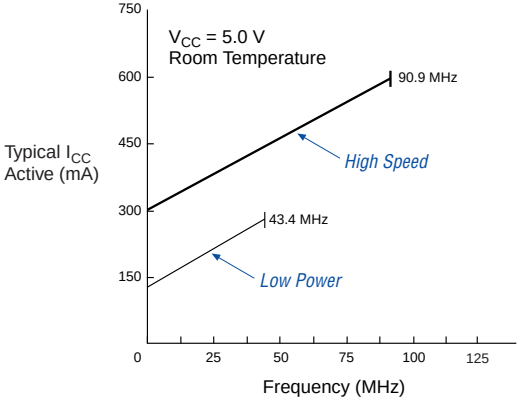
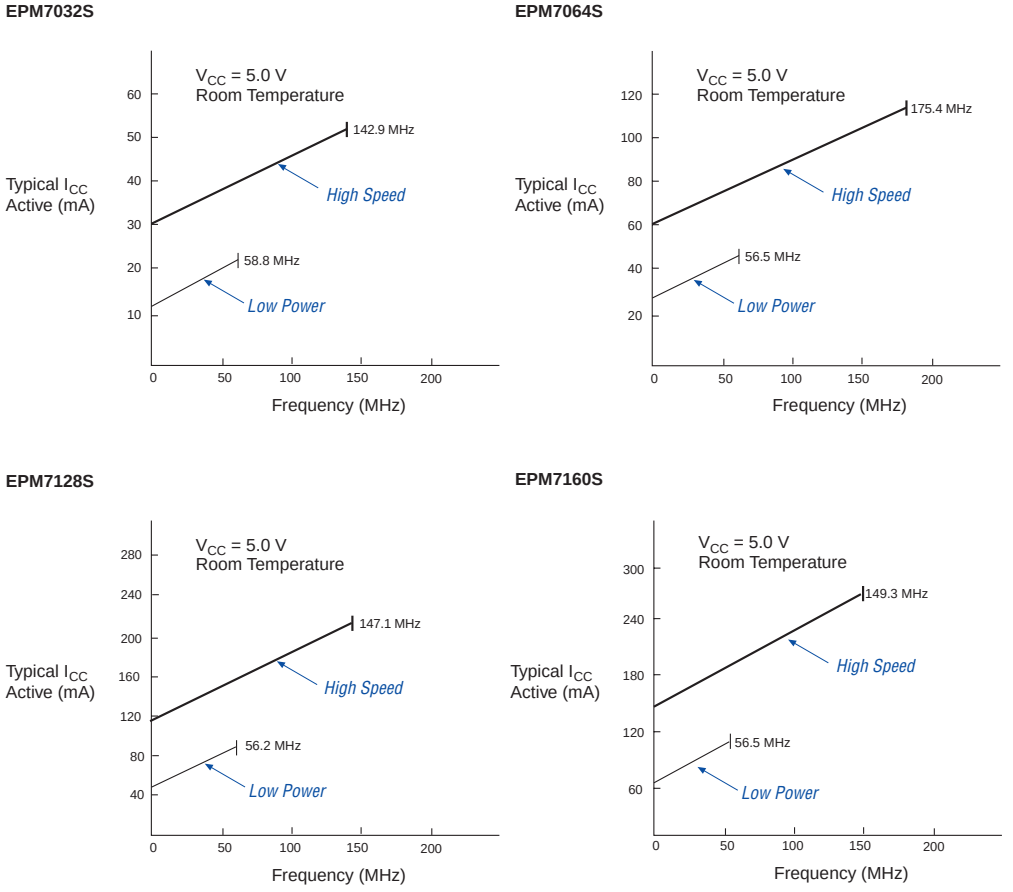


Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

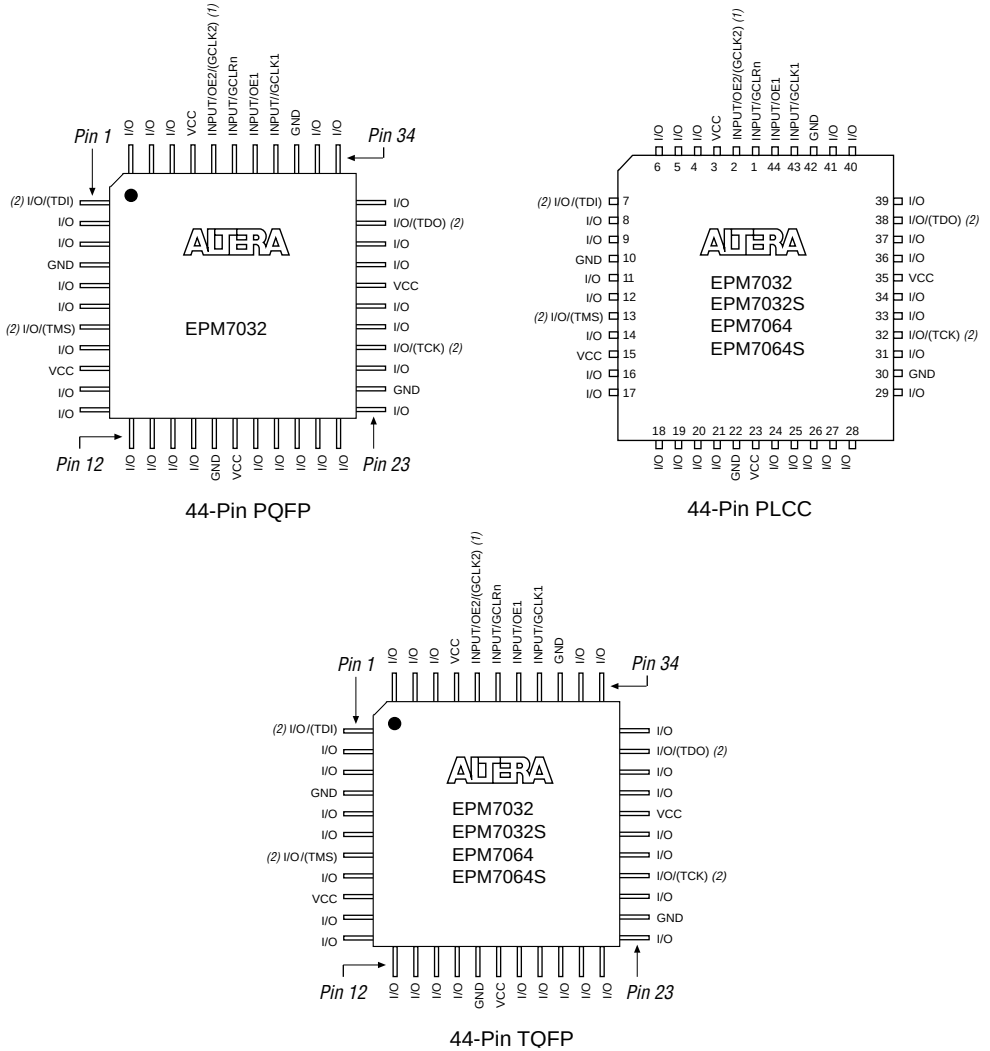
*Figure 15. $I_{CC}$ vs. Frequency for MAX 7000S Devices (Part 1 of 2)*



Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

### *Figure 16. 44-Pin Package Pin-Out Diagram*

*Package outlines not drawn to scale.*




44-Pin PQFP

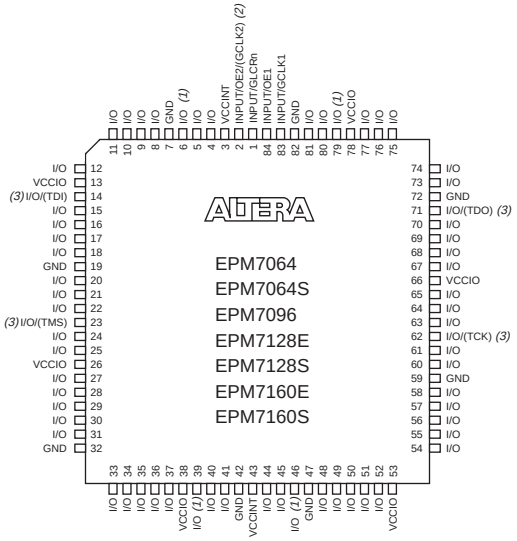
44-Pin PLCC

44-Pin TQFP

*Notes:*
(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(2) JTAG ports are available in MAX 7000S devices only.

### *Figure 18. 84-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*




84-Pin PLCC

*Notes:*
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
(2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(3) JTAG ports are available in MAX 7000S devices only.

*Notes:*