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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7064slc84-7n">https://www.e-xfl.com/product-detail/intel/epm7064slc84-7n</a>

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

**Table 3. MAX 7000 Speed Grades**

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

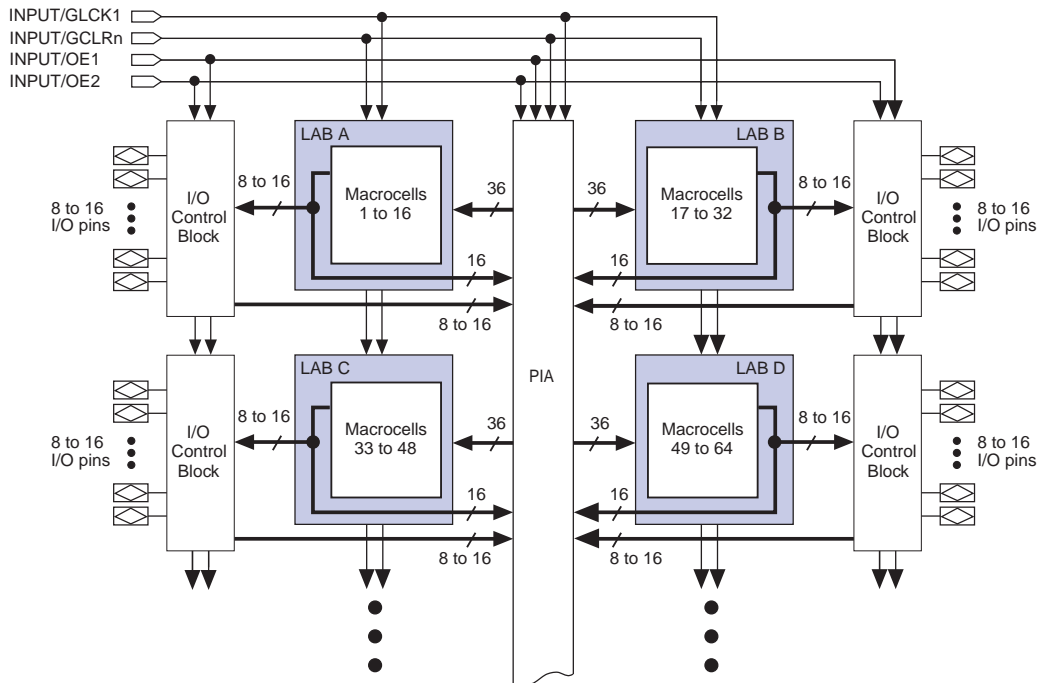
## Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

**Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram**



Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

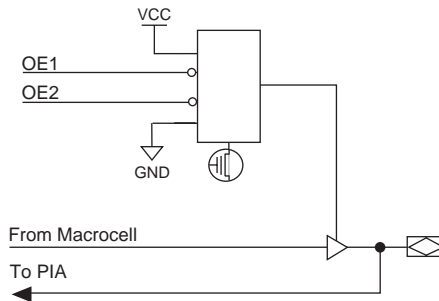
All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

## Expander Product Terms

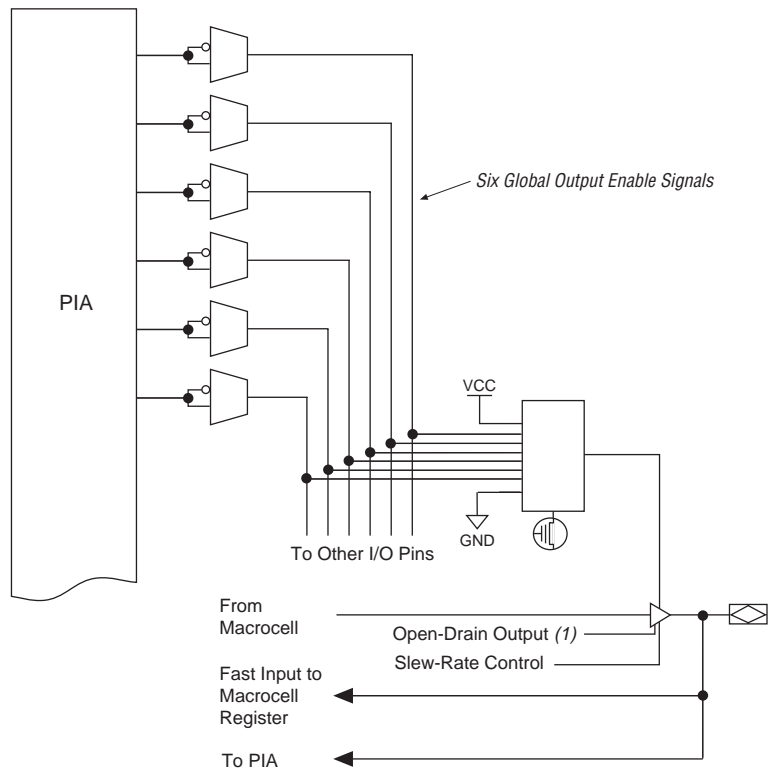
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

**Figure 8. I/O Control Block of MAX 7000 Devices**

**EPM7032, EPM7064 & EPM7096 Devices**



**MAX 7000E & MAX 7000S Devices**



**Note:**

- (1) The open-drain output option is available only in MAX 7000S devices.

The programming times described in Tables 6 through 8 are associated with the worst-case method using the enhanced ISP algorithm.

**Table 6. MAX 7000S  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PPULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

Tables 7 and 8 show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

**Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

## Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ , and  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters.

## Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

### Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

**Table 20. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade -6		Speed Grade -7		Unit
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.4		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.4		0.5	ns
$t_{FIN}$	Fast input delay	(2)		0.8		1.0	ns
$t_{SEXP}$	Shared expander delay			3.5		4.0	ns
$t_{PEXP}$	Parallel expander delay			0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.0		3.0	ns
$t_{LAC}$	Logic control array delay			2.0		3.0	ns
$t_{OE}$	Internal output enable delay	(2)				2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		2.0		2.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.5		2.5	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		7.0		7.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		4.0		4.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		4.5		4.5	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		4.0		4.0	ns
$t_{SU}$	Register setup time		3.0		3.0		ns
$t_H$	Register hold time		1.5		2.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	2.5		3.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.5		0.5		ns
$t_{RD}$	Register delay			0.8		1.0	ns
$t_{COMB}$	Combinatorial delay			0.8		1.0	ns
$t_{JC}$	Array clock delay			2.5		3.0	ns
$t_{EN}$	Register enable time			2.0		3.0	ns
$t_{GLOB}$	Global control delay			0.8		1.0	ns
$t_{PRE}$	Register preset time			2.0		2.0	ns
$t_{CLR}$	Register clear time			2.0		2.0	ns
$t_{PIA}$	PIA delay			0.8		1.0	ns
$t_{LPA}$	Low-power adder	(8)		10.0		10.0	ns

**Table 23. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		10.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		3.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t <sub>ACH</sub>	Array clock high time		5.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		5.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			11.0		11.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			11.0		11.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

**Table 25. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>SU</sub>	Global clock setup time		11.0		11.0		12.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		—		5.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		—		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t <sub>CH</sub>	Global clock high time		5.0		6.0		6.0		ns
t <sub>CL</sub>	Global clock low time		5.0		6.0		6.0		ns
t <sub>ASU</sub>	Array clock setup time		4.0		4.0		5.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		5.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>ACH</sub>	Array clock high time		6.0		6.5		8.0		ns
t <sub>ACL</sub>	Array clock low time		6.0		6.5		8.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	6.0		6.5		8.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			13.0		13.0		16.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	76.9		76.9		62.5		MHz
t <sub>ACNT</sub>	Minimum array clock period			13.0		13.0		16.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	76.9		76.9		62.5		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	100		83.3		83.3		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FSU}$	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
$t_{RD}$	Register delay			1.2		1.6		1.0		2.0	ns
$t_{COMB}$	Combinatorial delay			0.9		1.0		1.0		2.0	ns
$t_{IC}$	Array clock delay			2.7		3.3		3.0		5.0	ns
$t_{EN}$	Register enable time			2.6		3.2		3.0		5.0	ns
$t_{GLOB}$	Global control delay			1.6		1.9		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.0		2.4		2.0		3.0	ns
$t_{CLR}$	Register clear time			2.0		2.4		2.0		3.0	ns
$t_{PIA}$	PIA delay	(7)		1.1		1.3		1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		11.0		10.0		11.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$  and  $t_{CPW}$  parameters for macrocells running in the low-power mode.

**Table 33. EPM7160S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACNT</sub>	Minimum array clock period			6.7		8.2		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	149.3		122.0		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

**Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			2.6		3.2		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.6		4.3		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.3		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.8		3.4		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.8		3.4		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.9		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.9		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.0		1.2		2.0		4.0		ns
$t_H$	Register hold time		1.6		2.0		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
$t_{RD}$	Register delay			1.3		1.6		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.3		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		3.5		5.0		6.0	ns
$t_{EN}$	Register enable time			2.8		3.4		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.0		2.4		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.4		3.0		3.0		4.0	ns

**Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLR}$	Register clear time			2.4		3.0		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		1.6		2.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

**Table 35. EPM7192S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		4.1		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		1.0		2.0		4.0		ns

Tables 37 and 38 show the EPM7256S AC operating conditions.

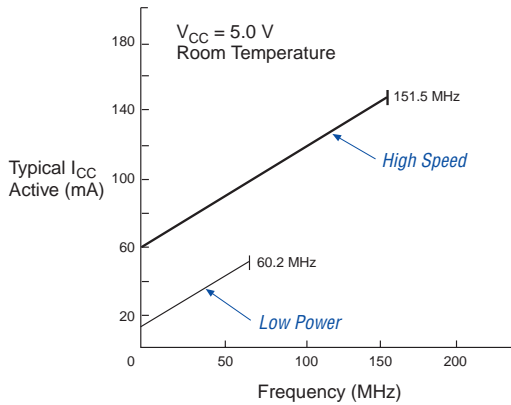
**Table 37. EPM7256S External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.9		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.8		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.9		3.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			7.8		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			7.8		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

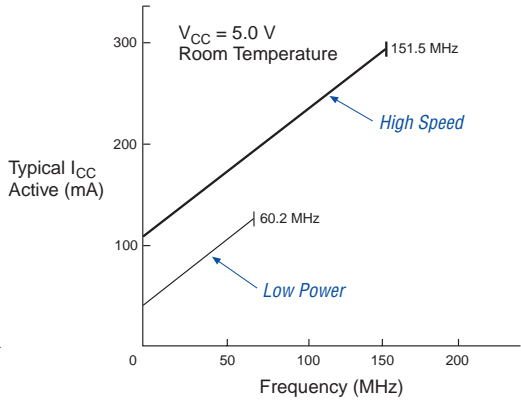
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 1 of 2)

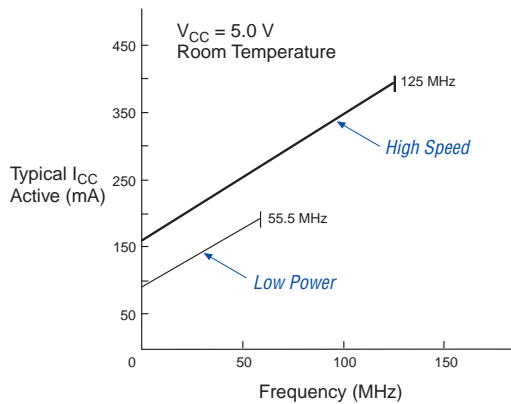
EPM7032



EPM7064

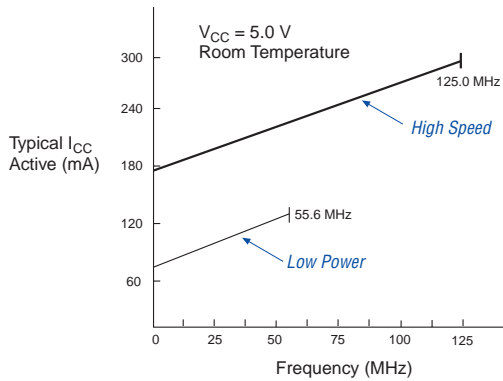


EPM7096

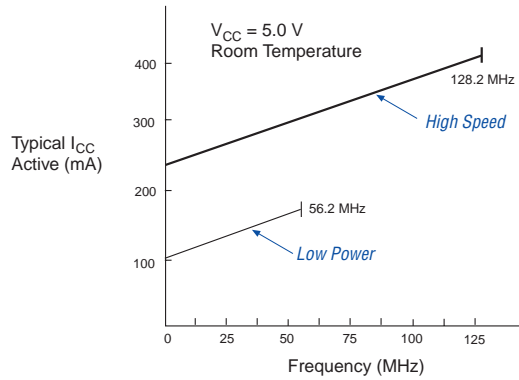


**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 2 of 2)**

EPM7192S



EPM7256S



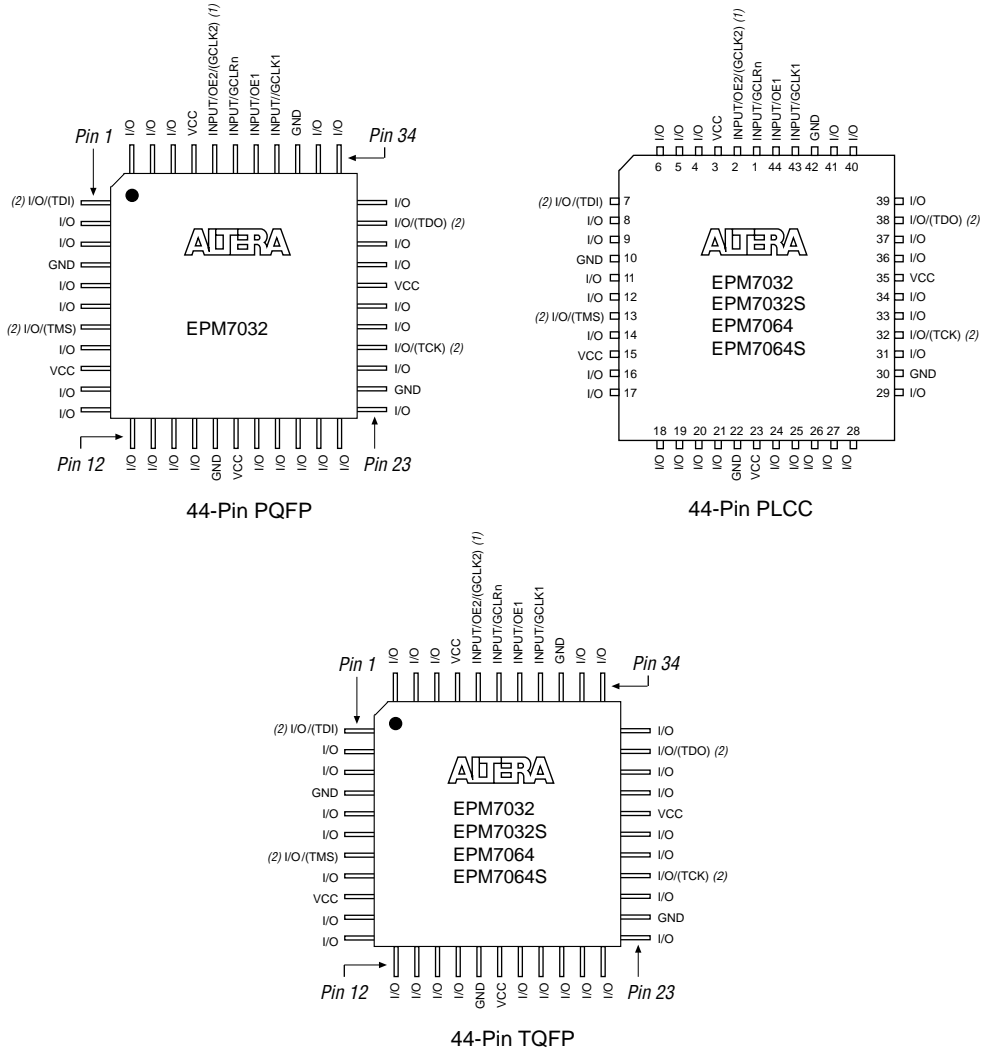
## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

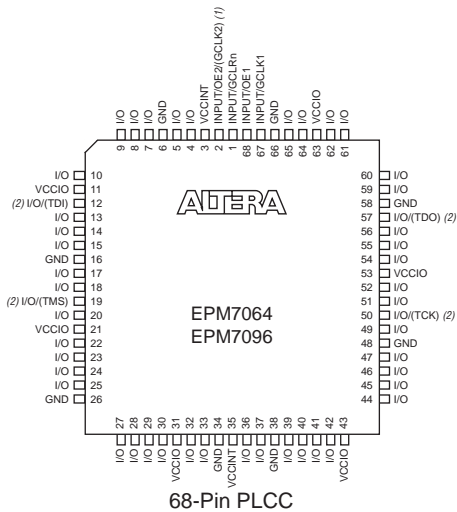
**Figure 16. 44-Pin Package Pin-Out Diagram**

Package outlines not drawn to scale.



**Notes:**

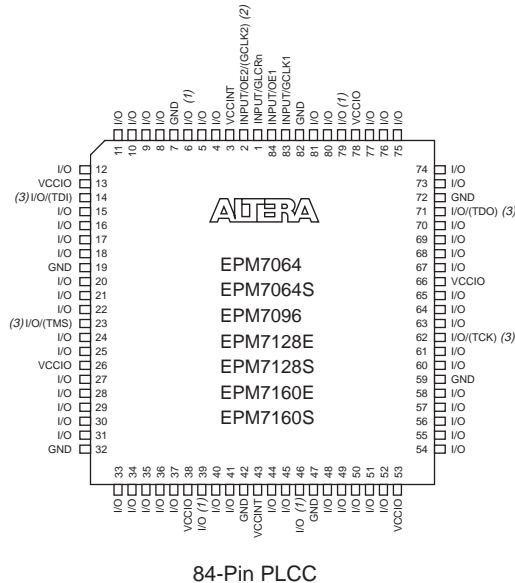
- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

**Figure 17. 68-Pin Package Pin-Out Diagram***Package outlines not drawn to scale.***Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

**Figure 18. 84-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.



**Notes:**

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

## Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

### Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

### Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

### Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

### Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

### Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).