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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

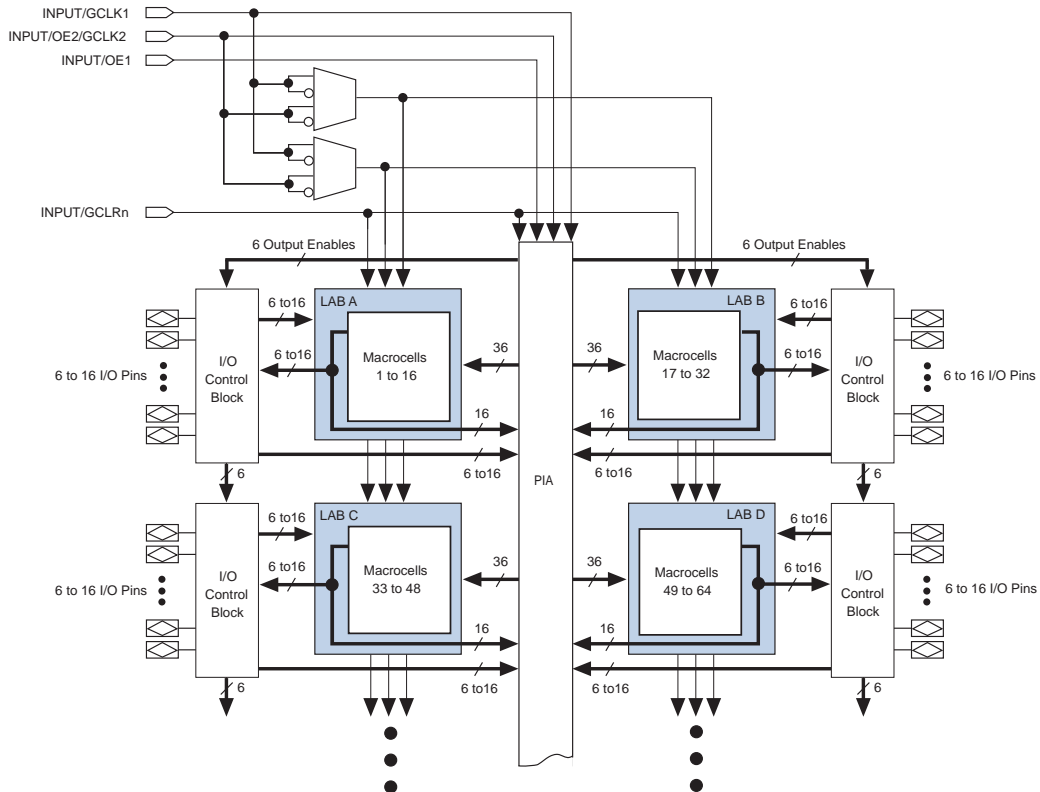
### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	6 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7064stc100-6f">https://www.e-xfl.com/product-detail/intel/epm7064stc100-6f</a>

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**



## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

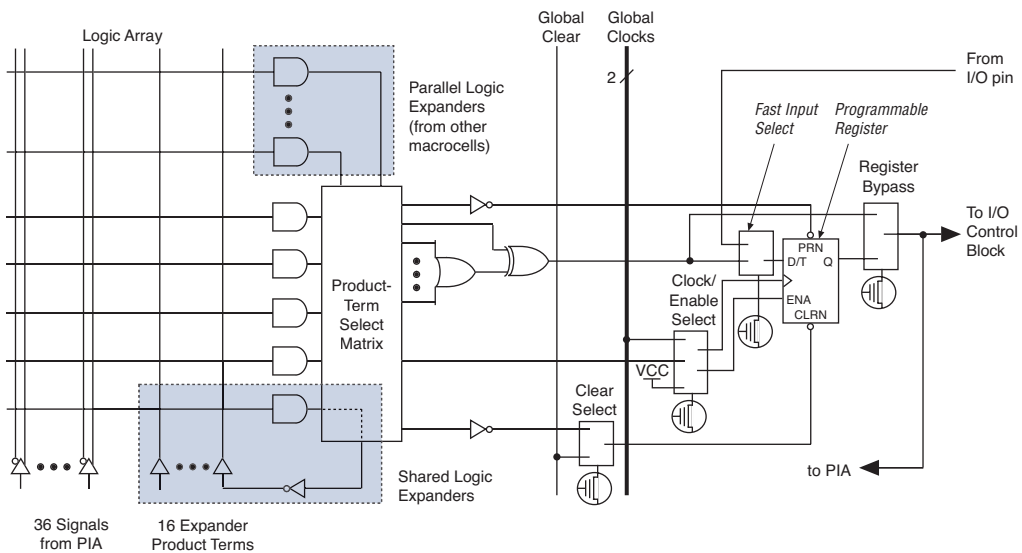
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

## Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

**Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell**



## Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ , and  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters.

## Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

### Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

### Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

## Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [\*Altera Programming Hardware Data Sheet\*](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [\*Programming Hardware Manufacturers\*](#).

## Design Security

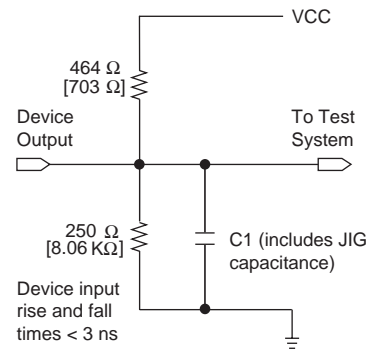
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 10](#). Test patterns can be used and then erased during early stages of the production flow.

**Figure 10. MAX 7000 AC Test Conditions**

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.*



## QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.



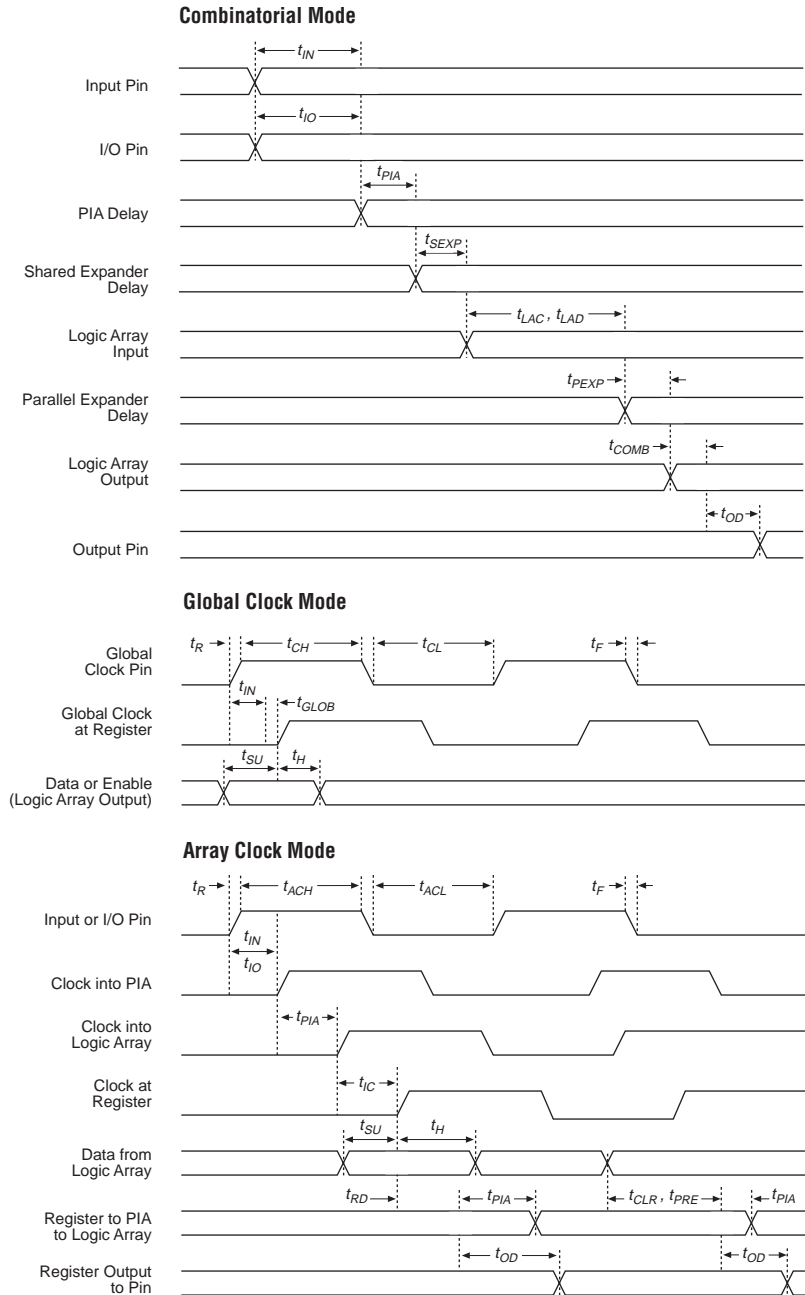
For detailed information and carrier dimensions, refer to the [QFP Carrier & Development Socket Data Sheet](#).



MAX 7000S devices are not shipped in carriers.

**Figure 13. Switching Waveforms**

$t_R$  &  $t_F < 3$  ns.  
Inputs are driven at 3 V  
for a logic high and 0 V  
for a logic low. All timing  
characteristics are  
measured at 1.5 V.



Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 19. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
$t_{SU}$	Global clock setup time		5.0		6.0		ns
$t_H$	Global clock hold time		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input	(2)	2.5		3.0		ns
$t_{FH}$	Global clock hold time of fast input	(2)	0.5		0.5		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
$t_{CH}$	Global clock high time		2.5		3.0		ns
$t_{CL}$	Global clock low time		2.5		3.0		ns
$t_{ASU}$	Array clock setup time		2.5		3.0		ns
$t_{AH}$	Array clock hold time		2.0		2.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
$t_{ACH}$	Array clock high time		3.0		3.0		ns
$t_{ACL}$	Array clock low time		3.0		3.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			6.6		8.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
$t_{ACNT}$	Minimum array clock period			6.6		8.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
$f_{MAX}$	Maximum clock frequency	(6)	200		166.7		MHz



**Table 21. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		8.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.5		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		2.0		3.0		ns
t <sub>AH</sub>	Array clock hold time		3.0		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t <sub>ACH</sub>	Array clock high time		4.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		4.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			10.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			10.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.5		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.5		1.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			5.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.8		0.8	ns
$t_{LAD}$	Logic array delay			5.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.5		2.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		2.5	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.5		6.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		5.0		5.0	ns
$t_{SU}$	Register setup time		2.0		3.0		ns
$t_H$	Register hold time		3.0		3.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.5		0.5		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			5.0		5.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0	ns
$t_{PRE}$	Register preset time			3.0		3.0	ns
$t_{CLR}$	Register clear time			3.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		11.0	ns

**Table 23. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		10.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		3.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t <sub>ACH</sub>	Array clock high time		5.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		5.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			11.0		11.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			11.0		11.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

### Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		4.0		5.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		1.1		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.7		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.0		8.6		10.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 33 and 34 show the EPM7160S AC operating conditions.

**Table 33. EPM7160S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.4		4.2		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.9		4.8		5		8	ns
t <sub>CH</sub>	Global clock high time		3.0		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.9		1.1		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.7		2.1		3.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		6.4		7.9		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			6.7		8.2		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	149.3		122.0		100.0		76.9		MHz

**Table 33. EPM7160S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACNT</sub>	Minimum array clock period			6.7		8.2		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	149.3		122.0		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

**Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			2.6		3.2		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.6		4.3		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.3		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.8		3.4		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.8		3.4		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.9		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.9		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.0		1.2		2.0		4.0		ns
$t_H$	Register hold time		1.6		2.0		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
$t_{RD}$	Register delay			1.3		1.6		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.3		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		3.5		5.0		6.0	ns
$t_{EN}$	Register enable time			2.8		3.4		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.0		2.4		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.4		3.0		3.0		4.0	ns

**Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_H$	Register hold time		1.7		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		2.3		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.7		0.5		1.0		ns
$t_{RD}$	Register delay			1.4		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.2		2.0		1.0	ns
$t_{IC}$	Array clock delay			3.2		5.0		6.0	ns
$t_{EN}$	Register enable time			3.1		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.5		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.7		3.0		4.0	ns
$t_{CLR}$	Register clear time			2.7		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		2.4		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$  and  $t_{CPW}$  parameters for macrocells running in the low-power mode.

**Table 38. EPM7256S Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			3.4		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.9		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.1		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.6		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.6		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.8		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.1		2.0		4.0		ns
$t_H$	Register hold time		1.6		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		2.4		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.5		1.0		ns
$t_{RD}$	Register delay			1.1		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.1		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		5.0		6.0	ns
$t_{EN}$	Register enable time			2.6		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.8		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.7		3.0		4.0	ns
$t_{CLR}$	Register clear time			2.7		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		3.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		10.0		11.0		13.0	ns



**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in [Table 14](#). See [Figure 13](#) for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPTW}$  parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$  in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{CCINT}$  value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC}$$

The parameters in this equation are shown below:

$MC_{TON}$	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
$MC_{DEV}$	=	Number of macrocells in the device
$MC_{USED}$	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
$f_{MAX}$	=	Highest clock frequency to the device
$\text{tog}_{LC}$	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in <a href="#">Table 39</a>

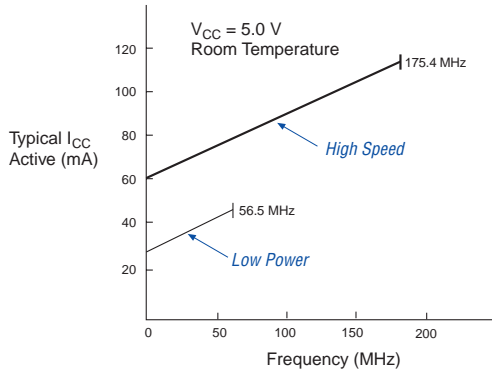
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 1 of 2)**

**EPM7032S**



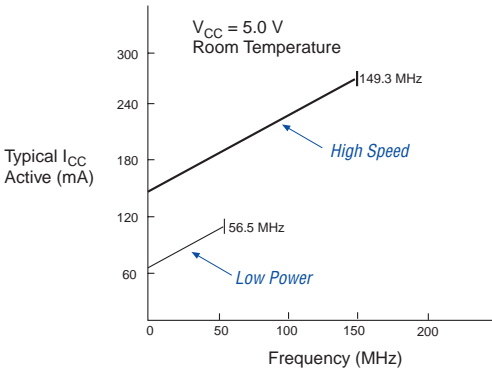
**EPM7064S**



**EPM7128S**



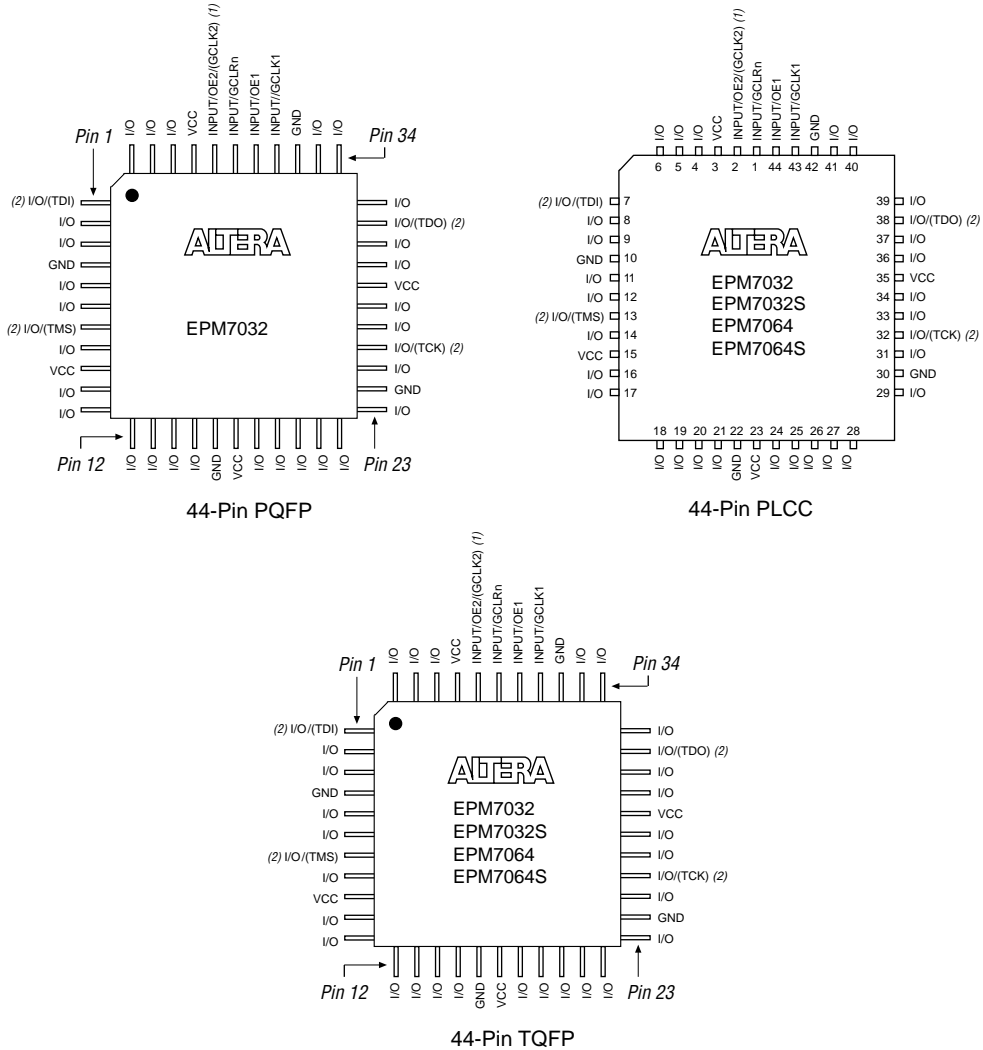
**EPM7160S**



Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

**Figure 16. 44-Pin Package Pin-Out Diagram**

Package outlines not drawn to scale.

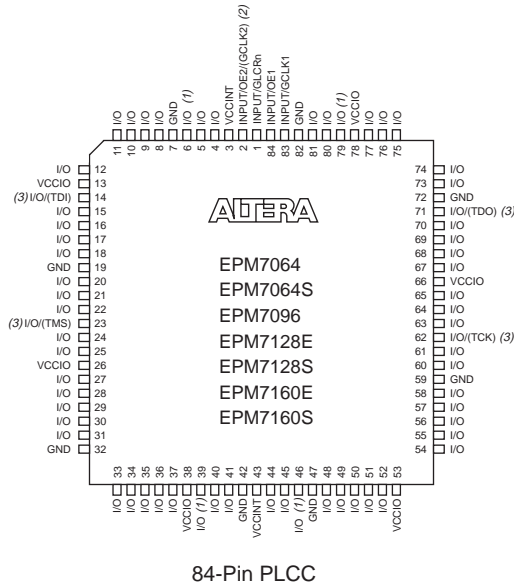


**Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

**Figure 18. 84-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.



**Notes:**

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

## Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

### Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

### Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

### Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

### Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

### Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).