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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	4
Number of Macrocells	64
Number of Gates	1250
Number of I/O	68
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7064sti100-7">https://www.e-xfl.com/product-detail/intel/epm7064sti100-7</a>

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

**Table 5. MAX 7000 Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

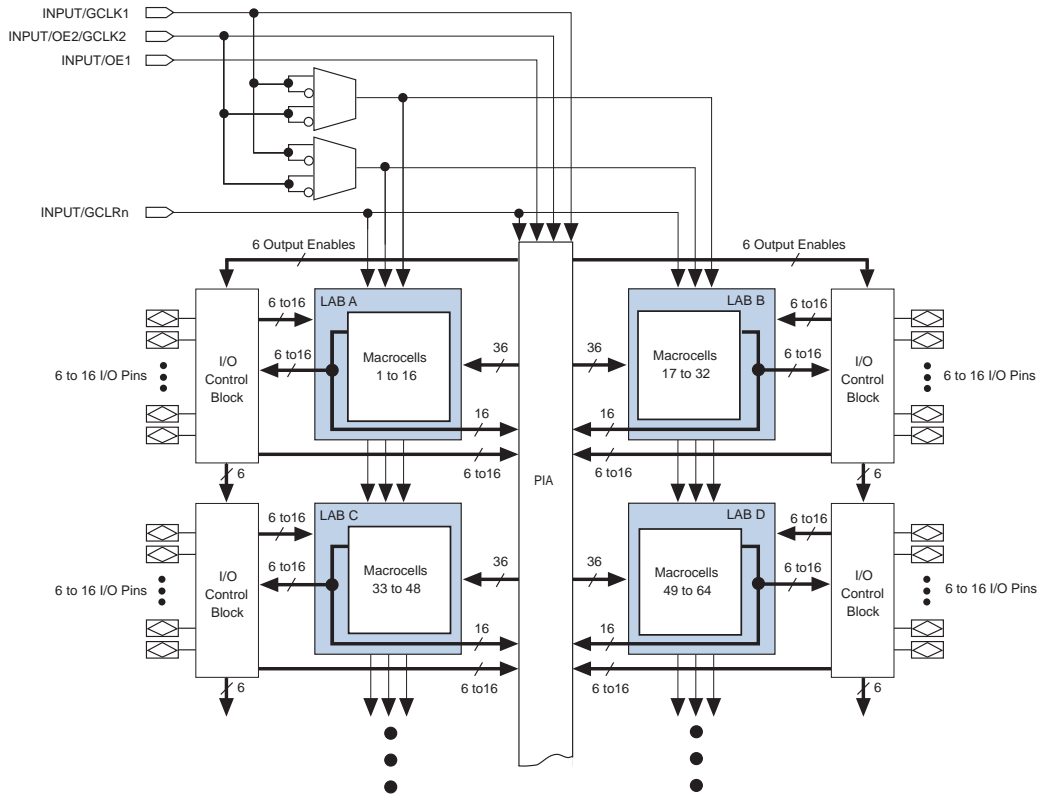
**Notes:**

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**



## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

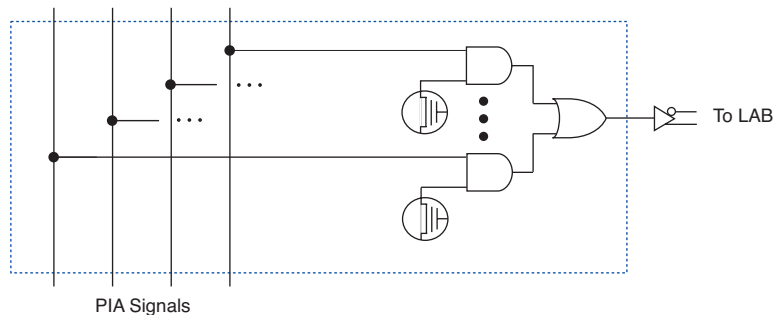
## Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

**Figure 7. PIA Routing**



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000S Device*

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

### Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

## Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the *Programming Hardware Manufacturers*.

## Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

**Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	Supply voltage	With respect to ground (2)	–2.0	7.0	V
V <sub>I</sub>	DC input voltage		–2.0	7.0	V
I <sub>OUT</sub>	DC output current, per pin		–25	25	mA
T <sub>STG</sub>	Storage temperature	No bias	–65	150	°C
T <sub>AMB</sub>	Ambient temperature	Under bias	–65	135	°C
T <sub>J</sub>	Junction temperature	Ceramic packages, under bias		150	°C
		PQFP and RQFP packages, under bias		135	°C

**Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions**

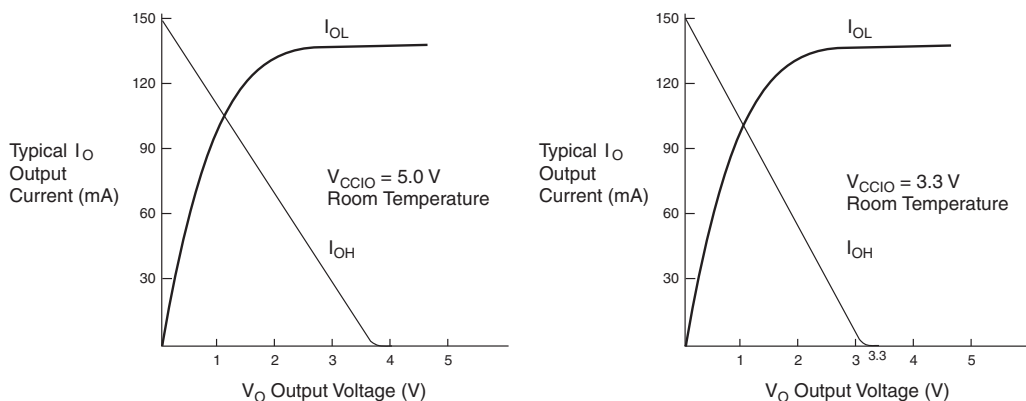
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CCINT</sub>	Supply voltage for internal logic and input buffers	(3), (4), (5)	4.75 (4.50)	5.25 (5.50)	V
V <sub>CCIO</sub>	Supply voltage for output drivers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	(3), (4), (6)	3.00 (3.00)	3.60 (3.60)	V
V <sub>CCISP</sub>	Supply voltage during ISP	(7)	4.75	5.25	V
V <sub>I</sub>	Input voltage		–0.5 (8)	V <sub>CCINT</sub> + 0.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CCIO</sub>	V
T <sub>A</sub>	Ambient temperature	For commercial use	0	70	°C
		For industrial use	–40	85	°C
T <sub>J</sub>	Junction temperature	For commercial use	0	90	°C
		For industrial use	–40	105	°C
t <sub>R</sub>	Input rise time			40	ns
t <sub>F</sub>	Input fall time			40	ns

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage on I/O pins is  $-0.5$  V and on 4 dedicated input pins is  $-0.3$  V. During transitions, the inputs may undershoot to  $-2.0$  V or overshoot to  $7.0$  V for input currents less than  $100$  mA and periods shorter than  $20$  ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4)  $V_{CC}$  must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed  $300$   $\mu$ s. The sufficient  $V_{CCINT}$  voltage level for POR is  $4.5$  V. The device is fully initialized within the POR time after  $V_{CCINT}$  reaches the sufficient POR voltage level.
- (6)  $3.3$ -V I/O operation is not available for 44-pin packages.
- (7) The  $V_{CCISP}$  parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is  $-0.3$  V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically  $-60$   $\mu$ A.
- (13) Capacitance is measured at  $25^\circ$  C and is sample-tested only. The  $\text{OE}1$  pin has a maximum capacitance of  $20$  pF.

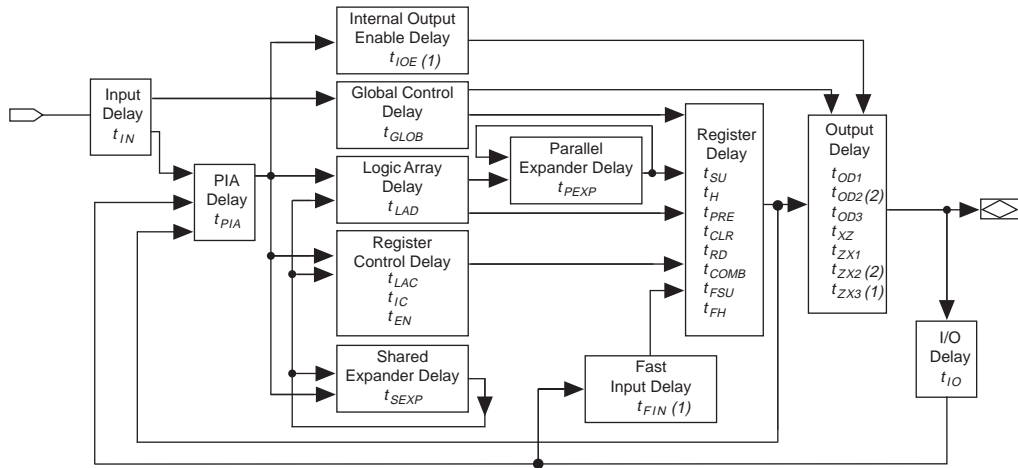
Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

**Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices**



## Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

**Figure 12. MAX 7000 Timing Model****Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).

**Table 21. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		8.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.5		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		2.0		3.0		ns
t <sub>AH</sub>	Array clock hold time		3.0		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t <sub>ACH</sub>	Array clock high time		4.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		4.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			10.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			10.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

**Table 23. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		10.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		3.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t <sub>ACH</sub>	Array clock high time		5.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		5.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			11.0		11.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			11.0		11.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

**Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			1.0		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			1.0		2.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			7.0		7.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0	ns
$t_{LAD}$	Logic array delay			7.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
$t_{SU}$	Register setup time		1.0		4.0		ns
$t_H$	Register hold time		6.0		4.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	4.0		2.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.0		2.0		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			7.0		5.0	ns
$t_{GLOB}$	Global control delay			2.0		0.0	ns
$t_{PRE}$	Register preset time			4.0		3.0	ns
$t_{CLR}$	Register clear time			4.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		12.0	ns

**Table 29. EPM7064S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.6		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.2		3.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.2		3.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		3.0		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.0		3.0		ns

Table 32. EPM7128S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.5		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.5		0.5		2.0	ns
$t_{FIN}$	Fast input delay			2.6		1.0		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.7		4.0		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.1		0.8		0.8		1.0	ns
$t_{LAD}$	Logic array delay			3.0		3.0		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			3.0		3.0		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.7		2.0		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.4		2.0		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.9		2.5		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.4		7.0		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.0		3.0		2.0		4.0		ns
$t_H$	Register hold time		1.7		2.0		5.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		3.0		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.5		0.5		1.0		ns
$t_{RD}$	Register delay			1.4		1.0		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.0		2.0		1.0	ns
$t_{IC}$	Array clock delay			3.1		3.0		5.0		6.0	ns
$t_{EN}$	Register enable time			3.0		3.0		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.0		1.0		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.4		2.0		3.0		4.0	ns
$t_{CLR}$	Register clear time			2.4		2.0		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		1.4		1.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

Tables 37 and 38 show the EPM7256S AC operating conditions.

**Table 37. EPM7256S External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.9		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.8		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.9		3.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			7.8		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			7.8		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in [Table 14](#). See [Figure 13](#) for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$  in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{CCINT}$  value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times tog_{LC}$$

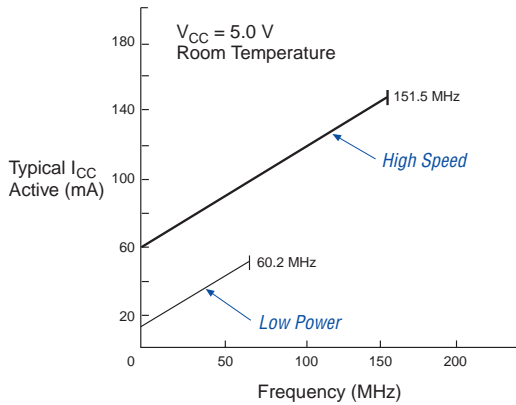
The parameters in this equation are shown below:

$MC_{TON}$	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
$MC_{DEV}$	=	Number of macrocells in the device
$MC_{USED}$	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
$f_{MAX}$	=	Highest clock frequency to the device
$tog_{LC}$	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in <a href="#">Table 39</a>

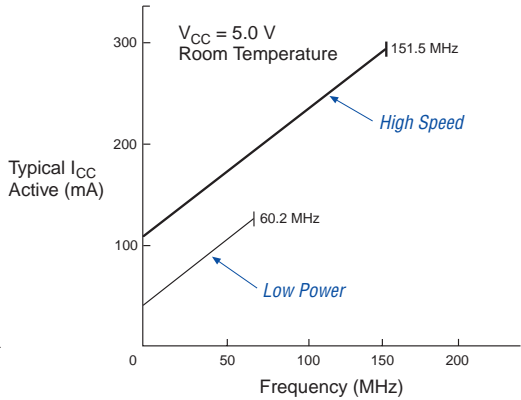
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 1 of 2)

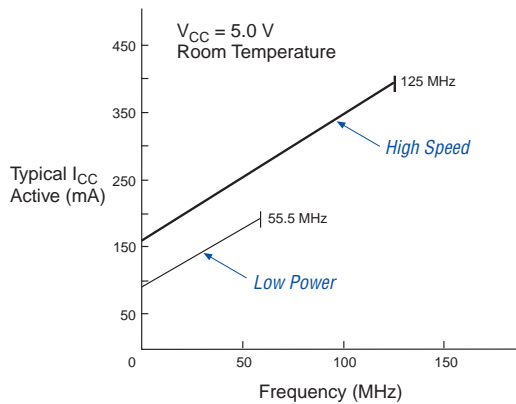
EPM7032



EPM7064

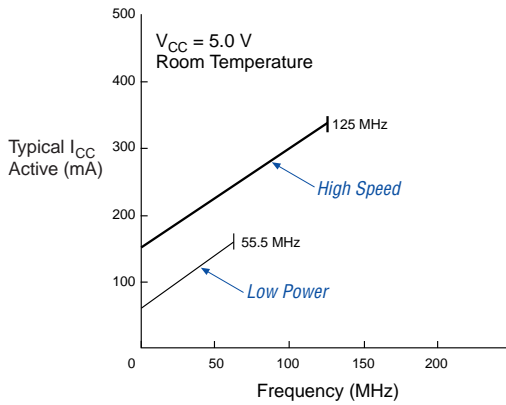


EPM7096

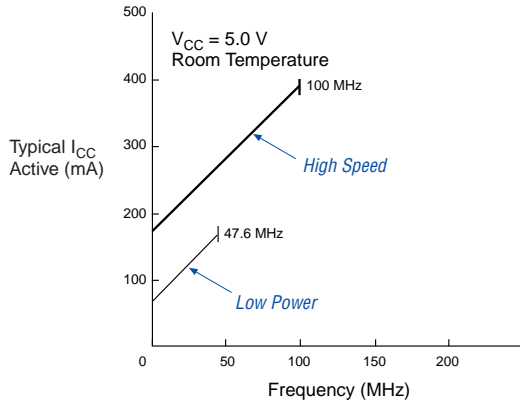


**Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 2 of 2)**

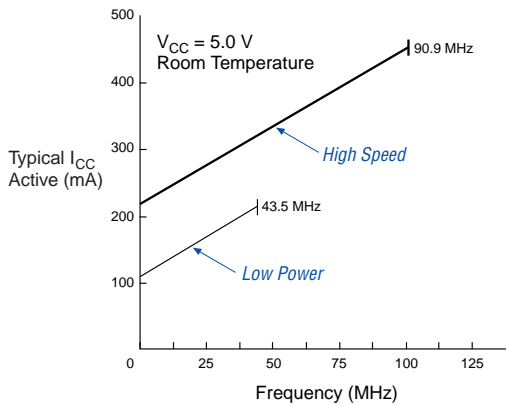
**EPM7128E**



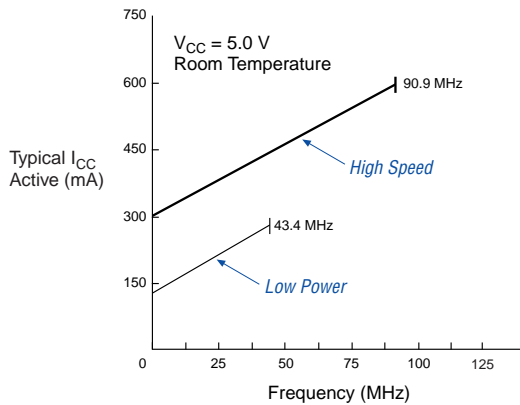
**EPM7160E**



**EPM7192E**



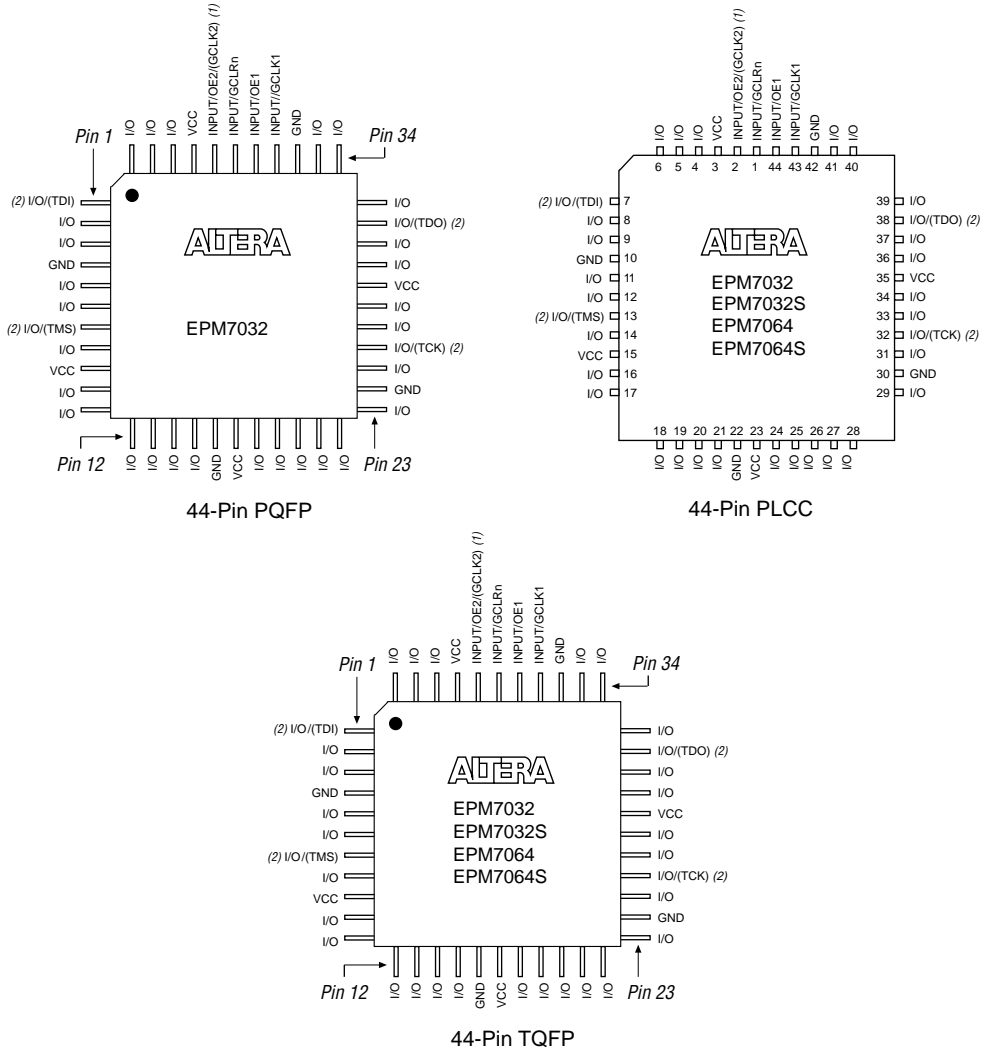
**EPM7256E**



Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

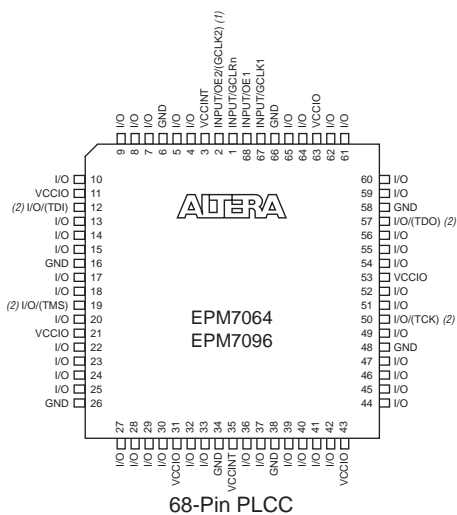
**Figure 16. 44-Pin Package Pin-Out Diagram**

Package outlines not drawn to scale.



**Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

**Figure 17. 68-Pin Package Pin-Out Diagram***Package outlines not drawn to scale.***Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.