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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Programmable Type | EE PLD |
| Delay Time tpd(1) Max | 12 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 6 |
| Number of Macrocells | 96 |
| Number of Gates | 1800 |
| Number of I/O | 68 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7096lc84-12 |

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 3 for available speed grades.

***Table 3. MAX 7000 Speed Grades***

| Device | Speed Grade | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **-5** | **-6** | **-7** | **-10P** | **-10** | **-12P** | **-12** | **-15** | **-15T** | **-20** |
| EPM7032 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | |
| EPM7032S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7064 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7064S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7096 | | | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7128E | | | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7128S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7160E | | | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7160S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7192E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7192S | | | ✓ | | ✓ | | | ✓ | | |
| EPM7256E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7256S | | | ✓ | | ✓ | | | ✓ | | |

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

***Table 4. MAX 7000 Device Features***

| Feature | EPM7032<br>EPM7064<br>EPM7096 | All MAX 7000E Devices | All MAX 7000S Devices |
|---|---|---|---|
| ISP via JTAG interface | | | ✓ |
| JTAG BST circuitry | | | ✓ *(1)* |
| Open-drain output option | | | ✓ |
| Fast input registers | | ✓ | ✓ |
| Six global output enables | | ✓ | ✓ |
| Two global clocks | | ✓ | ✓ |
| Slew-rate control | | ✓ | ✓ |
| MultiVolt interface *(2)* | ✓ | ✓ | ✓ |
| Programmable register | ✓ | ✓ | ✓ |
| Parallel expanders | ✓ | ✓ | ✓ |
| Shared expanders | ✓ | ✓ | ✓ |
| Power-saving mode | ✓ | ✓ | ✓ |
| Security bit | ✓ | ✓ | ✓ |
| PCI-compliant devices available | ✓ | ✓ | ✓ |

*Notes:*

(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.

(2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

***Table 5. MAX 7000 Maximum User I/O Pins*** *Note (1)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84 *(2)* | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84 *(2)* | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132 *(2)* | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164 *(2)* | 164 |

*Notes:*

(1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-`AND`/fixed-`OR` array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported byAltera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

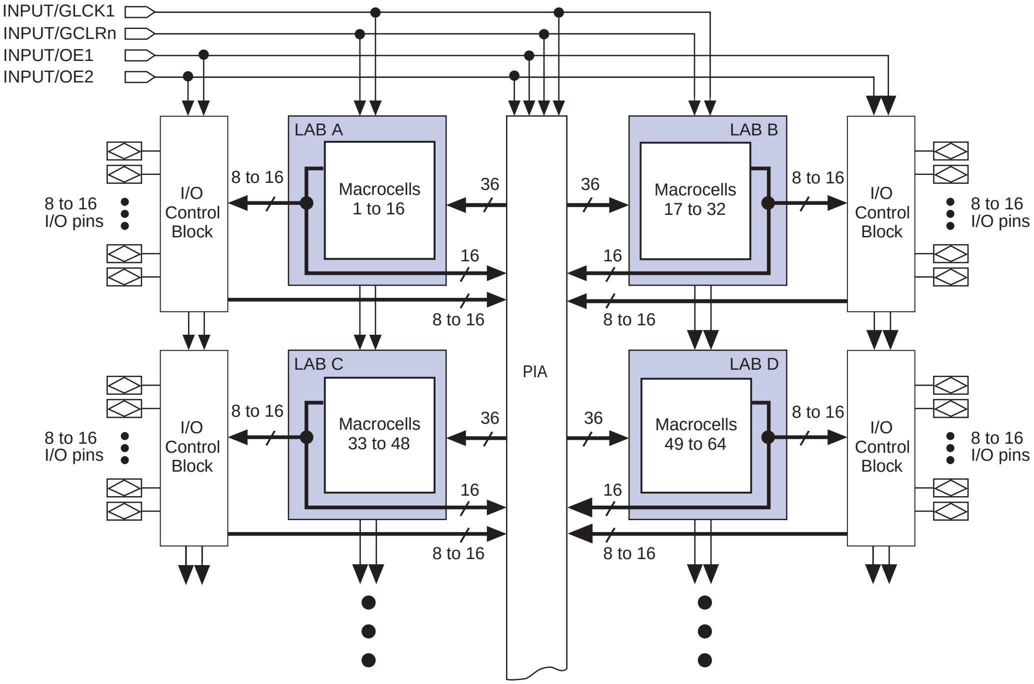
## Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

***Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram***

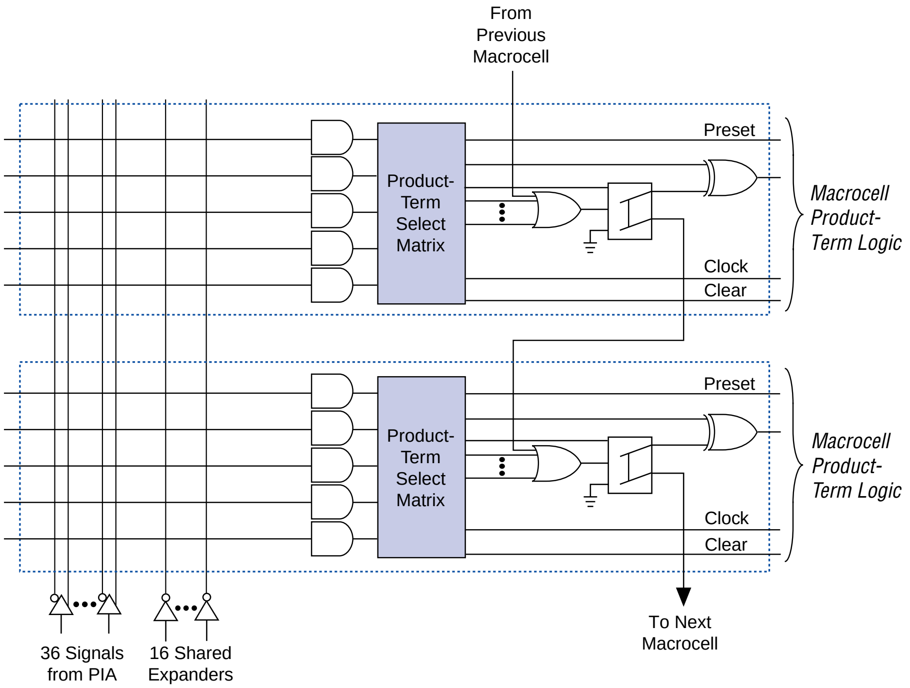


The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ($t_{PEXP}$). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

***Figure 6. Parallel Expanders***

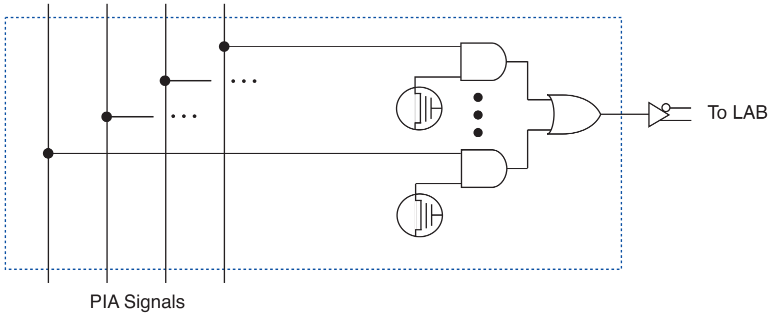
*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input `AND` gate, which selects a PIA signal to drive into the LAB.

*Figure 7. PIA Routing*



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or $V_{CC}$. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (`OE1` and `OE2`). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP*. The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.

2. *Check ID*. Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.

3. *Bulk Erase*. Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.

4. *Program*. Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.

5. *Verify*. Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.

6. *Exit ISP*. An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The programming times described in Tables 6 through 8 are associated with the worst-case method using the enhanced ISP algorithm.

**Table 6. MAX 7000S $t_{PULSE}$ & $Cycle_{TCK}$ Values**

| Device | Programming | | Stand-Alone Verification | |
|---|---|---|---|---|
| | $t_{PPULSE}$ (s) | $Cycle_{PTCK}$ | $t_{VPULSE}$ (s) | $Cycle_{VTCK}$ |
| EPM7032S | 4.02 | 342,000 | 0.03 | 200,000 |
| EPM7064S | 4.50 | 504,000 | 0.03 | 308,000 |
| EPM7128S | 5.11 | 832,000 | 0.03 | 528,000 |
| EPM7160S | 5.35 | 1,001,000 | 0.03 | 640,000 |
| EPM7192S | 5.71 | 1,192,000 | 0.03 | 764,000 |
| EPM7256S | 6.43 | 1,603,000 | 0.03 | 1,024,000 |

Tables 7 and 8 show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies**

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM7032S | 4.06 | 4.09 | 4.19 | 4.36 | 4.71 | 5.73 | 7.44 | 10.86 | s |
| EPM7064S | 4.55 | 4.60 | 4.76 | 5.01 | 5.51 | 7.02 | 9.54 | 14.58 | s |
| EPM7128S | 5.19 | 5.27 | 5.52 | 5.94 | 6.77 | 9.27 | 13.43 | 21.75 | s |
| EPM7160S | 5.45 | 5.55 | 5.85 | 6.35 | 7.35 | 10.35 | 15.36 | 25.37 | s |
| EPM7192S | 5.83 | 5.95 | 6.30 | 6.90 | 8.09 | 11.67 | 17.63 | 29.55 | s |
| EPM7256S | 6.59 | 6.75 | 7.23 | 8.03 | 9.64 | 14.45 | 22.46 | 38.49 | s |

**Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies**

| Device | $f_{TCK}$ | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | 10 MHz | 5 MHz | 2 MHz | 1 MHz | 500 kHz | 200 kHz | 100 kHz | 50 kHz | |
| EPM7032S | 0.05 | 0.07 | 0.13 | 0.23 | 0.43 | 1.03 | 2.03 | 4.03 | s |
| EPM7064S | 0.06 | 0.09 | 0.18 | 0.34 | 0.64 | 1.57 | 3.11 | 6.19 | s |
| EPM7128S | 0.08 | 0.14 | 0.29 | 0.56 | 1.09 | 2.67 | 5.31 | 10.59 | s |
| EPM7160S | 0.09 | 0.16 | 0.35 | 0.67 | 1.31 | 3.23 | 6.43 | 12.83 | s |
| EPM7192S | 0.11 | 0.18 | 0.41 | 0.79 | 1.56 | 3.85 | 7.67 | 15.31 | s |
| EPM7256S | 0.13 | 0.24 | 0.54 | 1.06 | 2.08 | 5.15 | 10.27 | 20.51 | s |

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

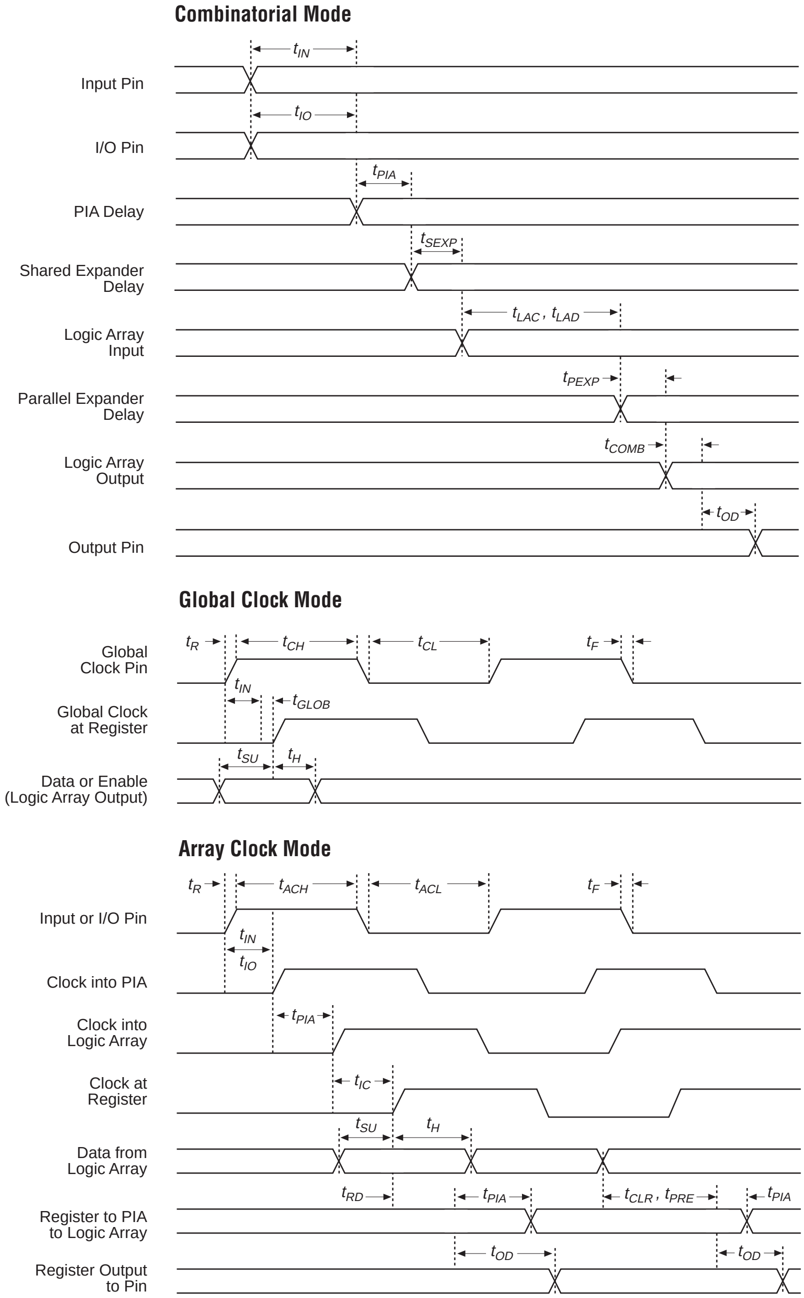
MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 9 describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (**http://www.altera.com**) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

*Table 9. MAX 7000 JTAG Instructions*

| JTAG Instruction | Devices | Description |
|---|---|---|
| SAMPLE/PRELOAD | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins. |
| EXTEST | EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation. |
| IDCODE | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | Selects the IDCODE register and places it between `TDI` and `TDO`, allowing the IDCODE to be serially shifted out of `TDO`. |
| ISP Instructions | EPM7032S<br>EPM7064S<br>EPM7128S<br>EPM7160S<br>EPM7192S<br>EPM7256S | These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (**.jam**), Jam Byte-Code file (**.jbc**), or Serial Vector Format file (**.svf**) via an embedded processor or test equipment. |

*Figure 13. Switching Waveforms*

*$t_R$ & $t_F$ < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.*



Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 19. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

| Symbol | Parameter | Conditions | -6 Speed Grade | | -7 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | ns |
| $t_{SU}$ | Global clock setup time | | 5.0 | | 6.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | *(2)* | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | *(2)* | 0.5 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | ns |
| $t_{CH}$ | Global clock high time | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.5 | | 3.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 2.5 | | 3.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 2.0 | | 2.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(3)* | 3.0 | | 3.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(4)* | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.6 | | 8.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.6 | | 8.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(5)* | 151.5 | | 125.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(6)* | 200 | | 166.7 | | MHz |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This parameter applies to MAX 7000E devices only.
(3) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.
(4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(6) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(7) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.
(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| $t_{SU}$ | Global clock setup time | | 2.9 | | 4.0 | | 5.0 | | 7.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | 0.5 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 3.2 | | 3.5 | | 4.3 | | 5.0 | ns |
| $t_{CH}$ | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CL}$ | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.7 | | 0.9 | | 1.1 | | 2.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.1 | | 2.7 | | 3.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.6 | | 8.2 | | 10.0 | ns |
| $t_{ACH}$ | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |

| *Table 27. EPM7032S External Timing Parameters (Part 2 of 2)* *Note (1)* | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | | | **Unit** |
| | | | **-5** | | **-6** | | **-7** | | **-10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 250.0 | | 200.0 | | 166.7 | | 125.0 | | MHz |

| *Table 28. EPM7032S Internal Timing Parameters* *Note (1)* | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Speed Grade** | | | | | | | | **Unit** |
| | | | **-5** | | **-6** | | **-7** | | **-10** | | |
| | | | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.2 | | 0.3 | | 0.5 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.2 | | 2.1 | | 2.5 | | 1.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.1 | | 3.8 | | 4.6 | | 5.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 0.9 | | 1.1 | | 1.4 | | 0.8 | ns |
| $t_{LAD}$ | Logic array delay | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 2.5 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 0.8 | | 1.0 | | 2.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.2 | | 0.3 | | 0.4 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.7 | | 0.8 | | 0.9 | | 2.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.2 | | 5.3 | | 5.4 | | 5.5 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 4.5 | | 5.5 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 9.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 4.0 | | 5.0 | ns |
| $t_{SU}$ | Register setup time | | 0.8 | | 1.0 | | 1.3 | | 2.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 1.8 | | 1.7 | | 3.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.7 | | 0.8 | | 0.5 | | ns |
| $t_{RD}$ | Register delay | | | 1.2 | | 1.6 | | 1.9 | | 2.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 1.1 | | 1.4 | | 2.0 | ns |
| $t_{IC}$ | Array clock delay | | | 2.7 | | 3.4 | | 4.2 | | 5.0 | ns |
| $t_{EN}$ | Register enable time | | | 2.6 | | 3.3 | | 4.0 | | 5.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 1.6 | | 1.4 | | 1.7 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.0 | | 2.4 | | 3.0 | | 3.0 | ns |

Tables 31 and 32 show the EPM7128S AC operating conditions.

***Table 31. EPM7128S External Timing Parameters*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{PD2}$ | I/O input to non-registered output | C1 = 35 pF | | 6.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{SU}$ | Global clock setup time | | 3.4 | | 6.0 | | 7.0 | | 11.0 | | ns |
| $t_{H}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{FSU}$ | Global clock setup time of fast input | | 2.5 | | 3.0 | | 3.0 | | 3.0 | | ns |
| $t_{FH}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.5 | | 0.0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 4.0 | | 4.5 | | 5.0 | | 8.0 | ns |
| $t_{CH}$ | Global clock high time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{CL}$ | Global clock low time | | 3.0 | | 3.0 | | 4.0 | | 5.0 | | ns |
| $t_{ASU}$ | Array clock setup time | | 0.9 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{AH}$ | Array clock hold time | | 1.8 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 6.5 | | 7.5 | | 10.0 | | 15.0 | ns |
| $t_{ACH}$ | Array clock high time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ACL}$ | Array clock low time | | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{CPPW}$ | Minimum pulse width for clear and preset | *(2)* | 3.0 | | 3.0 | | 4.0 | | 6.0 | | ns |
| $t_{ODH}$ | Output data hold time after clock | C1 = 35 pF *(3)* | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{CNT}$ | Maximum internal global clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 6.8 | | 8.0 | | 10.0 | | 13.0 | ns |
| $f_{ACNT}$ | Maximum internal array clock frequency | *(4)* | 147.1 | | 125.0 | | 100.0 | | 76.9 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *(5)* | 166.7 | | 166.7 | | 125.0 | | 100.0 | | MHz |

***Table 32. EPM7128S Internal Timing Parameters*** *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{IN}$ | Input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 0.2 | | 0.5 | | 0.5 | | 2.0 | ns |
| $t_{FIN}$ | Fast input delay | | | 2.6 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 3.7 | | 4.0 | | 5.0 | | 8.0 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1.1 | | 0.8 | | 0.8 | | 1.0 | ns |
| $t_{LAD}$ | Logic array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{LAC}$ | Logic control array delay | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{IOE}$ | Internal output enable delay | | | 0.7 | | 2.0 | | 2.0 | | 3.0 | ns |
| $t_{OD1}$ | Output buffer and pad delay | C1 = 35 pF | | 0.4 | | 2.0 | | 1.5 | | 4.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay | C1 = 35 pF *(6)* | | 0.9 | | 2.5 | | 2.0 | | 5.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay | C1 = 35 pF | | 5.4 | | 7.0 | | 5.5 | | 8.0 | ns |
| $t_{ZX1}$ | Output buffer enable delay | C1 = 35 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{ZX2}$ | Output buffer enable delay | C1 = 35 pF *(6)* | | 4.5 | | 4.5 | | 5.5 | | 7.0 | ns |
| $t_{ZX3}$ | Output buffer enable delay | C1 = 35 pF | | 9.0 | | 9.0 | | 9.0 | | 10.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 4.0 | | 4.0 | | 5.0 | | 6.0 | ns |
| $t_{SU}$ | Register setup time | | 1.0 | | 3.0 | | 2.0 | | 4.0 | | ns |
| $t_{H}$ | Register hold time | | 1.7 | | 2.0 | | 5.0 | | 4.0 | | ns |
| $t_{FSU}$ | Register setup time of fast input | | 1.9 | | 3.0 | | 3.0 | | 2.0 | | ns |
| $t_{FH}$ | Register hold time of fast input | | 0.6 | | 0.5 | | 0.5 | | 1.0 | | ns |
| $t_{RD}$ | Register delay | | | 1.4 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1.0 | | 1.0 | | 2.0 | | 1.0 | ns |
| $t_{IC}$ | Array clock delay | | | 3.1 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{EN}$ | Register enable time | | | 3.0 | | 3.0 | | 5.0 | | 6.0 | ns |
| $t_{GLOB}$ | Global control delay | | | 2.0 | | 1.0 | | 1.0 | | 1.0 | ns |
| $t_{PRE}$ | Register preset time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 2.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | *(7)* | | 1.4 | | 1.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | *(8)* | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

### *Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)* Note (1)

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -6 | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{CLR}$ | Register clear time | | | 2.4 | | 3.0 | | 3.0 | | 4.0 | ns |
| $t_{PIA}$ | PIA delay | (7) | | 1.6 | | 2.0 | | 1.0 | | 2.0 | ns |
| $t_{LPA}$ | Low-power adder | (8) | | 11.0 | | 10.0 | | 11.0 | | 13.0 | ns |

*Notes to tables:*

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The $t_{LPA}$ parameter must be added to this minimum width if the clear or reset signal incorporates the $t_{LAD}$ parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO}$ = 3.3 V ± 10% for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{EN}$, $t_{SEXP}$, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

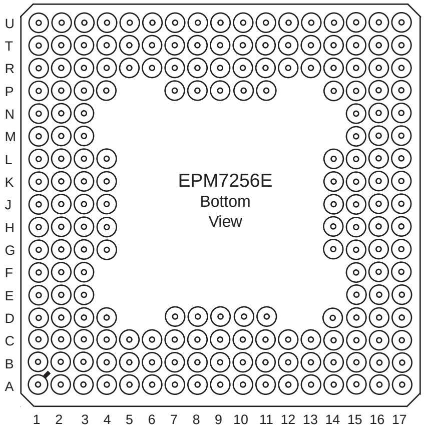
Tables 35 and 36 show the EPM7192S AC operating conditions.

### *Table 35. EPM7192S External Timing Parameters (Part 1 of 2)* Note (1)

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $\mathbf{t_{PD1}}$ | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{PD2}}$ | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| $\mathbf{t_{SU}}$ | Global clock setup time | | 4.1 | | 7.0 | | 11.0 | | ns |
| $\mathbf{t_{H}}$ | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| $\mathbf{t_{FSU}}$ | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| $\mathbf{t_{FH}}$ | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| $\mathbf{t_{CO1}}$ | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| $\mathbf{t_{CH}}$ | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{CL}}$ | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| $\mathbf{t_{ASU}}$ | Array clock setup time | | 1.0 | | 2.0 | | 4.0 | | ns |

### *Figure 21. 192-Pin Package Pin-Out Diagram*

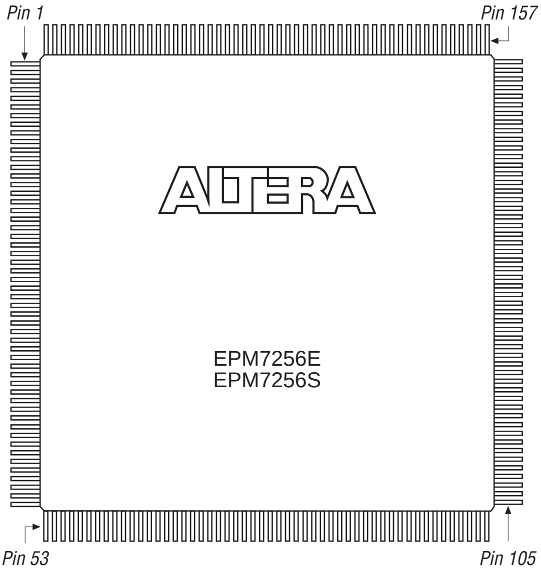
*Package outline not drawn to scale.*



192-Pin PGA

### *Figure 22. 208-Pin Package Pin-Out Diagram*

*Package outline not drawn to scale.*



208-Pin PQFP/RQFP

# Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

## Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

## Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

## Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on page 16.

## Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added *Note (5)* on page 28.

## Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.

*Notes:*