# E·XFL

### Intel - EPM7128SLC84-10 Datasheet



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#### Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

#### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128slc84-10

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#### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

#### Figure 5. Shareable Expanders



Shareable expanders can be shared by any or all macrocells in an LAB.

#### Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lowernumbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

#### Figure 6. Parallel Expanders



Unused product terms in a macrocell can be allocated to a neighboring macrocell.

### Figure 8. I/O Control Block of MAX 7000 Devices

#### EPM7032, EPM7064 & EPM7096 Devices







#### Note:

(1) The open-drain output option is available only in MAX 7000S devices.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

# In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k<sup>3</sup>4.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam<sup>™</sup> Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

# Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit<sup>TM</sup> option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ , and  $t_{SEXP}$ ,  $\mathbf{t}_{ACL}$ , and  $\mathbf{t}_{CPPW}$  parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

# MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V V<sub>CCINT</sub> level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When V<sub>CCIO</sub> is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V<sub>CCIO</sub> levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

# Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When  $V_{CCIO}$  is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

# **Slew-Rate Control**

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the Programming Hardware Manufacturers.

# Programming with External Hardware

# IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 9 describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (http://www.altera.com) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 9. MAX 7000 J	ITAG Instructions	3
JTAG Instruction	Devices	Description
SAMPLE/PRELOAD	EPM7128S EPM7160S EPM7192S EPM7256S	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	EPM7128S EPM7160S EPM7192S EPM7256S	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ISP Instructions	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File ( <b>.jam</b> ), Jam Byte-Code file ( <b>.jbc</b> ), or Serial Vector Format file ( <b>.svf</b> ) via an embedded processor or test equipment.

Table 1	5. MAX 7000 5.0-V Device DC (	<b>Operating Conditions</b> Note (9)			
Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>IH</sub>	High-level input voltage		2.0	V <sub>CCINT</sub> + 0.5	V
V <sub>IL</sub>	Low-level input voltage		-0.5 (8)	0.8	V
V <sub>OH</sub>	5.0-V high-level TTL output voltage	$I_{OH}$ = -4 mA DC, $V_{CCIO}$ = 4.75 V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4 \text{ mA DC}, V_{CCIO} = 3.00 \text{ V} (10)$	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1 \text{ mA DC}, V_{CCIO} = 3.0 \text{ V} (10)$	V <sub>CCIO</sub> – 0.2		V
V <sub>OL</sub>	5.0-V low-level TTL output voltage	$I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 4.75 V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V (11)		0.45	V
	3.3-V low-level CMOS output voltage	I <sub>OL</sub> = 0.1 mA DC, V <sub>CCIO</sub> = 3.0 V(11)		0.2	V
II.	Leakage current of dedicated input pins	$V_{I} = -0.5$ to 5.5 V (11)	-10	10	μA
I <sub>OZ</sub>	I/O pin tri-state output off-state current	V <sub>I</sub> = -0.5 to 5.5 V (11), (12)	-40	40	μA

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices    Note (13										
Symbol	Parameter	Conditions	Min	Max	Unit					
CIN	Input pin capacitance	V <sub>IN</sub> = 0 V, f = 1.0 MHz		12	pF					
C <sub>I/O</sub>	I/O pin capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		12	pF					

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices    Note (13)											
Symbol	Parameter	Conditions	Min	Max	Unit						
C <sub>IN</sub>	Input pin capacitance	V <sub>IN</sub> = 0 V, f = 1.0 MHz		15	pF						
C <sub>I/O</sub>	I/O pin capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		15	pF						

Table 1	Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices    Note (13)											
Symbol	Parameter	Conditions	Min	Max	Unit							
CIN	Dedicated input pin capacitance	V <sub>IN</sub> = 0 V, f = 1.0 MHz		10	pF							
C <sub>I/O</sub>	I/O pin capacitance	V <sub>OUT</sub> = 0 V, f = 1.0 MHz		10	pF							

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Figure 12. MAX 7000 Timing Model



#### Notes:

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more infomration, see *Application Note 94* (Understanding MAX 7000 *Timing*).

Symbol	Parameter	Conditions	Speed	Grade -6	Speed (	Grade -7	Unit
			Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			0.4		0.5	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.4		0.5	ns
t <sub>FIN</sub>	Fast input delay	(2)		0.8		1.0	ns
t <sub>SEXP</sub>	Shared expander delay			3.5		4.0	ns
t <sub>PEXP</sub>	Parallel expander delay			0.8		0.8	ns
t <sub>LAD</sub>	Logic array delay			2.0		3.0	ns
t <sub>LAC</sub>	Logic control array delay			2.0		3.0	ns
t <sub>IOE</sub>	Internal output enable delay	(2)				2.0	ns
t <sub>OD1</sub>	Output buffer and pad delay Slow slew rate = off, V <sub>CCIO</sub> = 5.0 V	C1 = 35 pF		2.0		2.0	ns
t <sub>OD2</sub>	Output buffer and pad delay Slow slew rate = off, V <sub>CCIO</sub> = 3.3 V	C1 = 35 pF (7)		2.5		2.5	ns
t <sub>OD3</sub>	Output buffer and pad delay Slow slew rate = on, V <sub>CCIO</sub> = 5.0 V or 3.3 V	C1 = 35 pF (2)		7.0		7.0	ns
t <sub>ZX1</sub>	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0 \text{ V}$	C1 = 35 pF		4.0		4.0	ns
t <sub>ZX2</sub>	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3 \text{ V}$	C1 = 35 pF (7)		4.5		4.5	ns
t <sub>ZX3</sub>	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0 V \text{ or } 3.3 V$	C1 = 35 pF (2)		9.0		9.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		4.0		4.0	ns
t <sub>SU</sub>	Register setup time		3.0		3.0		ns
t <sub>H</sub>	Register hold time		1.5		2.0		ns
t <sub>FSU</sub>	Register setup time of fast input	(2)	2.5		3.0		ns
t <sub>FH</sub>	Register hold time of fast input	(2)	0.5		0.5		ns
t <sub>RD</sub>	Register delay			0.8		1.0	ns
t <sub>COMB</sub>	Combinatorial delay			0.8		1.0	ns
t <sub>IC</sub>	Array clock delay			2.5		3.0	ns
t <sub>EN</sub>	Register enable time			2.0		3.0	ns
t <sub>GLOB</sub>	Global control delay			0.8		1.0	ns
t <sub>PRE</sub>	Register preset time			2.0		2.0	ns
t <sub>CLR</sub>	Register clear time			2.0		2.0	ns
t <sub>PIA</sub>	PIA delay			0.8		1.0	ns
t <sub>I PA</sub>	Low-power adder	(8)		10.0		10.0	ns

Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	15	-1	5T	-1	20	
			Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			2.0		2.0		3.0	ns
t <sub>IO</sub>	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t <sub>FIN</sub>	Fast input delay	(2)		2.0		-		4.0	ns
t <sub>SEXP</sub>	Shared expander delay			8.0		10.0		9.0	ns
t <sub>PEXP</sub>	Parallel expander delay			1.0		1.0		2.0	ns
t <sub>LAD</sub>	Logic array delay			6.0		6.0		8.0	ns
t <sub>LAC</sub>	Logic control array delay			6.0		6.0		8.0	ns
t <sub>IOE</sub>	Internal output enable delay	(2)		3.0		-		4.0	ns
t <sub>OD1</sub>	Output buffer and pad delay Slow slew rate = off V <sub>CCIO</sub> = 5.0 V	C1 = 35 pF		4.0		4.0		5.0	ns
t <sub>OD2</sub>	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF (7)		5.0		-		6.0	ns
t <sub>OD3</sub>	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0 V \text{ or } 3.3 V$	C1 = 35 pF (2)		8.0		-		9.0	ns
t <sub>ZX1</sub>	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0 V$	C1 = 35 pF		6.0		6.0		10.0	ns
t <sub>ZX2</sub>	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF (7)		7.0		-		11.0	ns
t <sub>ZX3</sub>	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0 V \text{ or } 3.3 V$	C1 = 35 pF (2)		10.0		-		14.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		6.0		6.0		10.0	ns
t <sub>SU</sub>	Register setup time		4.0		4.0		4.0		ns
t <sub>H</sub>	Register hold time		4.0		4.0		5.0		ns
t <sub>FSU</sub>	Register setup time of fast input	(2)	2.0		-		4.0		ns
t <sub>FH</sub>	Register hold time of fast input	(2)	2.0		-		3.0		ns
t <sub>RD</sub>	Register delay			1.0		1.0		1.0	ns
t <sub>COMB</sub>	Combinatorial delay			1.0		1.0		1.0	ns
t <sub>IC</sub>	Array clock delay			6.0		6.0		8.0	ns
t <sub>EN</sub>	Register enable time			6.0		6.0		8.0	ns
t <sub>GLOB</sub>	Global control delay			1.0		1.0		3.0	ns
t <sub>PRE</sub>	Register preset time			4.0		4.0		4.0	ns
t <sub>CLR</sub>	Register clear time			4.0		4.0		4.0	ns
t <sub>PIA</sub>	PIA delay			2.0		2.0		3.0	ns
t <sub>LPA</sub>	Low-power adder	(8)		13.0		15.0		15.0	ns

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t<sub>LPA</sub> parameter must be added to this minimum width if the clear or reset signal incorporates the t<sub>LAD</sub> parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

#### Tables 27 and 28 show the EPM7032S AC operating conditions.

Symbol	Parameter	Conditions	Speed Grade								
			-	-5		-6		7	-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		4.0		5.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		1.1		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.7		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
<b>t</b> ACNT	Minimum array clock period			5.7		7.0		8.6		10.0	ns

Table 2	9. EPM7064S External Timi	ing Parameters	(Part 2	2 of 2)	No	te (1)					
Symbol	Parameter	Conditions	Speed Grade								
			-	5	-	6	-	7	-1	0	
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

# Г

 

 Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)

Note (1)

Symbol	Parameter	Conditions	Speed Grade								
			-	5	-	6	-	7	-1	10	-
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t <sub>IO</sub>	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t <sub>FIN</sub>	Fast input delay			2.2		2.6		1.0		1.0	ns
t <sub>SEXP</sub>	Shared expander delay			3.1		3.8		4.0		5.0	ns
t <sub>PEXP</sub>	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t <sub>LAD</sub>	Logic array delay			2.6		3.2		3.0		5.0	ns
t <sub>LAC</sub>	Logic control array delay			2.5		3.2		3.0		5.0	ns
t <sub>IOE</sub>	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t <sub>OD1</sub>	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t <sub>OD2</sub>	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t <sub>OD3</sub>	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t <sub>ZX1</sub>	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t <sub>ZX2</sub>	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t <sub>ZX3</sub>	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t <sub>XZ</sub>	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t <sub>SU</sub>	Register setup time		0.8		1.0		3.0		2.0		ns
t <sub>H</sub>	Register hold time		1.7		2.0		2.0		3.0		ns

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t<sub>LPA</sub> parameter must be added to this minimum width if the clear or reset signal incorporates the t<sub>LAD</sub> parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

#### Tables 33 and 34 show the EPM7160S AC operating conditions.

Table 3	3. EPM7160S External Timi	ing Parameters	(Part	1 of 2)	No	te (1)					
Symbol	Parameter	Conditions				Speed	Grade	)			Unit
			-	6	-	7	-1	0	-1	15	
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.4		4.2		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.9		4.8		5		8	ns
t <sub>CH</sub>	Global clock high time		3.0		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.9		1.1		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.7		2.1		3.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		6.4		7.9		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			6.7		8.2		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	149.3		122.0		100.0		76.9		MHz

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Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2)    Note (1)										
Symbol	Parameter	Conditions	Speed Grade					Unit		
			-7		-10		-15			
			Min	Max	Min	Max	Min	Max		
t <sub>H</sub>	Register hold time		1.7		3.0		4.0		ns	
t <sub>FSU</sub>	Register setup time of fast input		2.3		3.0		2.0		ns	
t <sub>FH</sub>	Register hold time of fast input		0.7		0.5		1.0		ns	
t <sub>RD</sub>	Register delay			1.4		2.0		1.0	ns	
t <sub>COMB</sub>	Combinatorial delay			1.2		2.0		1.0	ns	
t <sub>IC</sub>	Array clock delay			3.2		5.0		6.0	ns	
t <sub>EN</sub>	Register enable time			3.1		5.0		6.0	ns	
t <sub>GLOB</sub>	Global control delay			2.5		1.0		1.0	ns	
t <sub>PRE</sub>	Register preset time			2.7		3.0		4.0	ns	
t <sub>CLR</sub>	Register clear time			2.7		3.0		4.0	ns	
t <sub>PIA</sub>	PIA delay	(7)		2.4		1.0		2.0	ns	
t <sub>LPA</sub>	Low-power adder	(8)		10.0		11.0		13.0	ns	

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t<sub>LPA</sub> parameter must be added to this minimum width if the clear or reset signal incorporates the t<sub>LAD</sub> parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t<sub>LPA</sub> parameter must be added to this minimum width if the clear or reset signal incorporates the t<sub>LAD</sub> parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

# Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$  in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note* 74 (*Evaluating Power for Altera Devices*).

The I<sub>CCINT</sub> value, which depends on the switching frequency and the application logic, is calculated with the following equation:

 $I_{CCINT} =$ 

 $A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times tog_{LC}$ 

The parameters in this equation are shown below:

MC <sub>TON</sub>	=	Number of macrocells with the Turbo Bit option turned on,
		as reported in the MAX+PLUS II Report File (.rpt)
MC <sub>DEV</sub>	=	Number of macrocells in the device
MC <sub>USED</sub>	=	Total number of macrocells in the design, as reported
		in the MAX+PLUS II Report File ( <b>.rpt</b> )
f <sub>MAX</sub>	=	Highest clock frequency to the device
tog <sub>LC</sub>	=	Average ratio of logic cells toggling at each clock
		(typically 0.125)
A, B, C	=	Constants, shown in Table 39

Table 39. MAX 7000 I <sub>CC</sub> Equation Constants									
Device	Α	В	C						
EPM7032	1.87	0.52	0.144						
EPM7064	1.63	0.74	0.144						
EPM7096	1.63	0.74	0.144						
EPM7128E	1.17	0.54	0.096						
EPM7160E	1.17	0.54	0.096						
EPM7192E	1.17	0.54	0.096						
EPM7256E	1.17	0.54	0.096						
EPM7032S	0.93	0.40	0.040						
EPM7064S	0.93	0.40	0.040						
EPM7128S	0.93	0.40	0.040						
EPM7160S	0.93	0.40	0.040						
EPM7192S	0.93	0.40	0.040						
EPM7256S	0.93	0.40	0.040						

This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions. Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

#### Figure 16. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

#### Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



84-Pin PLCC

Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

# Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

### Version 6.7

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.7:

Reference to AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor has been replaced by AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor.

### Version 6.6

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

### Version 6.5

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.5:

Updated text on page 16.

#### Version 6.4

The following changes were made in the *MAX* 7000 Programmable Logic Device Family Data Sheet version 6.4:

Added Note (5) on page 28.

### Version 6.3

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.3:

 Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.