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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	68
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128slc84-10n">https://www.e-xfl.com/product-detail/intel/epm7128slc84-10n</a>

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

## Functional Description

The MAX 7000 architecture includes the following elements:

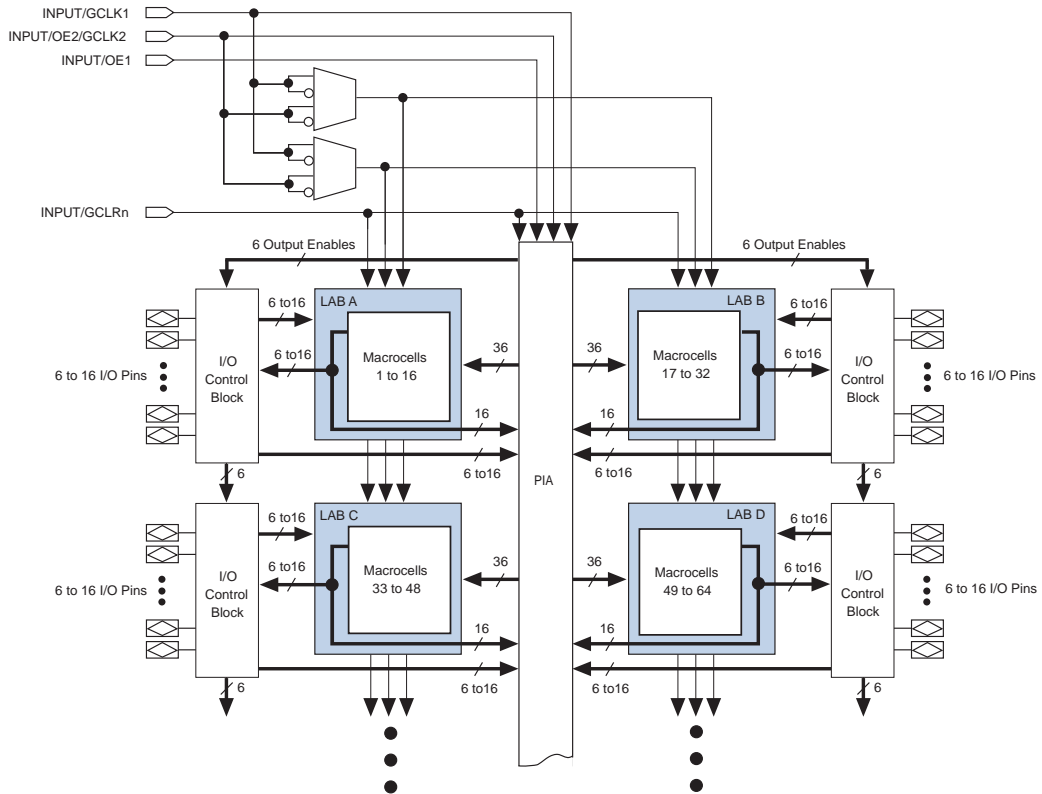
- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

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The diagram illustrates the PIA architecture, showing four LABs (A, B, C, D) connected to a central PIA block. Each LAB contains macrocells (1-16, 17-32, 33-48, 49-64) and is interfaced with I/O Control Blocks. The diagram illustrates the flow of data and control signals between the PIA and the LABs, including 8 to 16 I/O pins and 36-bit data paths.

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**



## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

## Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

**Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell**

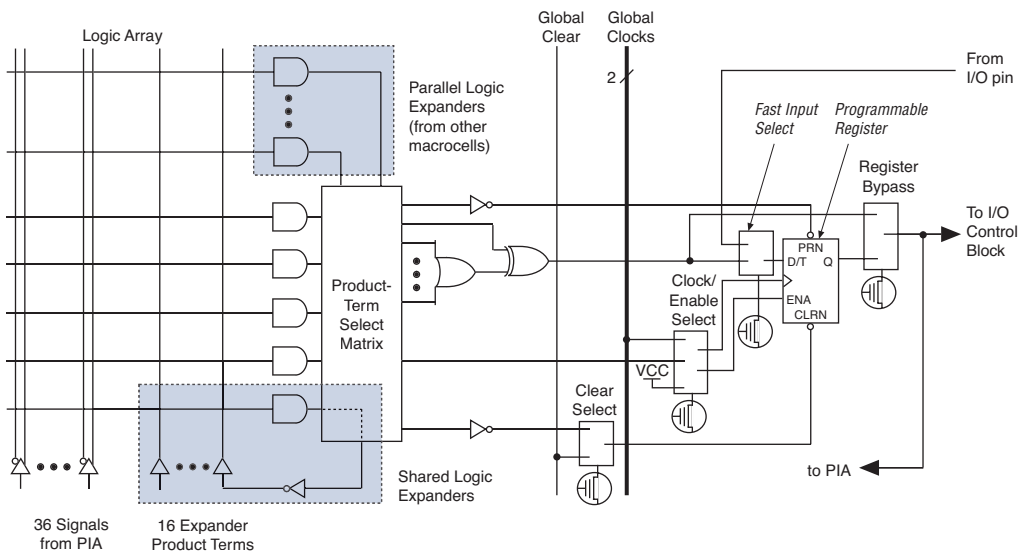
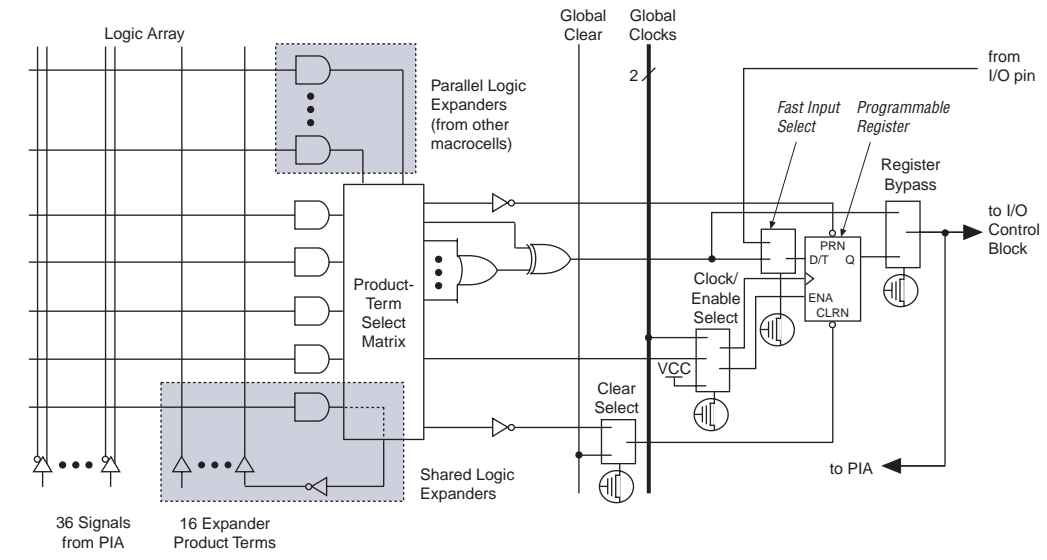


Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

**Figure 4. MAX 7000E & MAX 7000S Device Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

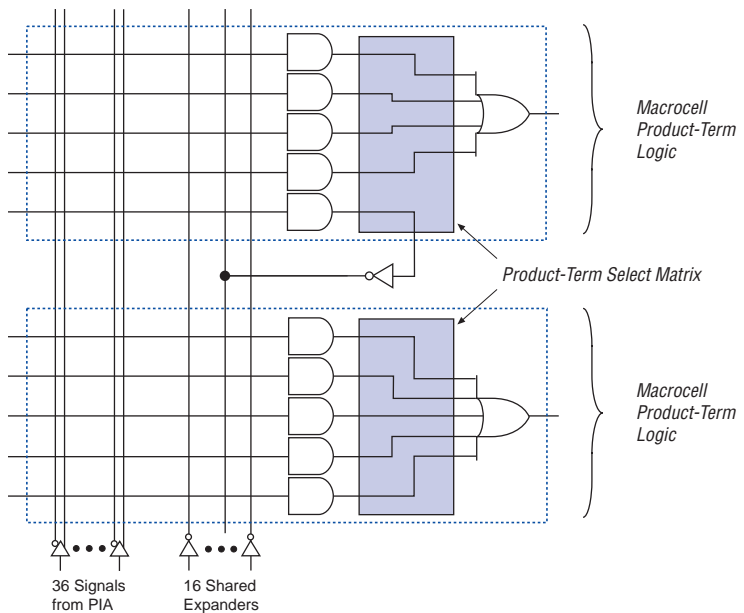
For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

**Figure 5. Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.



The programming times described in [Tables 6 through 8](#) are associated with the worst-case method using the enhanced ISP algorithm.

**Table 6. MAX 7000S  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

[Tables 7](#) and [8](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

**Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

**Table 10. MAX 7000S Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM7032S	1 (1)
EPM7064S	1 (1)
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

**Note:**

- (1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

**Table 11. 32-Bit MAX 7000 Device IDCODE** Note (1)

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.  
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Figure 9 shows the timing requirements for the JTAG signals.

**Figure 9. MAX 7000 JTAG Waveforms**

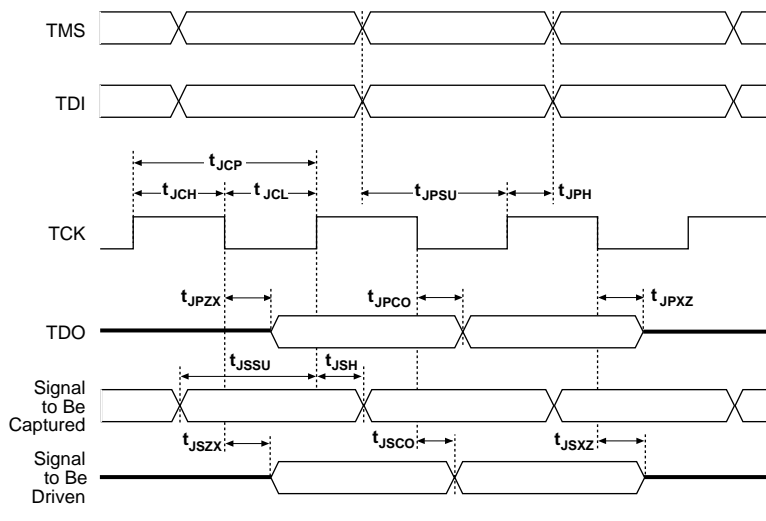


Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

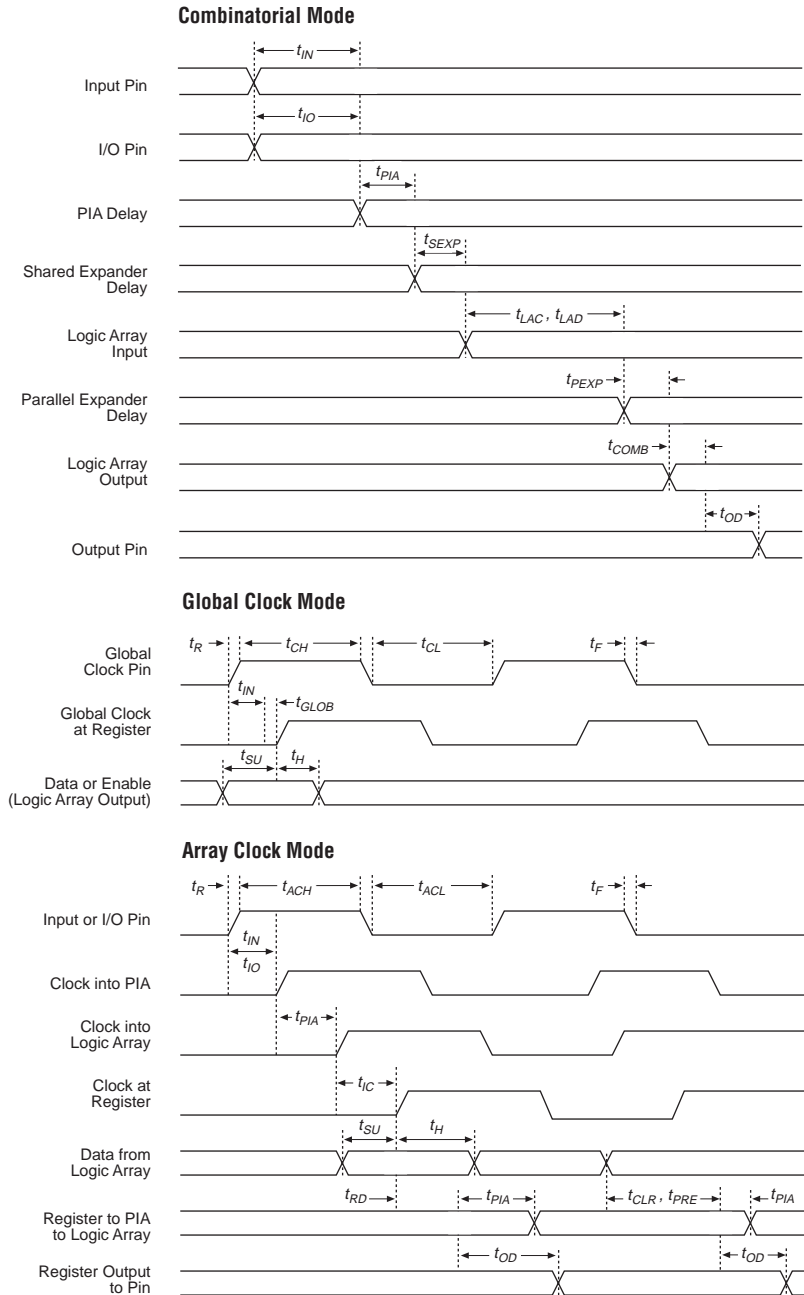
<b>Table 12. JTAG Timing Parameters &amp; Values for MAX 7000S Devices</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns



For more information, see [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#).

**Figure 13. Switching Waveforms**

$t_R$  &  $t_F < 3$  ns.  
Inputs are driven at 3 V  
for a logic high and 0 V  
for a logic low. All timing  
characteristics are  
measured at 1.5 V.



**Table 21. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		8.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.5		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		2.0		3.0		ns
t <sub>AH</sub>	Array clock hold time		3.0		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t <sub>ACH</sub>	Array clock high time		4.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		4.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			10.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			10.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

**Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.5		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.5		1.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			5.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.8		0.8	ns
$t_{LAD}$	Logic array delay			5.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.5		2.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		2.5	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.5		6.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		5.0		5.0	ns
$t_{SU}$	Register setup time		2.0		3.0		ns
$t_H$	Register hold time		3.0		3.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.5		0.5		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			5.0		5.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0	ns
$t_{PRE}$	Register preset time			3.0		3.0	ns
$t_{CLR}$	Register clear time			3.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		11.0	ns

**Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			1.0		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			1.0		2.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			7.0		7.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0	ns
$t_{LAD}$	Logic array delay			7.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
$t_{SU}$	Register setup time		1.0		4.0		ns
$t_H$	Register hold time		6.0		4.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	4.0		2.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.0		2.0		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			7.0		5.0	ns
$t_{GLOB}$	Global control delay			2.0		0.0	ns
$t_{PRE}$	Register preset time			4.0		3.0	ns
$t_{CLR}$	Register clear time			4.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		12.0	ns

Table 25. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>SU</sub>	Global clock setup time		11.0		11.0		12.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		–		5.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		–		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t <sub>CH</sub>	Global clock high time		5.0		6.0		6.0		ns
t <sub>CL</sub>	Global clock low time		5.0		6.0		6.0		ns
t <sub>ASU</sub>	Array clock setup time		4.0		4.0		5.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		5.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t <sub>ACH</sub>	Array clock high time		6.0		6.5		8.0		ns
t <sub>ACL</sub>	Array clock low time		6.0		6.5		8.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	6.0		6.5		8.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			13.0		13.0		16.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	76.9		76.9		62.5		MHz
t <sub>ACNT</sub>	Minimum array clock period			13.0		13.0		16.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	76.9		76.9		62.5		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	100		83.3		83.3		MHz



**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		4.0		5.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		1.1		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.7		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.0		8.6		10.0	ns

**Table 27. EPM7032S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.3		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.3		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.1		2.5		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.6		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		1.4		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.3		4.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.3		4.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		1.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		0.4		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		0.9		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		5.4		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		1.3		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.5		3.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		1.8		1.7		3.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.7		0.8		0.5		ns
$t_{RD}$	Register delay			1.2		1.6		1.9		2.0	ns
$t_{COMB}$	Combinatorial delay			0.9		1.1		1.4		2.0	ns
$t_{IC}$	Array clock delay			2.7		3.4		4.2		5.0	ns
$t_{EN}$	Register enable time			2.6		3.3		4.0		5.0	ns
$t_{GLOB}$	Global control delay			1.6		1.4		1.7		1.0	ns
$t_{PRE}$	Register preset time			2.0		2.4		3.0		3.0	ns
$t_{CLR}$	Register clear time			2.0		2.4		3.0		3.0	ns

**Table 29. EPM7064S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.6		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.2		3.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.2		3.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		3.0		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.0		3.0		ns

**Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLR}$	Register clear time			2.4		3.0		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		1.6		2.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

**Table 35. EPM7192S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		4.1		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		1.0		2.0		4.0		ns

## Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

### Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

### Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

### Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

### Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

### Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).