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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

| | |
|---------------------------------|---|
| Product Status | Obsolete |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 6 ns |
| Voltage Supply - Internal | 4.75V ~ 5.25V |
| Number of Logic Elements/Blocks | 8 |
| Number of Macrocells | 128 |
| Number of Gates | 2500 |
| Number of I/O | 68 |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm7128slc84-6n |

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
 - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
 - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

Table 3. MAX 7000 Speed Grades

| Device | Speed Grade | | | | | | | | | |
|----------|-------------|----|----|------|-----|------|-----|-----|------|-----|
| | -5 | -6 | -7 | -10P | -10 | -12P | -12 | -15 | -15T | -20 |
| EPM7032 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | ✓ | |
| EPM7032S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7064 | | ✓ | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7064S | ✓ | ✓ | ✓ | | ✓ | | | | | |
| EPM7096 | | | ✓ | | ✓ | | ✓ | ✓ | | |
| EPM7128E | | | ✓ | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7128S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7160E | | | | ✓ | ✓ | | ✓ | ✓ | | ✓ |
| EPM7160S | | ✓ | ✓ | | ✓ | | | ✓ | | |
| EPM7192E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7192S | | | ✓ | | ✓ | | | ✓ | | |
| EPM7256E | | | | | | ✓ | ✓ | ✓ | | ✓ |
| EPM7256S | | | ✓ | | ✓ | | | ✓ | | |

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

| Device | 44-Pin PLCC | 44-Pin PQFP | 44-Pin TQFP | 68-Pin PLCC | 84-Pin PLCC | 100-Pin PQFP | 100-Pin TQFP | 160-Pin PQFP | 160-Pin PGA | 192-Pin PGA | 208-Pin PQFP | 208-Pin RQFP |
|----------|----------------|----------------|----------------|----------------|----------------|-----------------|-----------------|-----------------|----------------|----------------|-----------------|-----------------|
| EPM7032 | 36 | 36 | 36 | | | | | | | | | |
| EPM7032S | 36 | | 36 | | | | | | | | | |
| EPM7064 | 36 | | 36 | 52 | 68 | 68 | | | | | | |
| EPM7064S | 36 | | 36 | | 68 | | 68 | | | | | |
| EPM7096 | | | | 52 | 64 | 76 | | | | | | |
| EPM7128E | | | | | 68 | 84 | | 100 | | | | |
| EPM7128S | | | | | 68 | 84 | 84 (2) | 100 | | | | |
| EPM7160E | | | | | 64 | 84 | | 104 | | | | |
| EPM7160S | | | | | 64 | | 84 (2) | 104 | | | | |
| EPM7192E | | | | | | | | 124 | 124 | | | |
| EPM7192S | | | | | | | | 124 | | | | |
| EPM7256E | | | | | | | | 132 (2) | | 164 | | 164 |
| EPM7256S | | | | | | | | | | | 164 (2) | 164 |

Notes:

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

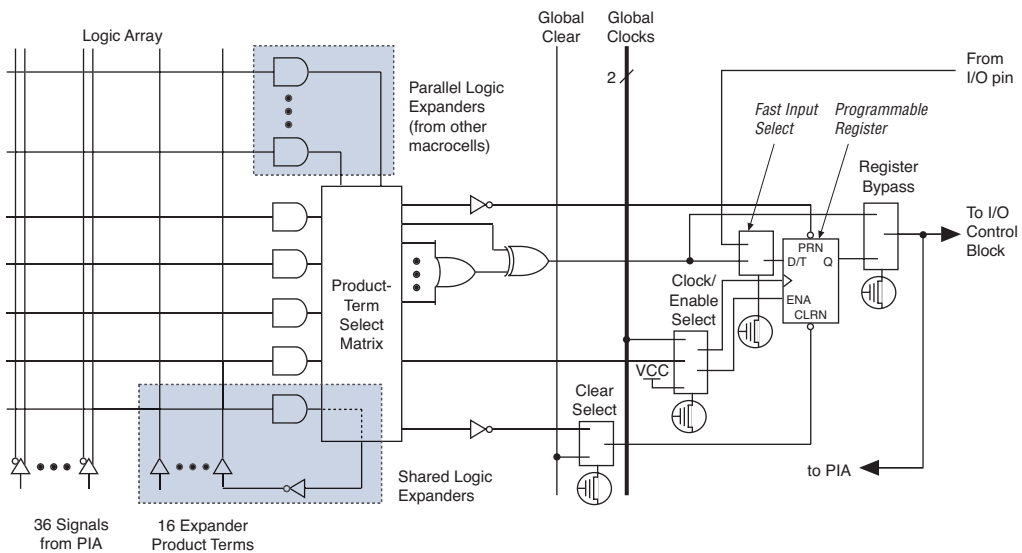
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

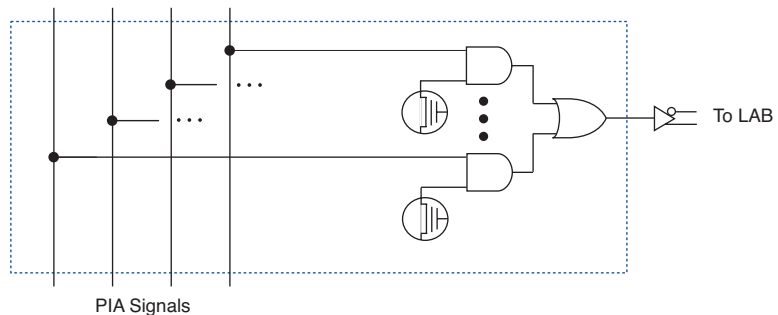
Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell



Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000S Device

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , and t_{SEXP} , t_{ACL} , and t_{CPPW} parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} .

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [Programming Hardware Manufacturers](#).

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

Table 10. MAX 7000S Boundary-Scan Register Length

| Device | Boundary-Scan Register Length |
|----------|-------------------------------|
| EPM7032S | 1 (1) |
| EPM7064S | 1 (1) |
| EPM7128S | 288 |
| EPM7160S | 312 |
| EPM7192S | 360 |
| EPM7256S | 480 |

Note:

- (1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

Table 11. 32-Bit MAX 7000 Device IDCODE Note (1)

| Device | IDCODE (32 Bits) | | | | 1 (1 Bit) (2) |
|----------|---------------------|-----------------------|--------------------------------------|--|------------------|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer's Identity (11 Bits) | | |
| EPM7032S | 0000 | 0111 0000 0011 0010 | 00001101110 | | 1 |
| EPM7064S | 0000 | 0111 0000 0110 0100 | 00001101110 | | 1 |
| EPM7128S | 0000 | 0111 0001 0010 1000 | 00001101110 | | 1 |
| EPM7160S | 0000 | 0111 0001 0110 0000 | 00001101110 | | 1 |
| EPM7192S | 0000 | 0111 0001 1001 0010 | 00001101110 | | 1 |
| EPM7256S | 0000 | 0111 0010 0101 0110 | 00001101110 | | 1 |

Notes:

- (1) The most significant bit (MSB) is on the left.
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|------------|---|------------------|------------------|------|-----------------------------------|------|------|
| | | | MAX 7000E (-10P) | | MAX 7000 (-10) MAX 7000E (-10) | | |
| | | | Min | Max | Min | Max | |
| t_{IN} | Input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 0.5 | | 1.0 | ns |
| t_{FIN} | Fast input delay | (2) | | 1.0 | | 1.0 | ns |
| t_{SEXP} | Shared expander delay | | | 5.0 | | 5.0 | ns |
| t_{PEXP} | Parallel expander delay | | | 0.8 | | 0.8 | ns |
| t_{LAD} | Logic array delay | | | 5.0 | | 5.0 | ns |
| t_{LAC} | Logic control array delay | | | 5.0 | | 5.0 | ns |
| t_{IOE} | Internal output enable delay | (2) | | 2.0 | | 2.0 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 1.5 | | 2.0 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF (7) | | 2.0 | | 2.5 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF (2) | | 5.5 | | 6.0 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V | $C1 = 35$ pF | | 5.0 | | 5.0 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V | $C1 = 35$ pF (7) | | 5.5 | | 5.5 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V | $C1 = 35$ pF (2) | | 9.0 | | 9.0 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5$ pF | | 5.0 | | 5.0 | ns |
| t_{SU} | Register setup time | | 2.0 | | 3.0 | | ns |
| t_H | Register hold time | | 3.0 | | 3.0 | | ns |
| t_{FSU} | Register setup time of fast input | (2) | 3.0 | | 3.0 | | ns |
| t_{FH} | Register hold time of fast input | (2) | 0.5 | | 0.5 | | ns |
| t_{RD} | Register delay | | | 2.0 | | 1.0 | ns |
| t_{COMB} | Combinatorial delay | | | 2.0 | | 1.0 | ns |
| t_{IC} | Array clock delay | | | 5.0 | | 5.0 | ns |
| t_{EN} | Register enable time | | | 5.0 | | 5.0 | ns |
| t_{GLOB} | Global control delay | | | 1.0 | | 1.0 | ns |
| t_{PRE} | Register preset time | | | 3.0 | | 3.0 | ns |
| t_{CLR} | Register clear time | | | 3.0 | | 3.0 | ns |
| t_{PIA} | PIA delay | | | 1.0 | | 1.0 | ns |
| t_{LPA} | Low-power adder | (8) | | 11.0 | | 11.0 | ns |

Table 23. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | Unit |
|-------------------|--|----------------|------------------|------|-----------------------------------|------|------|
| | | | MAX 7000E (-12P) | | MAX 7000 (-12) MAX 7000E (-12) | | |
| | | | Min | Max | Min | Max | |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| t _{SU} | Global clock setup time | | 7.0 | | 10.0 | | ns |
| t _H | Global clock hold time | | 0.0 | | 0.0 | | ns |
| t _{FSU} | Global clock setup time of fast input | (2) | 3.0 | | 3.0 | | ns |
| t _{FH} | Global clock hold time of fast input | (2) | 0.0 | | 0.0 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 6.0 | | 6.0 | ns |
| t _{CH} | Global clock high time | | 4.0 | | 4.0 | | ns |
| t _{CL} | Global clock low time | | 4.0 | | 4.0 | | ns |
| t _{ASU} | Array clock setup time | | 3.0 | | 4.0 | | ns |
| t _{AH} | Array clock hold time | | 4.0 | | 4.0 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 12.0 | | 12.0 | ns |
| t _{ACH} | Array clock high time | | 5.0 | | 5.0 | | ns |
| t _{ACL} | Array clock low time | | 5.0 | | 5.0 | | ns |
| t _{CPPW} | Minimum pulse width for clear and preset | (3) | 5.0 | | 5.0 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF (4) | 1.0 | | 1.0 | | ns |
| t _{CNT} | Minimum global clock period | | | 11.0 | | 11.0 | ns |
| f _{CNT} | Maximum internal global clock frequency | (5) | 90.9 | | 90.9 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 11.0 | | 11.0 | ns |
| f _{ACNT} | Maximum internal array clock frequency | (5) | 90.9 | | 90.9 | | MHz |
| f _{MAX} | Maximum clock frequency | (6) | 125.0 | | 125.0 | | MHz |

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|------------|---|-------------------------|-------------|------|------|------|-----|------|------|
| | | | -15 | | -15T | | -20 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t_{IN} | Input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| t_{IO} | I/O input pad and buffer delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| t_{FIN} | Fast input delay | (2) | | 2.0 | | — | | 4.0 | ns |
| t_{SEXP} | Shared expander delay | | | 8.0 | | 10.0 | | 9.0 | ns |
| t_{PEXP} | Parallel expander delay | | | 1.0 | | 1.0 | | 2.0 | ns |
| t_{LAD} | Logic array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| t_{LAC} | Logic control array delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| t_{IOE} | Internal output enable delay | (2) | | 3.0 | | — | | 4.0 | ns |
| t_{OD1} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 4.0 | | 4.0 | | 5.0 | ns |
| t_{OD2} | Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$ (7) | | 5.0 | | — | | 6.0 | ns |
| t_{OD3} | Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$ (2) | | 8.0 | | — | | 9.0 | ns |
| t_{ZX1} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$ | $C1 = 35\text{ pF}$ | | 6.0 | | 6.0 | | 10.0 | ns |
| t_{ZX2} | Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$ | $C1 = 35\text{ pF}$ (7) | | 7.0 | | — | | 11.0 | ns |
| t_{ZX3} | Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V | $C1 = 35\text{ pF}$ (2) | | 10.0 | | — | | 14.0 | ns |
| t_{XZ} | Output buffer disable delay | $C1 = 5\text{ pF}$ | | 6.0 | | 6.0 | | 10.0 | ns |
| t_{SU} | Register setup time | | 4.0 | | 4.0 | | 4.0 | | ns |
| t_H | Register hold time | | 4.0 | | 4.0 | | 5.0 | | ns |
| t_{FSU} | Register setup time of fast input | (2) | 2.0 | | — | | 4.0 | | ns |
| t_{FH} | Register hold time of fast input | (2) | 2.0 | | — | | 3.0 | | ns |
| t_{RD} | Register delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| t_{COMB} | Combinatorial delay | | | 1.0 | | 1.0 | | 1.0 | ns |
| t_{IC} | Array clock delay | | | 6.0 | | 6.0 | | 8.0 | ns |
| t_{EN} | Register enable time | | | 6.0 | | 6.0 | | 8.0 | ns |
| t_{GLOB} | Global control delay | | | 1.0 | | 1.0 | | 3.0 | ns |
| t_{PRE} | Register preset time | | | 4.0 | | 4.0 | | 4.0 | ns |
| t_{CLR} | Register clear time | | | 4.0 | | 4.0 | | 4.0 | ns |
| t_{PIA} | PIA delay | | | 2.0 | | 2.0 | | 3.0 | ns |
| t_{LPA} | Low-power adder | (8) | | 13.0 | | 15.0 | | 15.0 | ns |

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The f_{MAX} values represent the highest frequency for pipelined data.
- (7) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

Table 27. EPM7032S External Timing Parameters (Part 1 of 2) *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | | | Unit |
|-------------------|--|----------------|-------------|-----|-------|-----|-------|-----|-------|------|------|
| | | | -5 | | -6 | | -7 | | -10 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 5.0 | | 6.0 | | 7.5 | | 10.0 | ns |
| t _{SU} | Global clock setup time | | 2.9 | | 4.0 | | 5.0 | | 7.0 | | ns |
| t _H | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{FSU} | Global clock setup time of fast input | | 2.5 | | 2.5 | | 2.5 | | 3.0 | | ns |
| t _{FH} | Global clock hold time of fast input | | 0.0 | | 0.0 | | 0.0 | | 0.5 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 3.2 | | 3.5 | | 4.3 | | 5.0 | ns |
| t _{CH} | Global clock high time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| t _{CL} | Global clock low time | | 2.0 | | 2.5 | | 3.0 | | 4.0 | | ns |
| t _{ASU} | Array clock setup time | | 0.7 | | 0.9 | | 1.1 | | 2.0 | | ns |
| t _{AH} | Array clock hold time | | 1.8 | | 2.1 | | 2.7 | | 3.0 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 5.4 | | 6.6 | | 8.2 | | 10.0 | ns |
| t _{ACH} | Array clock high time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| t _{ACL} | Array clock low time | | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| t _{CPPW} | Minimum pulse width for clear and preset | (2) | 2.5 | | 2.5 | | 3.0 | | 4.0 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF (3) | 1.0 | | 1.0 | | 1.0 | | 1.0 | | ns |
| t _{CNT} | Minimum global clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |
| f _{CNT} | Maximum internal global clock frequency | (4) | 175.4 | | 142.9 | | 116.3 | | 100.0 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 5.7 | | 7.0 | | 8.6 | | 10.0 | ns |

Tables 37 and 38 show the EPM7256S AC operating conditions.

Table 37. EPM7256S External Timing Parameters *Note (1)*

| Symbol | Parameter | Conditions | Speed Grade | | | | | | Unit |
|-------------------|--|----------------|-------------|-----|-------|------|-------|------|------|
| | | | -7 | | -10 | | -15 | | |
| | | | Min | Max | Min | Max | Min | Max | |
| t _{PD1} | Input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| t _{PD2} | I/O input to non-registered output | C1 = 35 pF | | 7.5 | | 10.0 | | 15.0 | ns |
| t _{SU} | Global clock setup time | | 3.9 | | 7.0 | | 11.0 | | ns |
| t _H | Global clock hold time | | 0.0 | | 0.0 | | 0.0 | | ns |
| t _{FSU} | Global clock setup time of fast input | | 3.0 | | 3.0 | | 3.0 | | ns |
| t _{FH} | Global clock hold time of fast input | | 0.0 | | 0.5 | | 0.0 | | ns |
| t _{CO1} | Global clock to output delay | C1 = 35 pF | | 4.7 | | 5.0 | | 8.0 | ns |
| t _{CH} | Global clock high time | | 3.0 | | 4.0 | | 5.0 | | ns |
| t _{CL} | Global clock low time | | 3.0 | | 4.0 | | 5.0 | | ns |
| t _{ASU} | Array clock setup time | | 0.8 | | 2.0 | | 4.0 | | ns |
| t _{AH} | Array clock hold time | | 1.9 | | 3.0 | | 4.0 | | ns |
| t _{ACO1} | Array clock to output delay | C1 = 35 pF | | 7.8 | | 10.0 | | 15.0 | ns |
| t _{ACH} | Array clock high time | | 3.0 | | 4.0 | | 6.0 | | ns |
| t _{ACL} | Array clock low time | | 3.0 | | 4.0 | | 6.0 | | ns |
| t _{CPPW} | Minimum pulse width for clear and preset | (2) | 3.0 | | 4.0 | | 6.0 | | ns |
| t _{ODH} | Output data hold time after clock | C1 = 35 pF (3) | 1.0 | | 1.0 | | 1.0 | | ns |
| t _{CNT} | Minimum global clock period | | | 7.8 | | 10.0 | | 13.0 | ns |
| f _{CNT} | Maximum internal global clock frequency | (4) | 128.2 | | 100.0 | | 76.9 | | MHz |
| t _{ACNT} | Minimum array clock period | | | 7.8 | | 10.0 | | 13.0 | ns |
| f _{ACNT} | Maximum internal array clock frequency | (4) | 128.2 | | 100.0 | | 76.9 | | MHz |
| f _{MAX} | Maximum clock frequency | (5) | 166.7 | | 125.0 | | 100.0 | | MHz |

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in [Table 14](#). See [Figure 13](#) for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPTW} parameters for macrocells running in the low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The I_{CCINT} value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC}$$

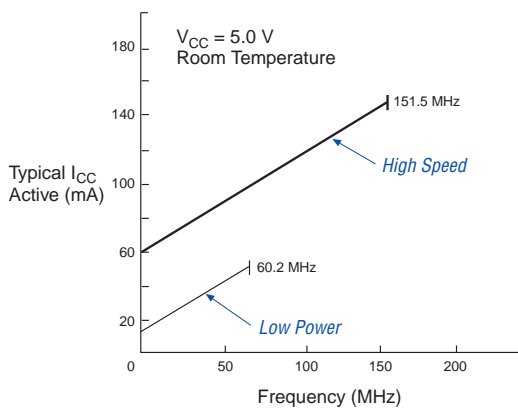
The parameters in this equation are shown below:

| | | |
|-------------------|---|---|
| MC_{TON} | = | Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt) |
| MC_{DEV} | = | Number of macrocells in the device |
| MC_{USED} | = | Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt) |
| f_{MAX} | = | Highest clock frequency to the device |
| tog_{LC} | = | Average ratio of logic cells toggling at each clock (typically 0.125) |
| A, B, C | = | Constants, shown in Table 39 |

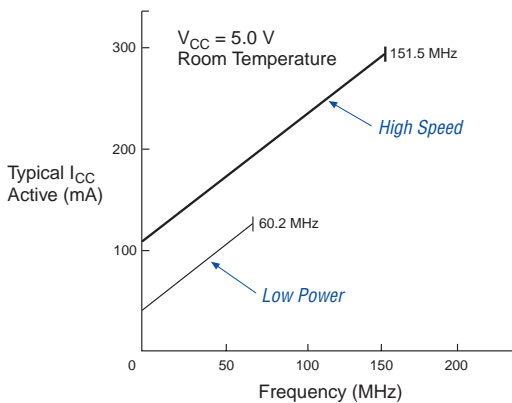
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

EPM7032



EPM7064



EPM7096

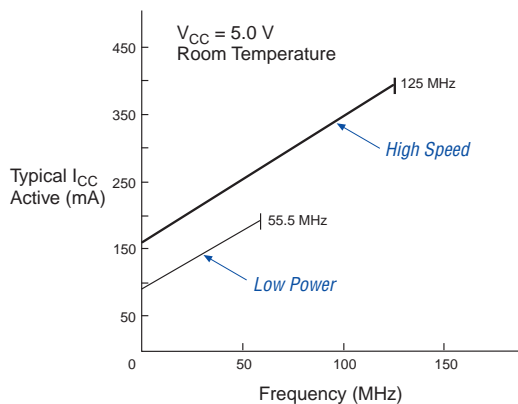
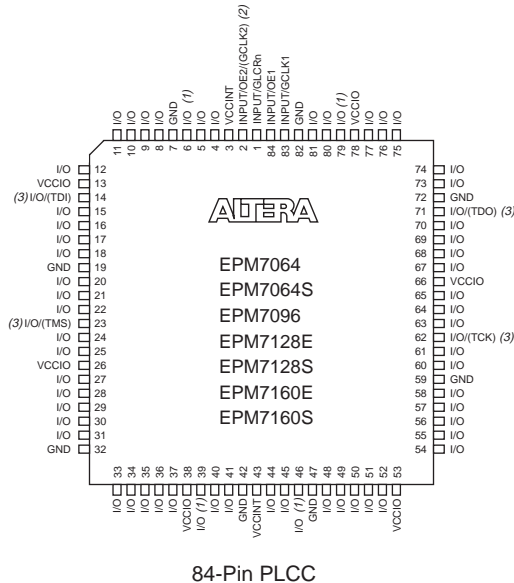


Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

Figure 19. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

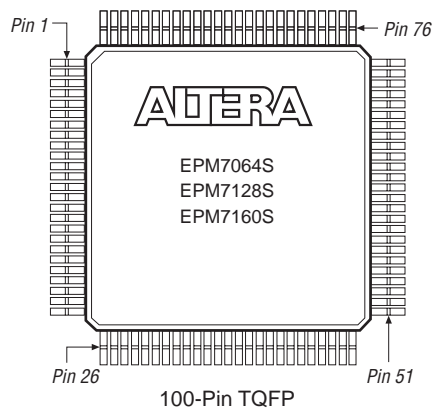
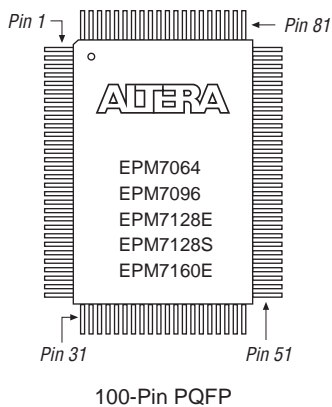
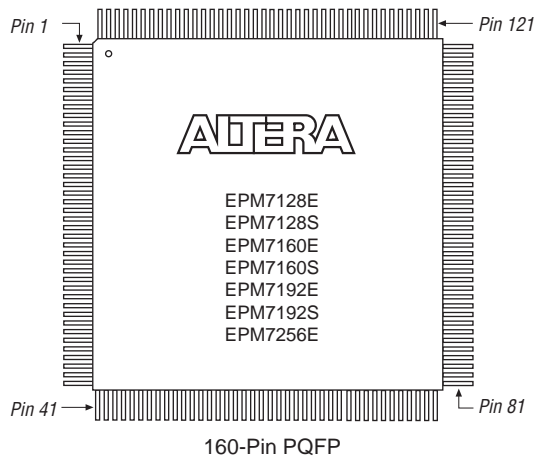
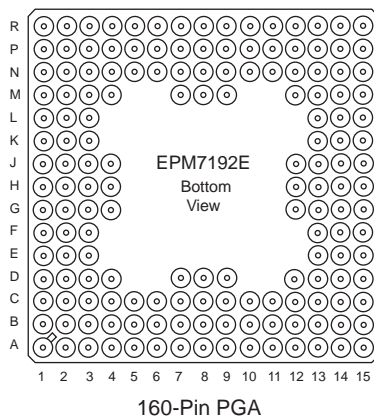


Figure 20. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.





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