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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128sqc100-10

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
 - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
 - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

Table 3. MAX 7000 Speed Grades

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

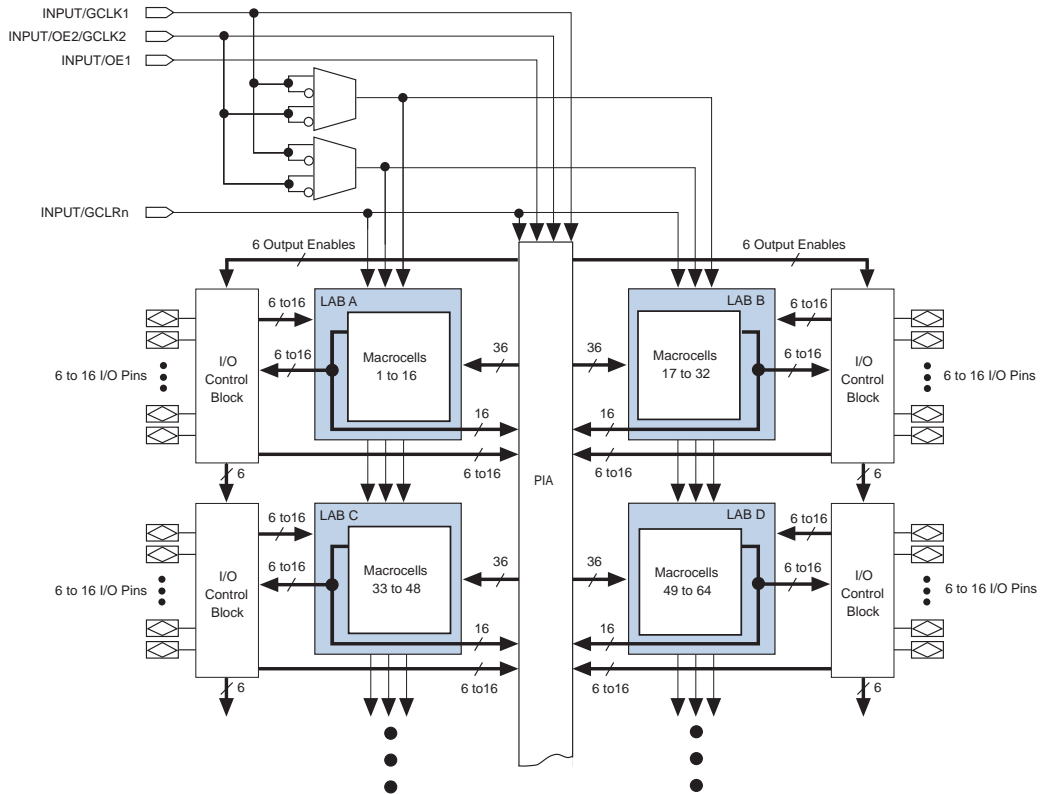
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram

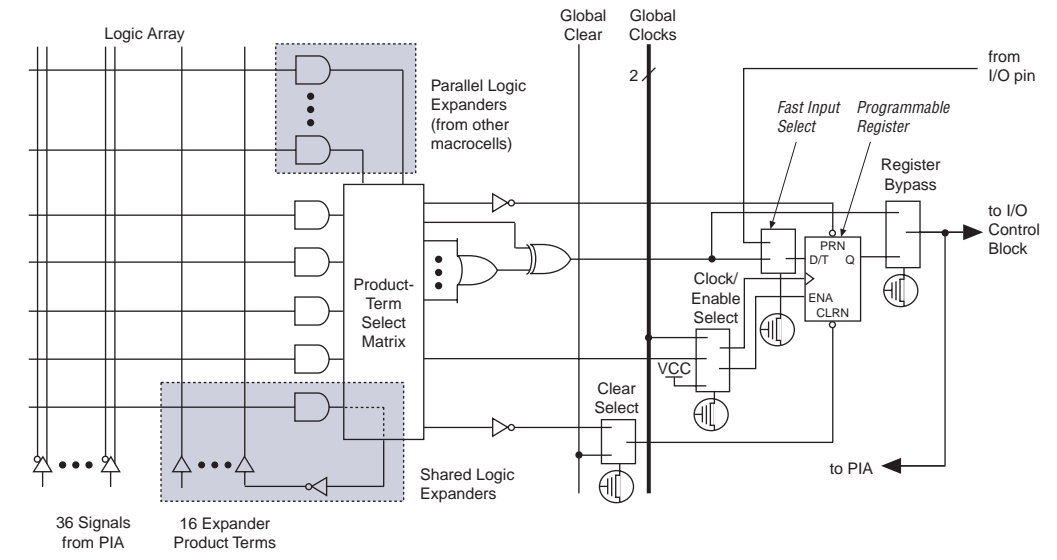


Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell

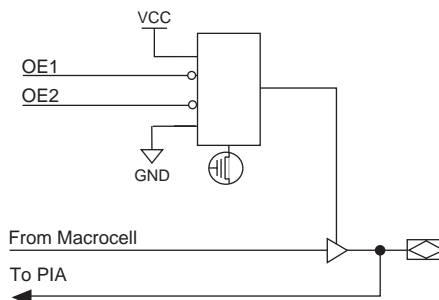
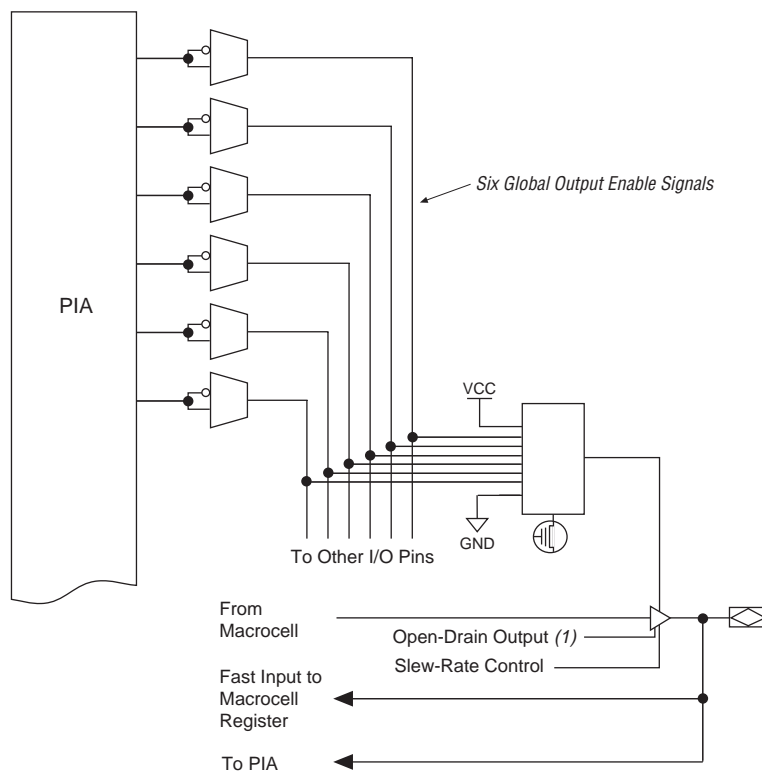


Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Figure 8. I/O Control Block of MAX 7000 Devices**EPM7032, EPM7064 & EPM7096 Devices****MAX 7000E & MAX 7000S Devices****Note:**

- (1) The open-drain output option is available only in MAX 7000S devices.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000S Device

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
 t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
 $Cycle_{PTCK}$ = Number of TCK cycles to program a device
 f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
 t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
 $Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Figure 9 shows the timing requirements for the JTAG signals.

Figure 9. MAX 7000 JTAG Waveforms

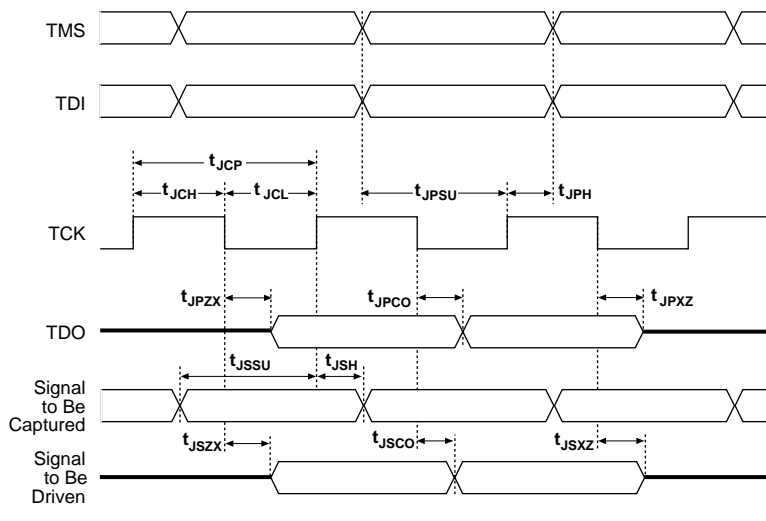


Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

Table 12. JTAG Timing Parameters & Values for MAX 7000S Devices				
Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns



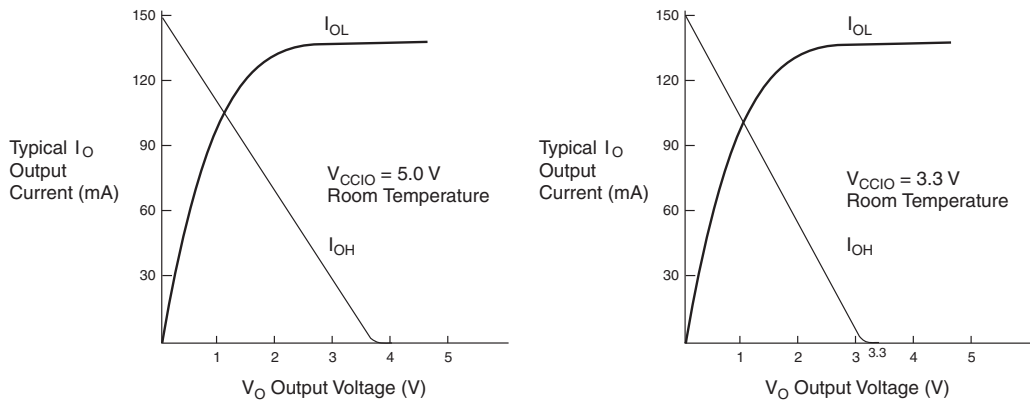
For more information, see [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#).

Notes to tables:

- (1) See the [Operating Requirements for Altera Devices Data Sheet](#).
- (2) Minimum DC input voltage on I/O pins is -0.5 V and on 4 dedicated input pins is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) V_{CC} must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed 300 μ s. The sufficient V_{CCINT} voltage level for POR is 4.5 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
- (6) 3.3 -V I/O operation is not available for 44-pin packages.
- (7) The V_{CCISP} parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is -0.3 V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically -60 μ A.
- (13) Capacitance is measured at 25° C and is sample-tested only. The $\text{OE}1$ pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 19. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	(2)		2.0		—		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	(2)		3.0		—		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		5.0		—		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$ (2)		8.0		—		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		7.0		—		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or 3.3 V	$C1 = 35\text{ pF}$ (2)		10.0		—		14.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5\text{ pF}$		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_H	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	(2)	2.0		—		4.0		ns
t_{FH}	Register hold time of fast input	(2)	2.0		—		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	(8)		13.0		15.0		15.0	ns

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t _{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t _{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t _{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t _{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t _{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t _{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_H	Register hold time		1.7		2.0		2.0		3.0		ns

Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{FSU}	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.0		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.0		1.0		2.0	ns
t_{IC}	Array clock delay			2.7		3.3		3.0		5.0	ns
t_{EN}	Register enable time			2.6		3.2		3.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.9		1.0		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		2.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		2.0		3.0	ns
t_{PIA}	PIA delay	(7)		1.1		1.3		1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		11.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} and t_{CPW} parameters for macrocells running in the low-power mode.

Tables 31 and 32 show the EPM7128S AC operating conditions.

Table 31. EPM7128S External Timing Parameters Note (1)											
Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t _{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_H	Register hold time		1.7		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		2.3		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.7		0.5		1.0		ns
t_{RD}	Register delay			1.4		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.2		2.0		1.0	ns
t_{IC}	Array clock delay			3.2		5.0		6.0	ns
t_{EN}	Register enable time			3.1		5.0		6.0	ns
t_{GLOB}	Global control delay			2.5		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	(7)		2.4		1.0		2.0	ns
t_{LPA}	Low-power adder	(8)		10.0		11.0		13.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} and t_{CPW} parameters for macrocells running in the low-power mode.

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in [Table 14](#). See [Figure 13](#) for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The I_{CCINT} value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC}$$

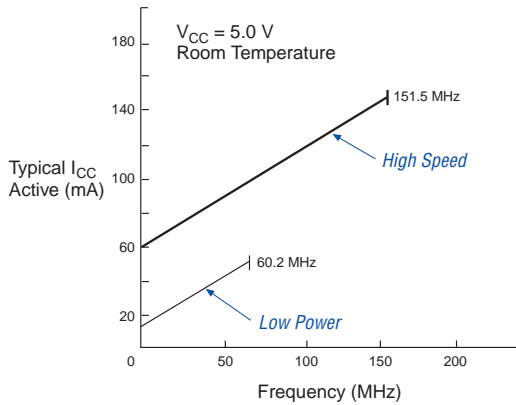
The parameters in this equation are shown below:

MC_{TON}	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
f_{MAX}	=	Highest clock frequency to the device
tog_{LC}	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in Table 39

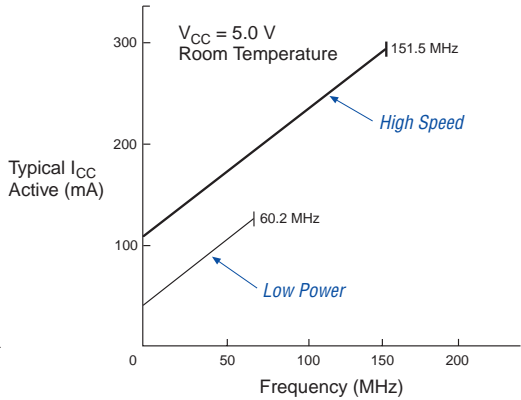
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)

EPM7032



EPM7064



EPM7096

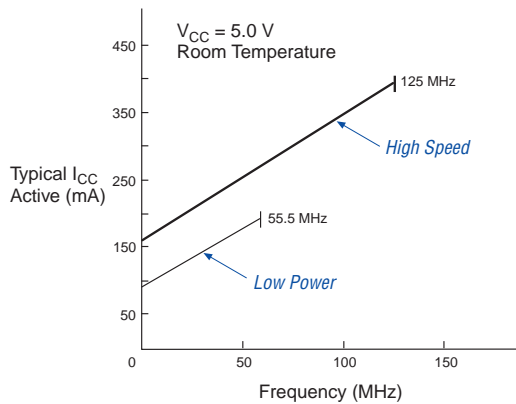
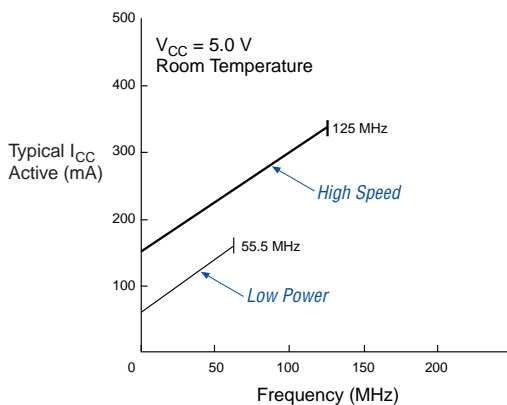
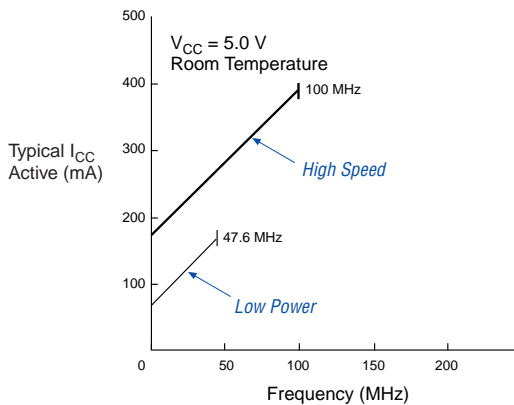


Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

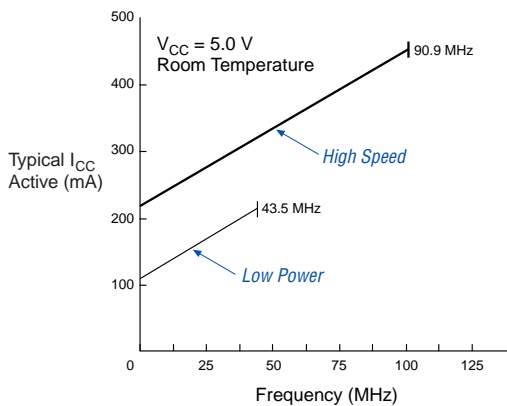
EPM7128E



EPM7160E



EPM7192E



EPM7256E

