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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7128sqc100-10n">https://www.e-xfl.com/product-detail/intel/epm7128sqc100-10n</a>

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See [Table 4](#).

<b>Table 4. MAX 7000 Device Features</b>			
<b>Feature</b>	<b>EPM7032 EPM7064 EPM7096</b>	<b>All MAX 7000E Devices</b>	<b>All MAX 7000S Devices</b>
ISP via JTAG interface			✓
JTAG BST circuitry			✓ <sup>(1)</sup>
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface <sup>(2)</sup>	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

**Notes:**

- (1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
- (2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

**Table 5. MAX 7000 Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68	68						
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

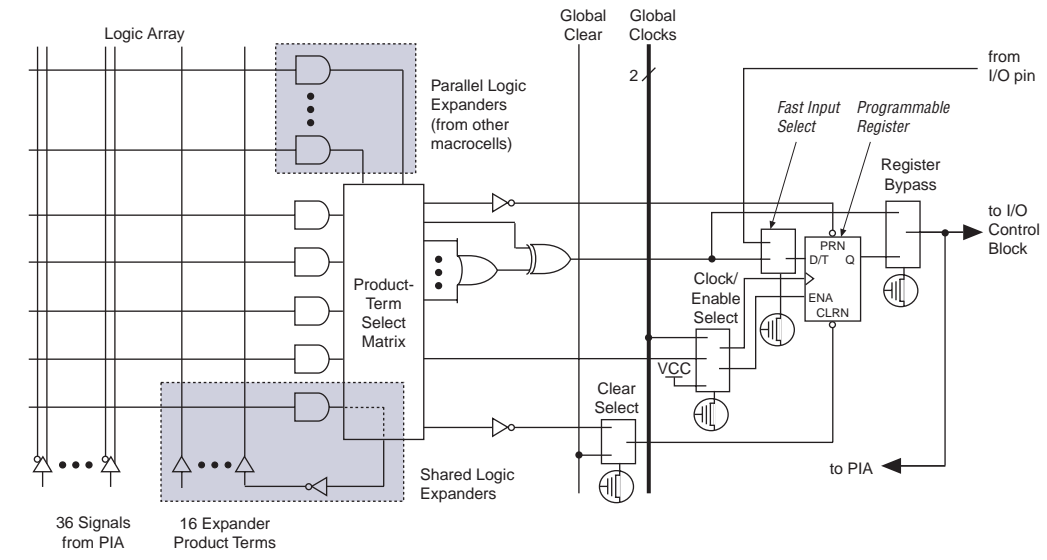
**Notes:**

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

**Figure 4. MAX 7000E & MAX 7000S Device Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

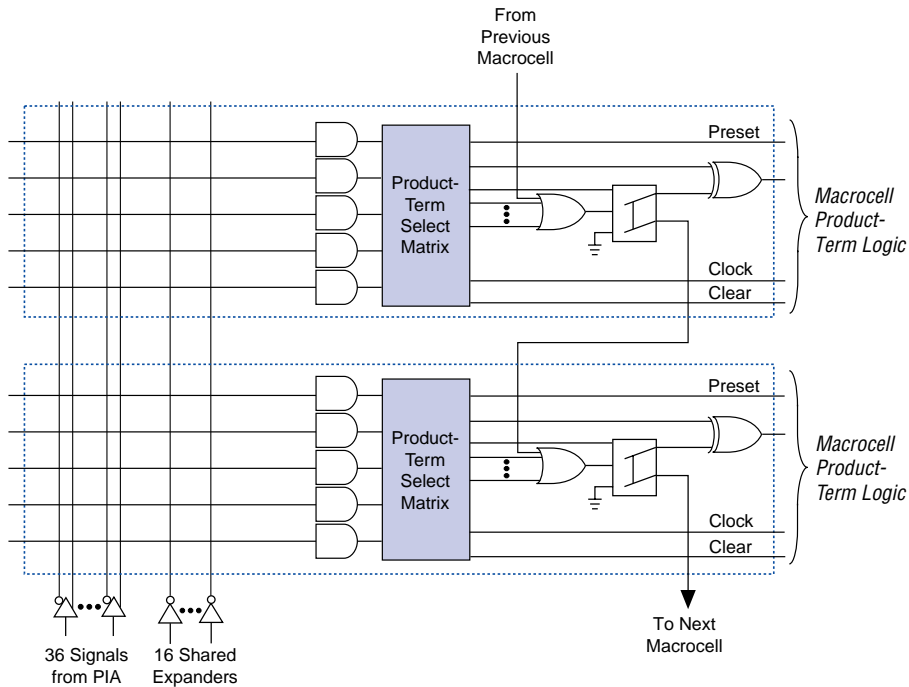
For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 6. Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*



When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to  $V_{CC}$ , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

## **In-System Programmability (ISP)**

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k $\Omega$ .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

Figure 9 shows the timing requirements for the JTAG signals.

**Figure 9. MAX 7000 JTAG Waveforms**

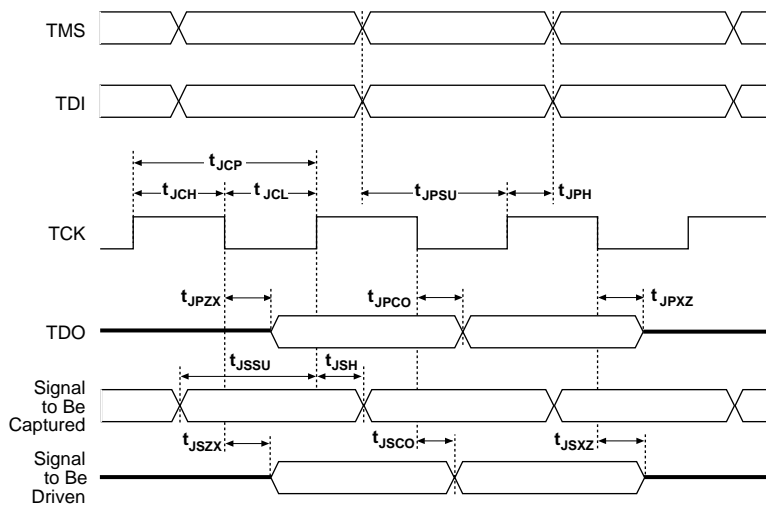
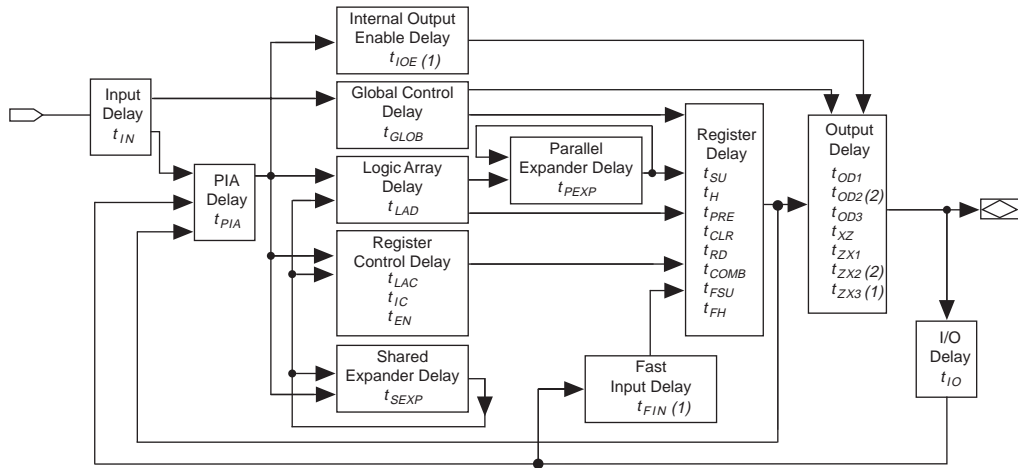


Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

<b>Table 12. JTAG Timing Parameters &amp; Values for MAX 7000S Devices</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min</b>	<b>Max</b>	<b>Unit</b>
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns



For more information, see [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#).

**Figure 12. MAX 7000 Timing Model****Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).



**Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.5		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.5		1.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			5.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.8		0.8	ns
$t_{LAD}$	Logic array delay			5.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.5		2.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		2.5	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.5		6.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		5.0		5.0	ns
$t_{SU}$	Register setup time		2.0		3.0		ns
$t_H$	Register hold time		3.0		3.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.5		0.5		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			5.0		5.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0	ns
$t_{PRE}$	Register preset time			3.0		3.0	ns
$t_{CLR}$	Register clear time			3.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		11.0	ns

**Table 23. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t <sub>SU</sub>	Global clock setup time		7.0		10.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input	(2)	3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input	(2)	0.0		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t <sub>CH</sub>	Global clock high time		4.0		4.0		ns
t <sub>CL</sub>	Global clock low time		4.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		3.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		4.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t <sub>ACH</sub>	Array clock high time		5.0		5.0		ns
t <sub>ACL</sub>	Array clock low time		5.0		5.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			11.0		11.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			11.0		11.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(6)	125.0		125.0		MHz

### Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		4.0		5.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		1.1		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.7		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.0		8.6		10.0	ns

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PIA}$	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

**Table 29. EPM7064S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		3.6		6.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		3.0		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.0		3.0		ns

**Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FSU}$	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
$t_{RD}$	Register delay			1.2		1.6		1.0		2.0	ns
$t_{COMB}$	Combinatorial delay			0.9		1.0		1.0		2.0	ns
$t_{IC}$	Array clock delay			2.7		3.3		3.0		5.0	ns
$t_{EN}$	Register enable time			2.6		3.2		3.0		5.0	ns
$t_{GLOB}$	Global control delay			1.6		1.9		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.0		2.4		2.0		3.0	ns
$t_{CLR}$	Register clear time			2.0		2.4		2.0		3.0	ns
$t_{PIA}$	PIA delay	(7)		1.1		1.3		1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		11.0		10.0		11.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$  and  $t_{CPW}$  parameters for macrocells running in the low-power mode.

**Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLR}$	Register clear time			2.4		3.0		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		1.6		2.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPWP}$  parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

**Table 35. EPM7192S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		4.1		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		1.0		2.0		4.0		ns

Tables 37 and 38 show the EPM7256S AC operating conditions.

**Table 37. EPM7256S External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.9		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.8		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.9		3.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			7.8		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			7.8		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

**Table 38. EPM7256S Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			3.4		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.9		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.1		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.6		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.6		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.8		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.1		2.0		4.0		ns
$t_H$	Register hold time		1.6		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		2.4		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.5		1.0		ns
$t_{RD}$	Register delay			1.1		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.1		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		5.0		6.0	ns
$t_{EN}$	Register enable time			2.6		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.8		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.7		3.0		4.0	ns
$t_{CLR}$	Register clear time			2.7		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		3.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		10.0		11.0		13.0	ns



**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in [Table 14](#). See [Figure 13](#) for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPTW}$  parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$  in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{CCINT}$  value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} =$$

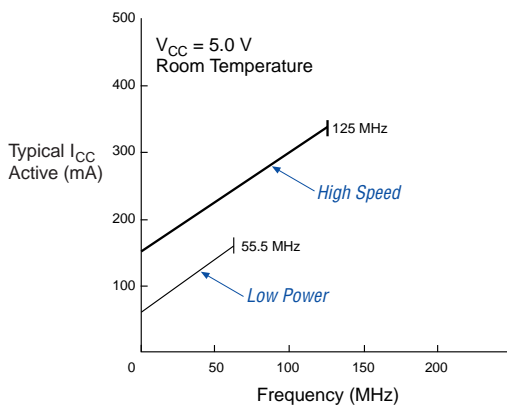
$$A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC}$$

The parameters in this equation are shown below:

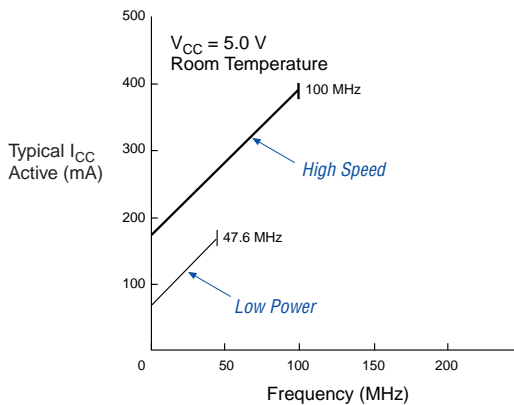
$MC_{TON}$	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
$MC_{DEV}$	=	Number of macrocells in the device
$MC_{USED}$	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
$f_{MAX}$	=	Highest clock frequency to the device
$\text{tog}_{LC}$	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in <a href="#">Table 39</a>

Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 2 of 2)

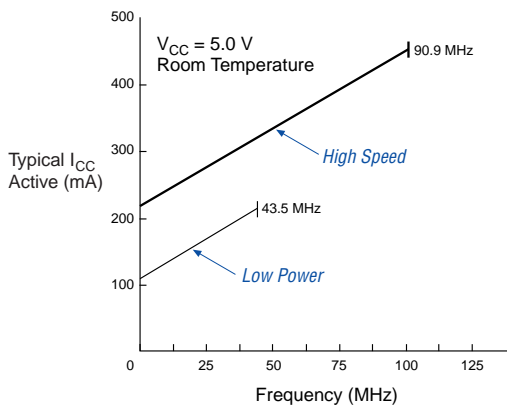
EPM7128E



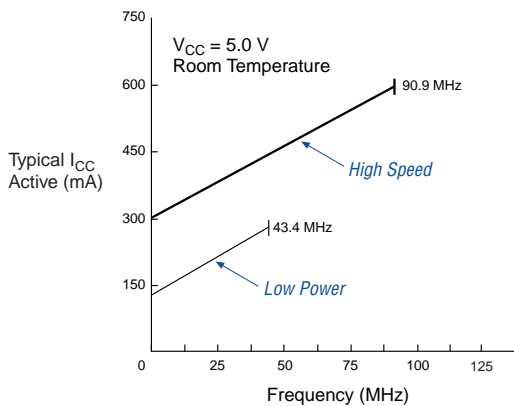
EPM7160E



EPM7192E

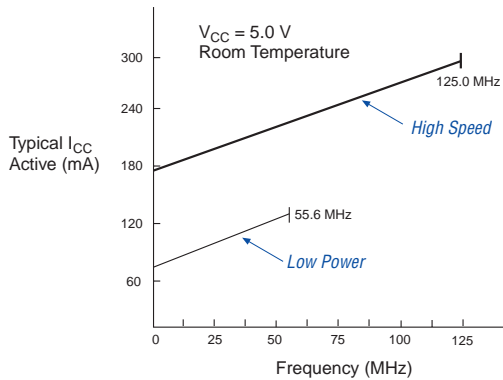


EPM7256E

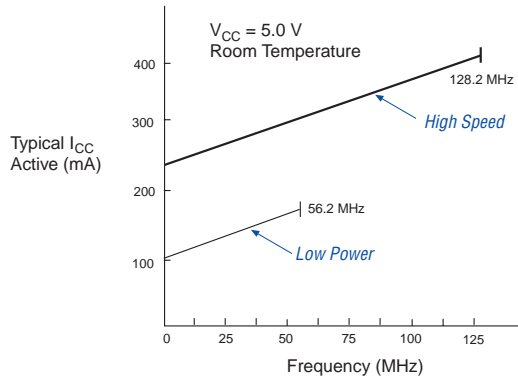


**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 2 of 2)**

EPM7192S



EPM7256S



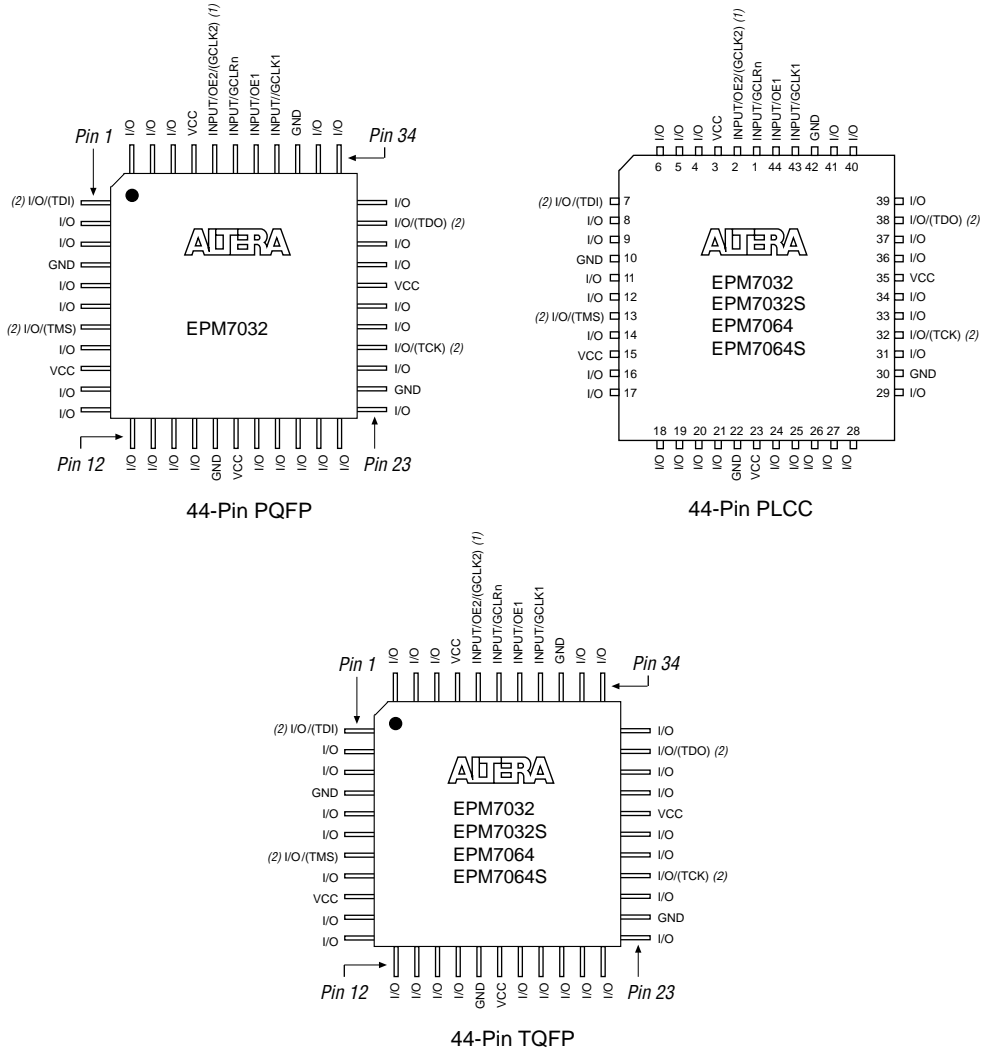
## Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

**Figure 16. 44-Pin Package Pin-Out Diagram**

Package outlines not drawn to scale.

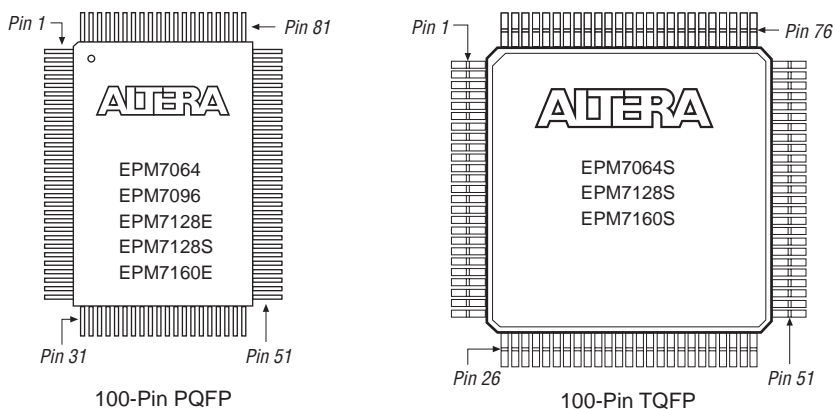


**Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

**Figure 19. 100-Pin Package Pin-Out Diagram**

*Package outline not drawn to scale.*



**Figure 20. 160-Pin Package Pin-Out Diagram**

*Package outline not drawn to scale.*

