Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

| Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	6 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128sqc160-6f

<table>
<caption>Table 2. MAX 7000S Device Features</caption>

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t_{PD} (ns)	5	5	6	6	7.5	7.5
t_{SU} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f_{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

</table>

...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

*Figure 2. MAX 7000E & MAX 7000S Device Block Diagram*
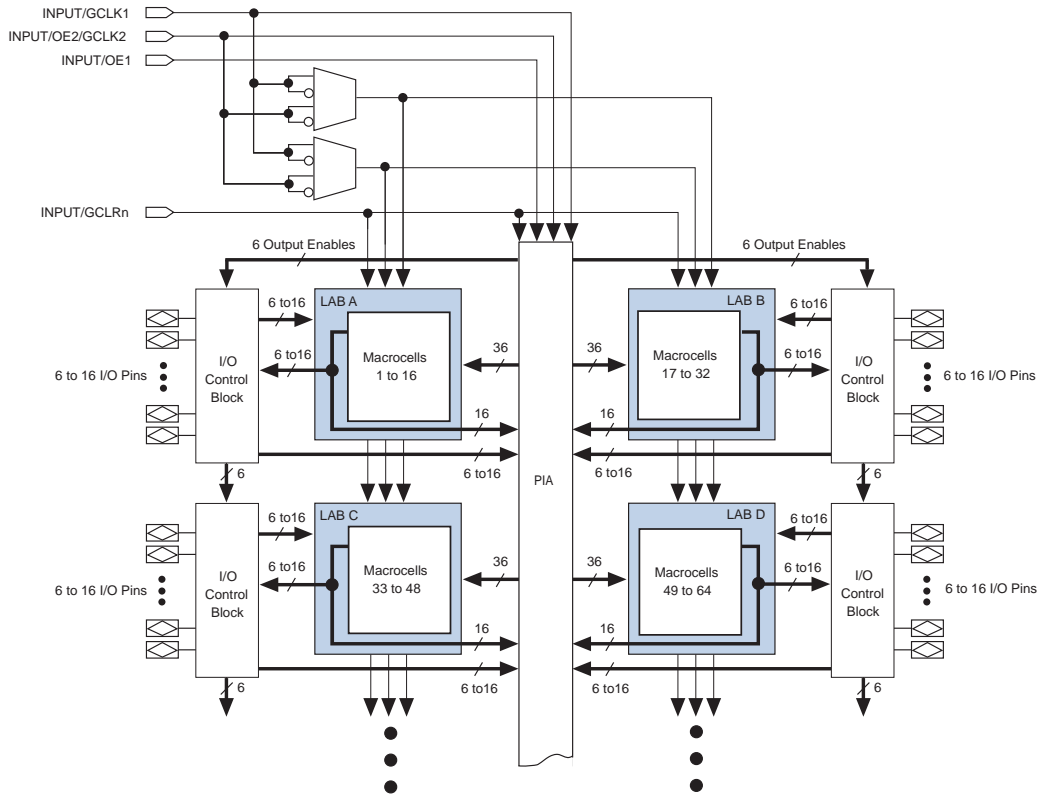
Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell
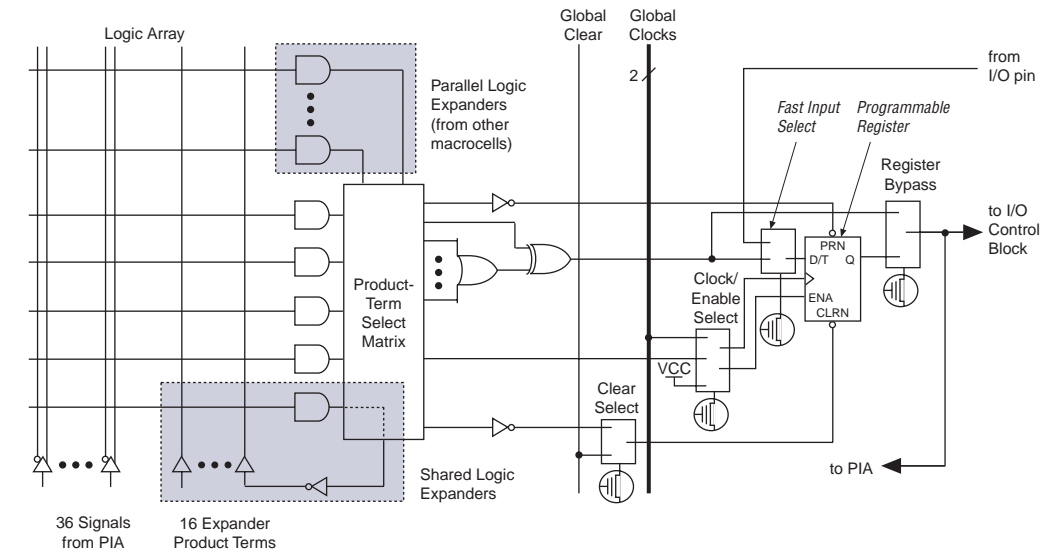
Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

■ Shareable expanders, which are inverted product terms that are fed back into the logic array
■ Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7064 & EPM7096 Devices
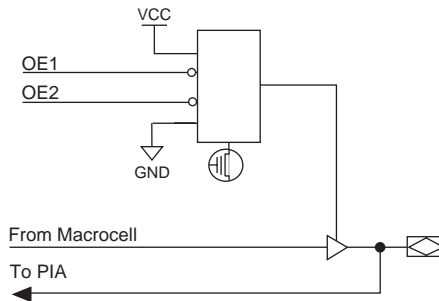
MAX 7000E & MAX 7000S Devices
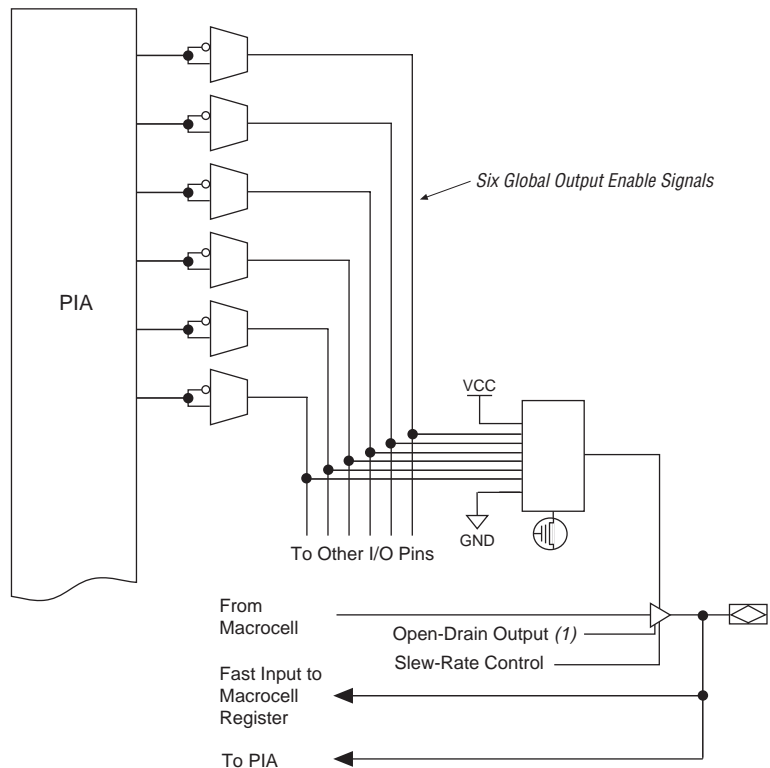
Note:
(1)   The open-drain output option is available only in MAX 7000S devices.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.

For more information, see the *Programming Hardware Manufacturers*.

Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	−2.0	7.0	V
V_I	DC input voltage		−2.0	7.0	V
I_{OUT}	DC output current, per pin		−25	25	mA
T_{STG}	Storage temperature	No bias	−65	150	° C
T_{AMB}	Ambient temperature	Under bias	−65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3)*, *(4)*, *(5)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3)*, *(4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3)*, *(4)*, *(6)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during ISP	*(7)*	4.75	5.25	V
V_I	Input voltage		−0.5 *(8)*	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	−40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	−40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage on I/O pins is –0.5 V and on 4 dedicated input pins is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) V_{CC} must rise monotonically.
(5) The POR time for all 7000S devices does not exceed 300 µs. The sufficient V_{CCINT} voltage level for POR is 4.5 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
(6) 3.3-V I/O operation is not available for 44-pin packages.
(7) The V_{CCISP} parameter applies only to MAX 7000S devices.
(8) During in-system programming, the minimum DC input voltage is –0.3 V.
(9) These values are specified under the MAX 7000 recommended operating conditions in Table 14 on page 26.
(10) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(11) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current.
(12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically –60 µA.
(13) Capacitance is measured at 25° C and is sample-tested only. The OE1 pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices
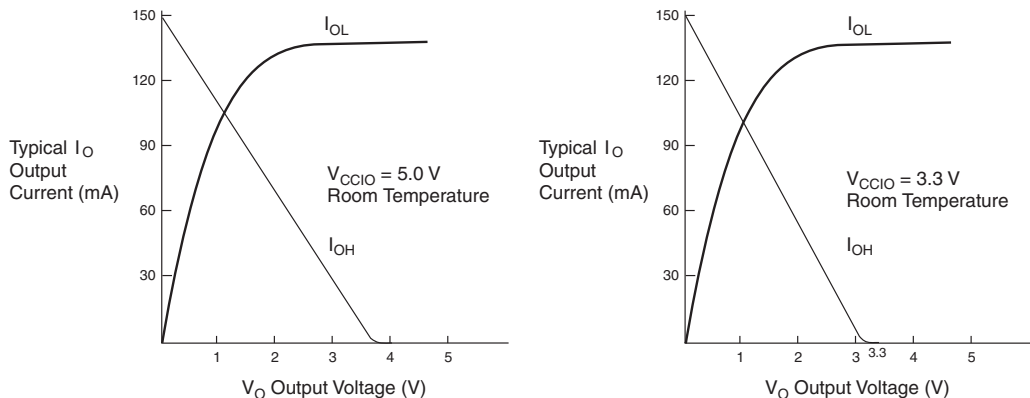
Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 12. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Figure 13. Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.
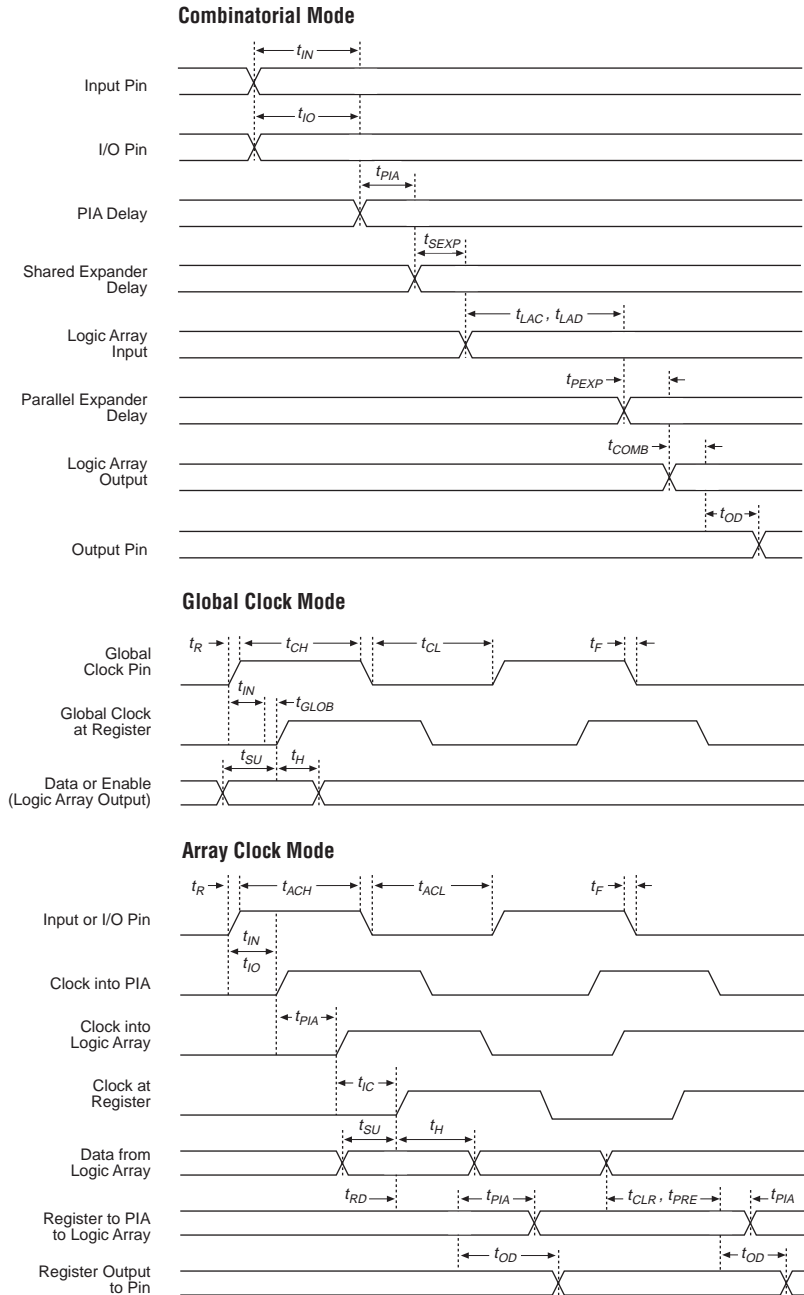
Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

Table 19. MAX 7000 & MAX 7000E External Timing Parameters   Note (1)

Table 28. EPM7032S Internal Timing Parameters   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		**-6**		**-7**		**-10**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	*(7)*		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	*(8)*		12.0		10.0		10.0		11.0	ns

Notes to tables:
(1)   These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2)   This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(3)   This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4)   These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5)   The f_{MAX} values represent the highest frequency for pipelined data.
(6)   Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial and industrial use.
(7)   For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8)   The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		**-6**		**-7**		**-10**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t_H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t_{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t_{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t_{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2)   Note (1)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		**-6**		**-7**		**-10**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{FSU}	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.0		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.0		1.0		2.0	ns
t_{IC}	Array clock delay			2.7		3.3		3.0		5.0	ns
t_{EN}	Register enable time			2.6		3.2		3.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.9		1.0		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		2.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		2.0		3.0	ns
t_{PIA}	PIA delay	(7)		1.1		1.3		1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		11.0		10.0		11.0	ns

Notes to tables:

(1)   These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2)   This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(3)   This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4)   These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5)   The f_{MAX} values represent the highest frequency for pipelined data.

(6)   Operating conditions: $V_{CCIO} = 3.3$ V $\pm$ 10% for commercial and industrial use.

(7)   For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8)   The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Table 31. EPM7128S External Timing Parameters   Note (1)

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		**-7**		**-10**		**-15**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		3.4		6.0		7.0		11.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		0.9		3.0		2.0		4.0		ns
t_{AH}	Array clock hold time		1.8		2.0		5.0		4.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		3.0		4.0		6.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f_{CNT}	Maximum internal global clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
t_{ACNT}	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f_{ACNT}	Maximum internal array clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
f_{MAX}	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		**-7**		**-10**		**-15**		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLR}	Register clear time			2.4		3.0		3.0		4.0	ns
t_{PIA}	PIA delay	*(7)*		1.6		2.0		1.0		2.0	ns
t_{LPA}	Low-power adder	*(8)*		11.0		10.0		11.0		13.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The f_{MAX} values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, **t_{ACL}**, and **t_{CPPW}** parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

Table 35. EPM7192S External Timing Parameters (Part 1 of 2)   *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		**-10**		**-15**		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t_{SU}	Global clock setup time		4.1		7.0		11.0		ns
t_H	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t_{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t_{CH}	Global clock high time		3.0		4.0		5.0		ns
t_{CL}	Global clock low time		3.0		4.0		5.0		ns
t_{ASU}	Array clock setup time		1.0		2.0		4.0		ns

Table 38. EPM7256S Internal Timing Parameters   *Note (1)*

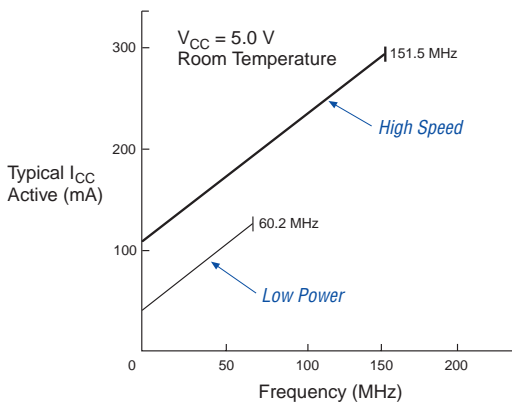| Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			3.4		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.9		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.1		0.8		1.0	ns
t_{LAD}	Logic array delay			2.6		5.0		6.0	ns
t_{LAC}	Logic control array delay			2.6		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.8		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF *(6)*		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF *(6)*		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.1		2.0		4.0		ns
t_{H}	Register hold time		1.6		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		2.4		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.5		1.0		ns
t_{RD}	Register delay			1.1		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.1		2.0		1.0	ns
t_{IC}	Array clock delay			2.9		5.0		6.0	ns
t_{EN}	Register enable time			2.6		5.0		6.0	ns
t_{GLOB}	Global control delay			2.8		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	*(7)*		3.0		1.0		2.0	ns
t_{LPA}	Low-power adder	*(8)*		10.0		11.0		13.0	ns

Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

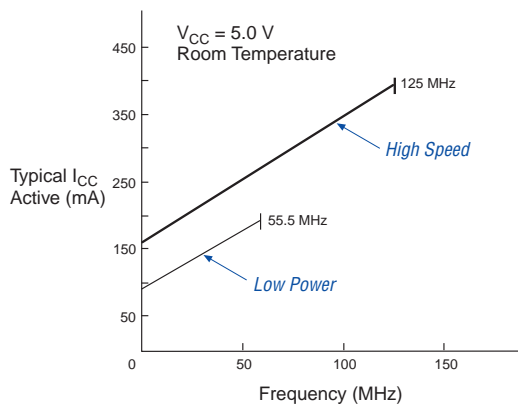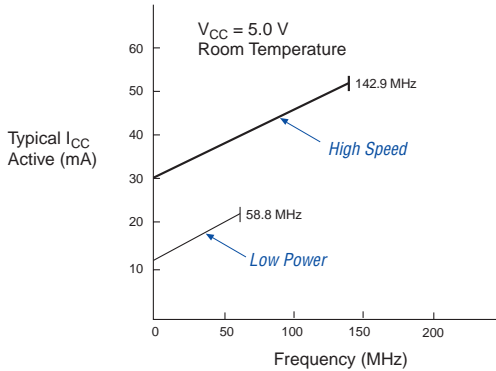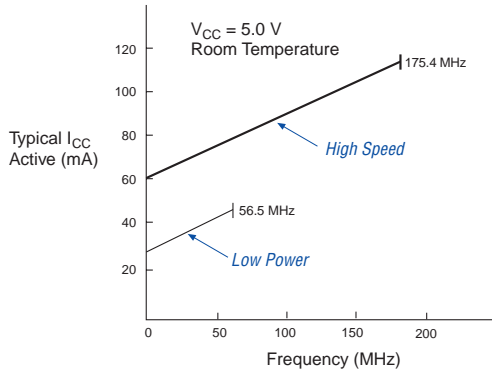*Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 1 of 2)*

Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

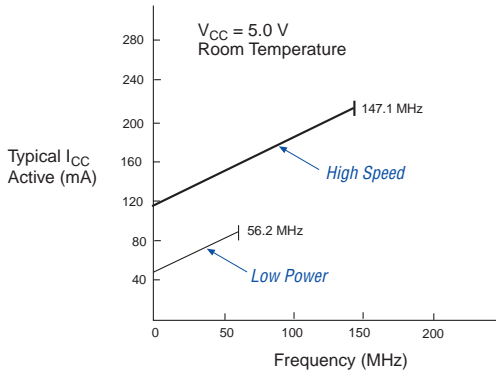*Figure 15. I$_{CC}$ vs. Frequency for MAX 7000S Devices (Part 1 of 2)*

EPM7032S

V$_{CC}$ = 5.0 V
Room Temperature

Typical I$_{CC}$ Active (mA)

60
50
40
30
20
10

142.9 MHz

High Speed

58.8 MHz

Low Power

0   50   100   150   200
Frequency (MHz)

EPM7064S

V$_{CC}$ = 5.0 V
Room Temperature

Typical I$_{CC}$ Active (mA)

120
100
80
60
40
20

175.4 MHz

High Speed

56.5 MHz

Low Power

0   50   100   150   200
Frequency (MHz)

EPM7128S

V$_{CC}$ = 5.0 V
Room Temperature

Typical I$_{CC}$ Active (mA)

280
240
200
160
120
80
40

147.1 MHz

High Speed

56.2 MHz

Low Power

0   50   100   150   200
Frequency (MHz)

EPM7160S

V$_{CC}$ = 5.0 V
Room Temperature

Typical I$_{CC}$ Active (mA)

300
240
180
120
60

149.3 MHz

High Speed

56.5 MHz

Low Power

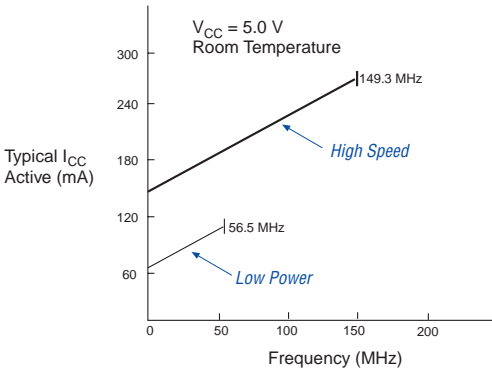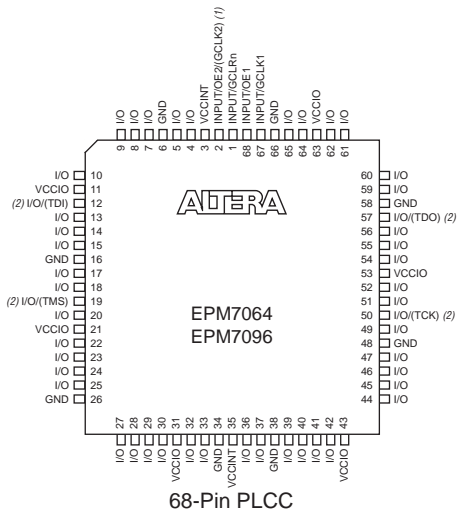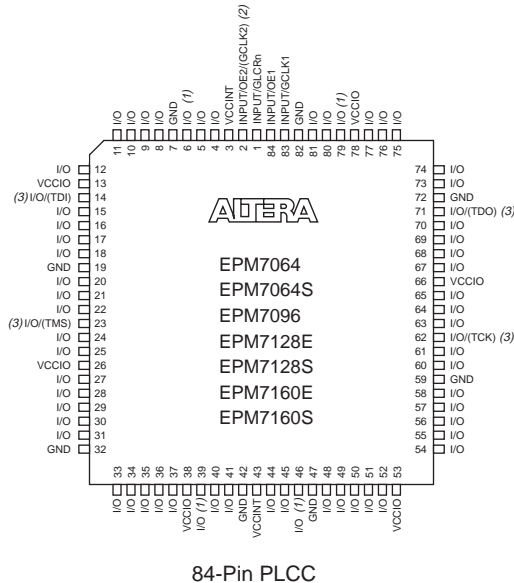0   50   100   150   200
Frequency (MHz)

Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.

68-Pin PLCC

Notes:
(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(2) JTAG ports are available in MAX 7000S devices only.

Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

Top pins (left to right): I/O (11), I/O (10), I/O (9), I/O (8), GND (7), I/O (6) (1), I/O (5), I/O (4), VCCINT (3), INPUT/OE2/(GCLK2) (2), INPUT/GLCRn (1), INPUT/OE1 (84), INPUT/GCLK1 (83), GND (82), I/O (81), I/O (80), I/O (79) (1), VCCIO (78), I/O (77), I/O (76), I/O (75)

Left pins (top to bottom):
I/O — 12
VCCIO — 13
(3) I/O/(TDI) — 14
I/O — 15
I/O — 16
I/O — 17
I/O — 18
GND — 19
I/O — 20
I/O — 21
I/O — 22
(3) I/O/(TMS) — 23
I/O — 24
I/O — 25
VCCIO — 26
I/O — 27
I/O — 28
I/O — 29
I/O — 30
I/O — 31
GND — 32

Right pins (top to bottom):
74 — I/O
73 — I/O
72 — GND
71 — I/O/(TDO) (3)
70 — I/O
69 — I/O
68 — I/O
67 — I/O
66 — VCCIO
65 — I/O
64 — I/O
63 — I/O
62 — I/O/(TCK) (3)
61 — I/O
60 — I/O
59 — GND
58 — I/O
57 — I/O
56 — I/O
55 — I/O
54 — I/O

Center device labels:
ALTERA

EPM7064
EPM7064S
EPM7096
EPM7128E
EPM7128S
EPM7160E
EPM7160S

Bottom pins (left to right): I/O (33), I/O (34), I/O (35), I/O (36), I/O (37), VCCIO (38), I/O (39) (1), I/O (40), I/O (41), GND (42), VCCINT (43), I/O (44), I/O (45), I/O (46) (1), I/O (47), GND (48), I/O (49), I/O (50), I/O (51), I/O (52), VCCIO (53)
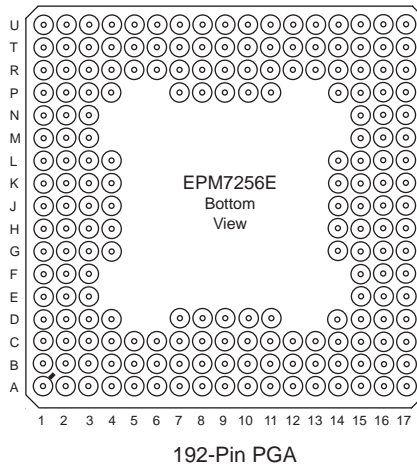
84-Pin PLCC

Notes:
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
(2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
(3) JTAG ports are available in MAX 7000S devices only.

Figure 21. 192-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

192-Pin PGA

Figure 22. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

208-Pin PQFP/RQFP
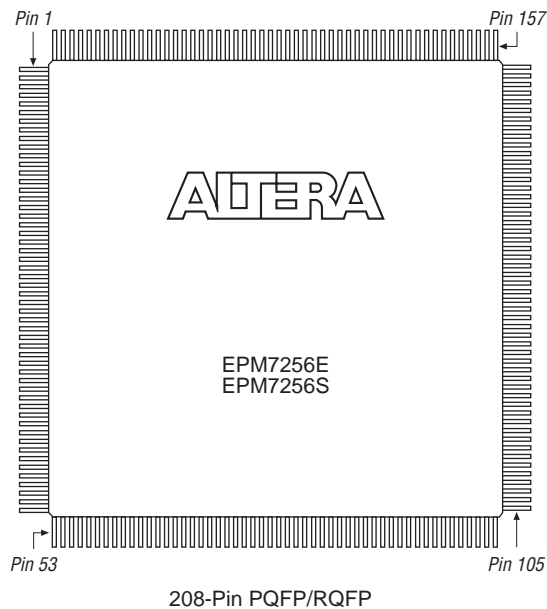
Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

■ Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

■ Added Tables 6 through 8.
■ Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

■ Updated text on page 16.

Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

■ Added *Note (5)* on page 28.

Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

■ Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.