



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	100
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128sqi160-10

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

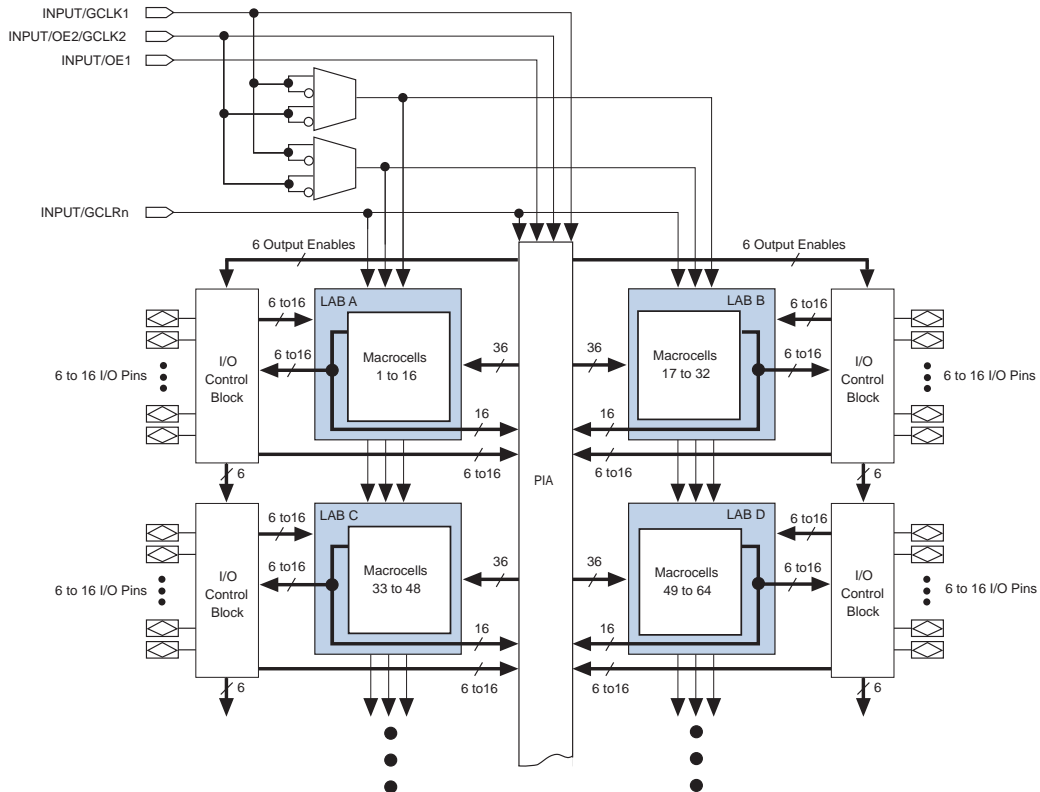
Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

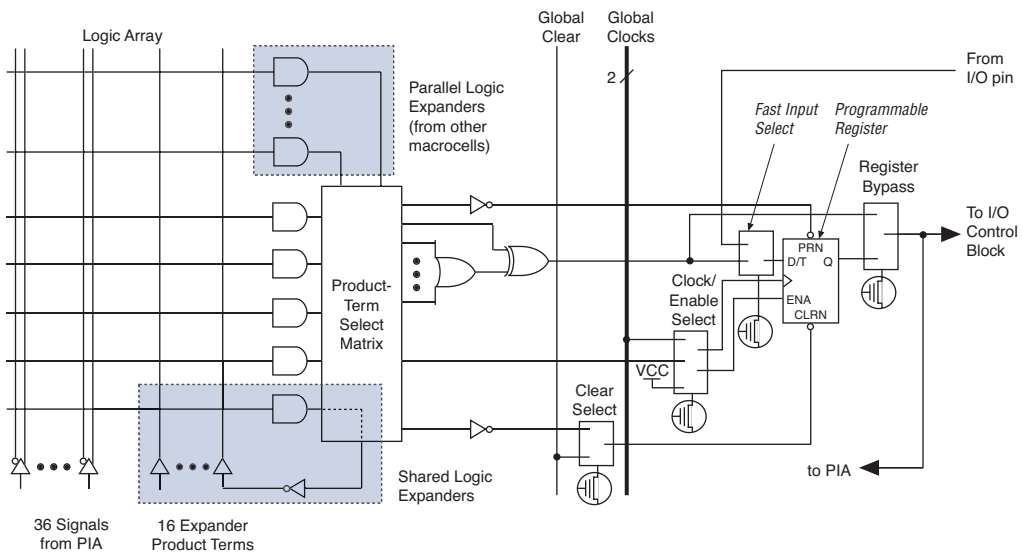
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for MAX 7000E and MAX 7000S devices

Macrocells

The MAX 7000 macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell



Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

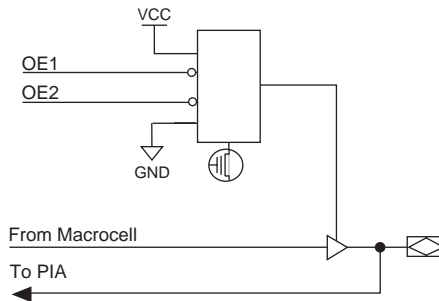
All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

Expander Product Terms

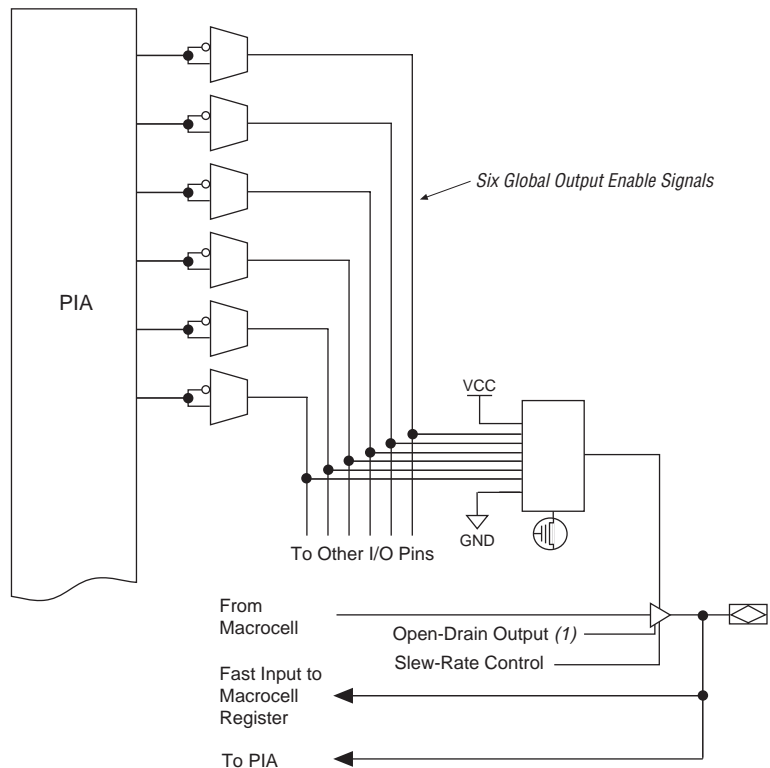
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Figure 8. I/O Control Block of MAX 7000 Devices

EPM7032, EPM7064 & EPM7096 Devices



MAX 7000E & MAX 7000S Devices



Note:

- (1) The open-drain output option is available only in MAX 7000S devices.



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The programming times described in [Tables 6 through 8](#) are associated with the worst-case method using the enhanced ISP algorithm.

Table 6. MAX 7000S t_{PULSE} & $Cycle_{TCK}$ Values

Device	Programming		Stand-Alone Verification	
	t_{PULSE} (s)	$Cycle_{PTCK}$	t_{VPULSE} (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

[Tables 7](#) and [8](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies

Device	f_{TCK}								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the *Altera Programming Hardware Data Sheet*.

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the *Programming Hardware Manufacturers*.

Design Security

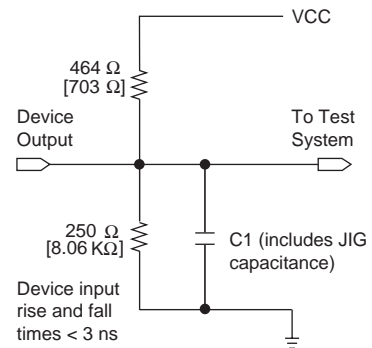
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 10](#). Test patterns can be used and then erased during early stages of the production flow.

Figure 10. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.



QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.



For detailed information and carrier dimensions, refer to the [QFP Carrier & Development Socket Data Sheet](#).



MAX 7000S devices are not shipped in carriers.

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5 (8)	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V (10)	$V_{CCIO} - 0.2$		V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (11)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V (11)		0.2	V
I_I	Leakage current of dedicated input pins	$V_I = -0.5$ to 5.5 V (11)	-10	10	μ A
I_{OZ}	I/O pin tri-state output off-state current	$V_I = -0.5$ to 5.5 V (11), (12)	-40	40	μ A

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 19. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

Table 20. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade -6		Speed Grade -7		Unit
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.5	ns
t_{FIN}	Fast input delay	(2)		0.8		1.0	ns
t_{SEXP}	Shared expander delay			3.5		4.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			2.0		3.0	ns
t_{LAC}	Logic control array delay			2.0		3.0	ns
t_{OE}	Internal output enable delay	(2)				2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		2.0		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		7.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		4.0		4.0	ns
t_{SU}	Register setup time		3.0		3.0		ns
t_H	Register hold time		1.5		2.0		ns
t_{FSU}	Register setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Register hold time of fast input	(2)	0.5		0.5		ns
t_{RD}	Register delay			0.8		1.0	ns
t_{COMB}	Combinatorial delay			0.8		1.0	ns
t_{JC}	Array clock delay			2.5		3.0	ns
t_{EN}	Register enable time			2.0		3.0	ns
t_{GLOB}	Global control delay			0.8		1.0	ns
t_{PRE}	Register preset time			2.0		2.0	ns
t_{CLR}	Register clear time			2.0		2.0	ns
t_{PIA}	PIA delay			0.8		1.0	ns
t_{LPA}	Low-power adder	(8)		10.0		10.0	ns

Table 21. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{SU}	Global clock setup time		7.0		8.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		2.0		3.0		ns
t _{AH}	Array clock hold time		3.0		3.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t _{ACH}	Array clock high time		4.0		4.0		ns
t _{ACL}	Array clock low time		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			10.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t _{ACNT}	Minimum array clock period			10.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t_{FIN}	Fast input delay	(2)		1.0		1.0	ns
t_{SEXP}	Shared expander delay			7.0		7.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0	ns
t_{LAD}	Logic array delay			7.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	(2)		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
t_{SU}	Register setup time		1.0		4.0		ns
t_H	Register hold time		6.0		4.0		ns
t_{FSU}	Register setup time of fast input	(2)	4.0		2.0		ns
t_{FH}	Register hold time of fast input	(2)	0.0		2.0		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			7.0		5.0	ns
t_{GLOB}	Global control delay			2.0		0.0	ns
t_{PRE}	Register preset time			4.0		3.0	ns
t_{CLR}	Register clear time			4.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		12.0	ns

Table 27. EPM7032S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.3		0.5	ns
t_{FIN}	Fast input delay			2.2		2.1		2.5		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.6		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		1.4		0.8	ns
t_{LAD}	Logic array delay			2.6		3.3		4.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.3		4.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		1.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		0.4		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		0.9		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		5.4		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		1.3		2.0		ns
t_H	Register hold time		1.7		2.0		2.5		3.0		ns
t_{FSU}	Register setup time of fast input		1.9		1.8		1.7		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.8		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.9		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.1		1.4		2.0	ns
t_{IC}	Array clock delay			2.7		3.4		4.2		5.0	ns
t_{EN}	Register enable time			2.6		3.3		4.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.4		1.7		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		3.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		3.0		3.0	ns

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t _{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t _{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t _{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

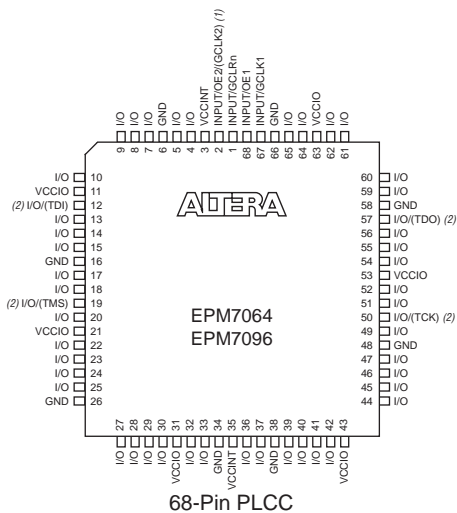
Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t _{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t _{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t _{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_H	Register hold time		1.7		2.0		2.0		3.0		ns

Table 32. EPM7128S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		1.0		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.7		4.0		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.1		0.8		0.8		1.0	ns
t_{LAD}	Logic array delay			3.0		3.0		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.0		3.0		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		2.0		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		2.0		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.9		2.5		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		7.0		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		3.0		2.0		4.0		ns
t_H	Register hold time		1.7		2.0		5.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		3.0		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.5		0.5		1.0		ns
t_{RD}	Register delay			1.4		1.0		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		2.0		1.0	ns
t_{IC}	Array clock delay			3.1		3.0		5.0		6.0	ns
t_{EN}	Register enable time			3.0		3.0		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		1.0		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		2.0		3.0		4.0	ns
t_{CLR}	Register clear time			2.4		2.0		3.0		4.0	ns
t_{PIA}	PIA delay	(7)		1.4		1.0		1.0		2.0	ns
t_{LPA}	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

Figure 17. 68-Pin Package Pin-Out Diagram*Package outlines not drawn to scale.***Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.



Notes: