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Intel - EPM7128STC100-15N Datasheet



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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	8
Number of Macrocells	128
Number of Gates	2500
Number of I/O	84
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7128stc100-15n

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Table 2. MAX	7000S Device I	Features				
Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t _{PD} (ns)	5	5	6	6	7.5	7.5
t _{su} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t _{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f _{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
 - MultiVoltTM I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
 - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
 - Six pin- or logic-driven output enable signals
 - Two global clock signals with optional inversion
 - Enhanced interconnect resources for improved routability
 - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
 - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

	 Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest Programming support Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices The BitBlasterTM serial download cable, ByteBlasterMVTM parallel port download cable, and MasterBlasterTM serial/universal serial bus (USB) download cable program MAX 7000S devices
General Description	The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) <i>PCI Local Bus Specification, Revision 2.2.</i> See Table 3 for available speed grades.

Table 3. MA	Table 3. MAX 7000 Speed Grades											
Device					Speed	Grade						
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20		
EPM7032		~	~		\checkmark		~	>	 			
EPM7032S	~	~	~		~							
EPM7064		~	~		~		~	\checkmark				
EPM7064S	\checkmark	~	~		~							
EPM7096			~		\checkmark		~	\checkmark				
EPM7128E			~	 	~		~	\checkmark		~		
EPM7128S		~	~		~			\checkmark				
EPM7160E				 Image: A start of the start of	~		~	~		~		
EPM7160S		 Image: A start of the start of	~		~			~				
EPM7192E						 Image: A start of the start of	~	~		~		
EPM7192S			~		~			~				
EPM7256E						~	\checkmark	\checkmark		\checkmark		
EPM7256S			\checkmark		\checkmark			\checkmark				

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

Table 5. M.	Table 5. MAX 7000 Maximum User I/O Pins Note (1)											
Device	44- Pin PLCC	44- Pin PQFP	44- Pin TQFP	68- Pin PLCC	84- Pin PLCC	100- Pin PQFP	100- Pin TQFP	160- Pin PQFP	160- Pin PGA	192- Pin PGA	208- Pin PQFP	208- Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

Notes:

 When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and highspeed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)— and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.

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For more information on development tools, see the MAX+PLUS II Programmable Logic Development System & Software Data Sheet and the Quartus Programmable Logic Development System & Software Data Sheet.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders



Shareable expanders can be shared by any or all macrocells in an LAB.

Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lowernumbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders



Unused product terms in a macrocell can be allocated to a neighboring macrocell.

Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC} . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

MAX 7000 Programmable Logic Device Family Data Sheet

Notes to tables:

- (1) See the Operating Requirements for Altera Devices Data Sheet.
- (2) Minimum DC input voltage on I/O pins is -0.5 V and on 4 dedicated input pins is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) V_{CC} must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed 300 μs. The sufficient V_{CCINT} voltage level for POR is 4.5 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
- (6) 3.3-V I/O operation is not available for 44-pin packages.
- (7) The V_{CCISP} parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is -0.3 V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in Table 14 on page 26.
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically -60 μA.
- (13) Capacitance is measured at 25° C and is sample-tested only. The OE1 pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 12. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Symbol	Parameter	Conditions		Speed	Grade		Unit
			MAX 700	OE (-10P)	MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{SU}	Global clock setup time		7.0		8.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		2.0		3.0		ns
t _{AH}	Array clock hold time		3.0		3.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t _{ACH}	Array clock high time		4.0		4.0		ns
t _{ACL}	Array clock low time		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			10.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
tACNT	Minimum array clock period			10.0		10.0	ns
f _{acnt}	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Symbol	Parameter	Conditions		Speed Min Max 1.0 1.0 1.0 1.0 1.0 1.0 7.0 1.0 7.0 1.0 7.0 5.0 2.0 1.0 5.0 2.0 1.0 1.0 7.0 1.0 6.0 1.0 6.0 10.0 6.0 10.0 6.0 2.0 1.0 6.0 1.0 2.0	Grade		Unit
			MAX 700	IOE (-12P)	MAX 70 Max 70	100 (-12) Doe (-12)	
			Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			1.0		2.0	ns
t _{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t _{FIN}	Fast input delay	(2)		1.0		1.0	ns
t _{SEXP}	Shared expander delay			7.0		7.0	ns
t _{PEXP}	Parallel expander delay			1.0		1.0	ns
t _{LAD}	Logic array delay			7.0		5.0	ns
t _{LAC}	Logic control array delay			5.0		5.0	ns
t _{IOE}	Internal output enable delay	(2)		2.0		2.0	ns
t _{OD1}	Output buffer and pad delay Slow slew rate = off V _{CCIO} = 5.0 V	C1 = 35 pF		1.0		3.0	ns
t _{OD2}	Output buffer and pad delay Slow slew rate = off V _{CCIO} = 3.3 V	C1 = 35 pF (7)		2.0		4.0	ns
t _{OD3}	Output buffer and pad delay Slow slew rate = on V _{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF (2)		5.0		7.0	ns
t _{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0 V$	C1 = 35 pF		6.0		6.0	ns
t _{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3 V$	C1 = 35 pF (7)		7.0		7.0	ns
t _{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0 V \text{ or } 3.3 V$	C1 = 35 pF (2)		10.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0	ns
t _{SU}	Register setup time		1.0		4.0		ns
t _H	Register hold time		6.0		4.0		ns
t _{FSU}	Register setup time of fast input	(2)	4.0		2.0		ns
t _{FH}	Register hold time of fast input	(2)	0.0		2.0		ns
t _{RD}	Register delay			2.0		1.0	ns
t _{COMB}	Combinatorial delay			2.0		1.0	ns
t _{IC}	Array clock delay			5.0		5.0	ns
t _{EN}	Register enable time			7.0		5.0	ns
t _{GLOB}	Global control delay			2.0		0.0	ns
t _{PRE}	Register preset time			4.0		3.0	ns
t _{CLR}	Register clear time			4.0		3.0	ns
t _{PIA}	PIA delay			1.0		1.0	ns
t _{LPA}	Low-power adder	(8)		12.0		12.0	ns

Table 28. EPM7032S Internal Timing Parameters Note (1)											
Symbol	Parameter	Conditions		Speed Grade							
			-5 -6			-7		-10			
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PIA}	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
t _{LPA}	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) Note (1)											
Symbol	Parameter	Conditions	Speed Grade								
			-	5	-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t _{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t _{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t _{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3 \text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 33 and 34 show the EPM7160S AC operating conditions.

Table 33. EPM7160S External Timing Parameters (Part 1 of 2) Note (1)											
Symbol	Parameter	Conditions				Speed	Grade)			Unit
			-	6	-	7	-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.4		4.2		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		3.9		4.8		5		8	ns
t _{CH}	Global clock high time		3.0		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.9		1.1		2.0		4.0		ns
t _{AH}	Array clock hold time		1.7		2.1		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		6.4		7.9		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			6.7		8.2		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	149.3		122.0		100.0		76.9		MHz

Altera Corporation

Table 3	Table 35. EPM7192S External Timing Parameters (Part 2 of 2) Note (1)											
Symbol	Parameter	Conditions			Speed	Grade			Unit			
			-	-7		-10		-15				
			Min	Max	Min	Max	Min	Max				
t _{AH}	Array clock hold time		1.8		3.0		4.0		ns			
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns			
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns			
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns			
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns			
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns			
t _{CNT}	Minimum global clock period			8.0		10.0		13.0	ns			
f _{CNT}	Maximum internal global clock frequency	(4)	125.0		100.0		76.9		MHz			
t _{ACNT}	Minimum array clock period			8.0		10.0		13.0	ns			
f _{ACNT}	Maximum internal array clock frequency	(4)	125.0		100.0		76.9		MHz			
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz			

Symbol	Parameter	Conditions			Speed	Grade			Unit
			-	7		10	-15]
			Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t _{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t _{FIN}	Fast input delay			3.2		1.0		2.0	ns
t _{SEXP}	Shared expander delay			4.2		5.0		8.0	ns
t _{PEXP}	Parallel expander delay			1.2		0.8		1.0	ns
t _{LAD}	Logic array delay			3.1		5.0		6.0	ns
t _{LAC}	Logic control array delay			3.1		5.0		6.0	ns
t _{IOE}	Internal output enable delay			0.9		2.0		3.0	ns
t _{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t _{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		1.0		2.0		5.0	ns
t _{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		7.0	ns
t _{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t _{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		5.5		7.0	ns
t _{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t _{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t _{SU}	Register setup time		1.1		2.0		4.0		ns

Table 39. MAX 7000 I _{CC} Equation Constants			
Device	Α	В	C
EPM7032	1.87	0.52	0.144
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S	0.93	0.40	0.040
EPM7064S	0.93	0.40	0.040
EPM7128S	0.93	0.40	0.040
EPM7160S	0.93	0.40	0.040
EPM7192S	0.93	0.40	0.040
EPM7256S	0.93	0.40	0.040

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

- The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

Figure 18. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



84-Pin PLCC

Notes:

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

Figure 19. 100-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 20. 160-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 21. 192-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Figure 22. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.7:

Reference to AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor has been replaced by AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor.

Version 6.6

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

Version 6.5

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.5:

Updated text on page 16.

Version 6.4

The following changes were made in the *MAX* 7000 Programmable Logic Device Family Data Sheet version 6.4:

Added Note (5) on page 28.

Version 6.3

The following changes were made in the *MAX* 7000 *Programmable Logic Device Family Data Sheet* version 6.3:

 Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.