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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	10
Number of Macrocells	160
Number of Gates	3200
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7160slc84-10n">https://www.e-xfl.com/product-detail/intel/epm7160slc84-10n</a>

**Table 2. MAX 7000S Device Features**

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
$t_{PD}$ (ns)	5	5	6	6	7.5	7.5
$t_{SU}$ (ns)	2.9	2.9	3.4	3.4	4.1	3.9
$t_{FSU}$ (ns)	2.5	2.5	2.5	2.5	3	3
$t_{CO1}$ (ns)	3.2	3.2	4	3.9	4.7	4.7
$f_{CNT}$ (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

## ...and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

**Table 3. MAX 7000 Speed Grades**

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See [Table 4](#).

<b>Table 4. MAX 7000 Device Features</b>			
<b>Feature</b>	<b>EPM7032 EPM7064 EPM7096</b>	<b>All MAX 7000E Devices</b>	<b>All MAX 7000S Devices</b>
ISP via JTAG interface			✓
JTAG BST circuitry			✓ <sup>(1)</sup>
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface <sup>(2)</sup>	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

**Notes:**

- (1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
- (2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

**Table 5. MAX 7000 Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

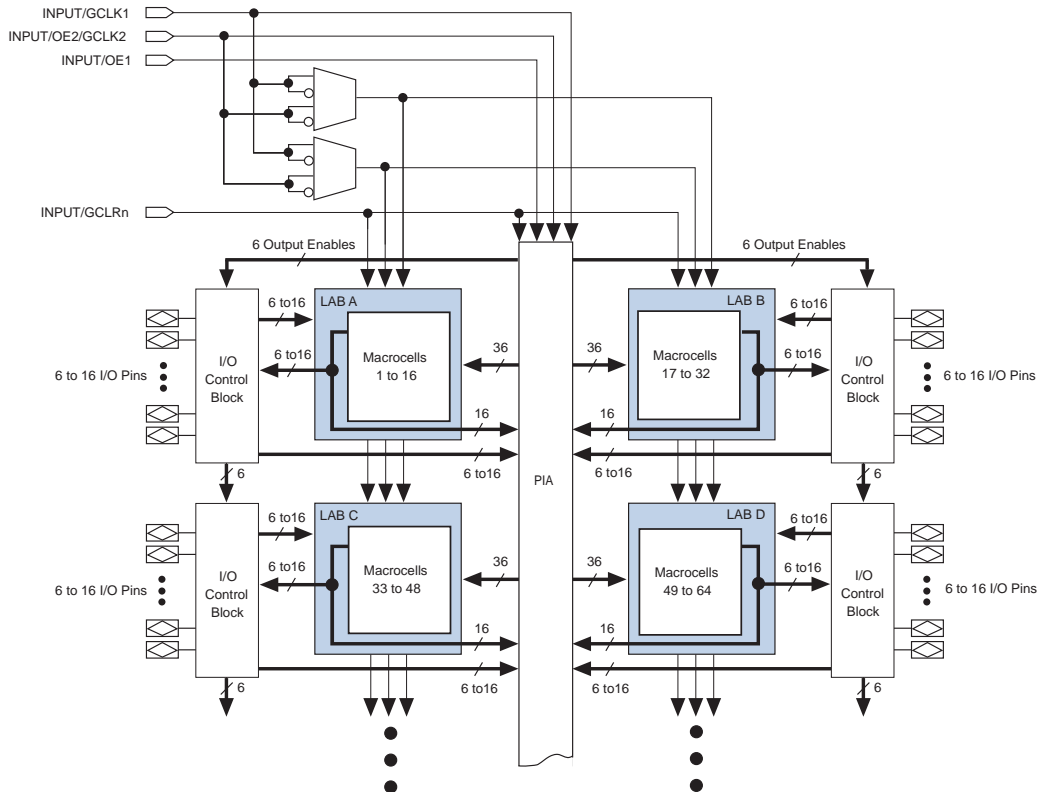
**Notes:**

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**



## Logic Array Blocks

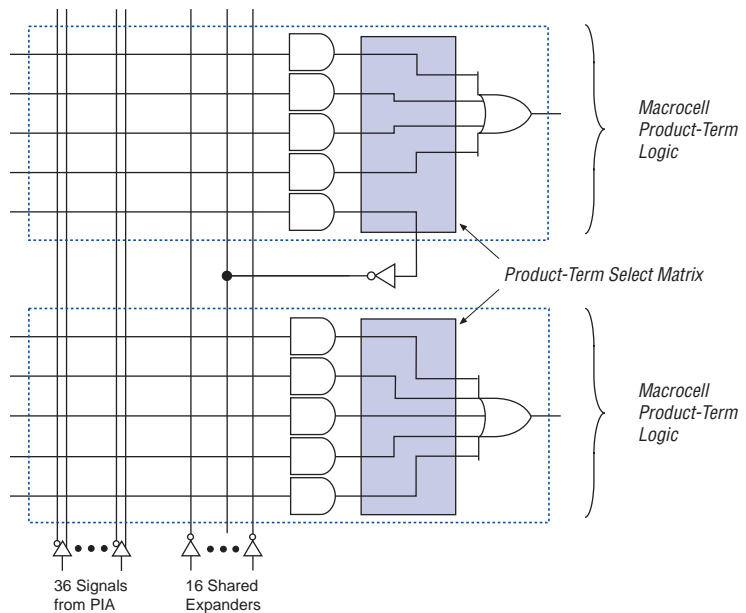
The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

### Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ( $t_{SEXP}$ ) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

**Figure 5. Shareable Expanders**

*Shareable expanders can be shared by any or all macrocells in an LAB.*



### Parallel Expanders

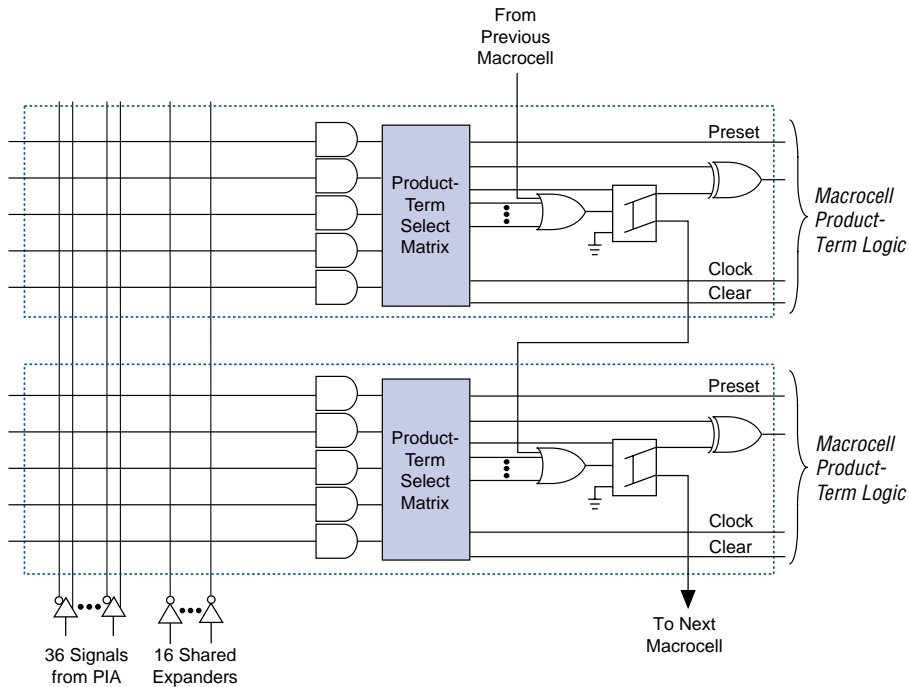
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay ( $t_{PEXP}$ ). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by  $2 \times t_{PEXP}$ .

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

**Figure 6. Parallel Expanders**

*Unused product terms in a macrocell can be allocated to a neighboring macrocell.*





## Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder ( $t_{LPA}$ ) for the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ , and  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters.

## Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

### MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of  $t_{OD2}$  instead of  $t_{OD1}$ .

### Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

**Table 15. MAX 7000 5.0-V Device DC Operating Conditions** *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{IH}$	High-level input voltage		2.0	$V_{CCINT} + 0.5$	V
$V_{IL}$	Low-level input voltage		-0.5 (8)	0.8	V
$V_{OH}$	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V (10)	$V_{CCIO} - 0.2$		V
$V_{OL}$	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (11)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V (11)		0.2	V
$I_I$	Leakage current of dedicated input pins	$V_I = -0.5$ to $5.5$ V (11)	-10	10	$\mu$ A
$I_{OZ}$	I/O pin tri-state output off-state current	$V_I = -0.5$ to $5.5$ V (11), (12)	-40	40	$\mu$ A

**Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices** *Note (13)*

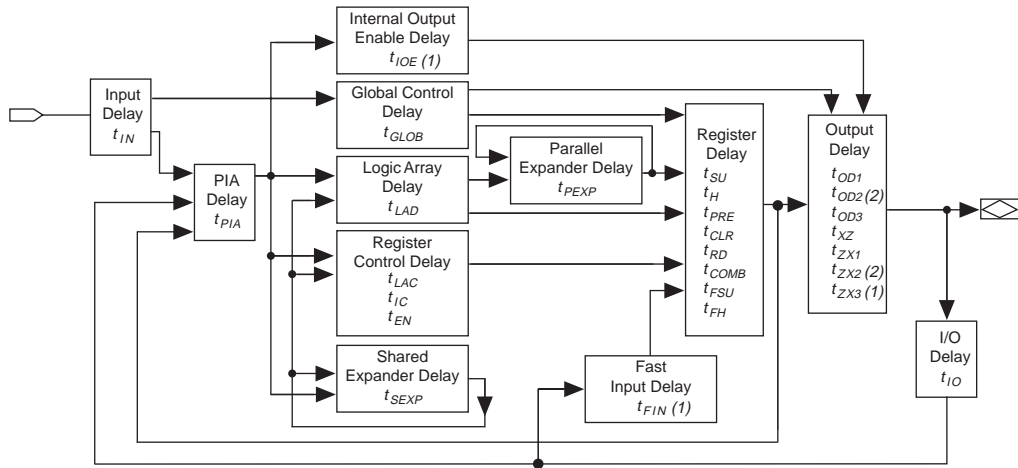
Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

**Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices** *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		15	pF

**Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices** *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
$C_{IN}$	Dedicated input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

**Figure 12. MAX 7000 Timing Model****Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see *Application Note 94 (Understanding MAX 7000 Timing)*.

Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

**Table 19. MAX 7000 & MAX 7000E External Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
$t_{SU}$	Global clock setup time		5.0		6.0		ns
$t_H$	Global clock hold time		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input	(2)	2.5		3.0		ns
$t_{FH}$	Global clock hold time of fast input	(2)	0.5		0.5		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
$t_{CH}$	Global clock high time		2.5		3.0		ns
$t_{CL}$	Global clock low time		2.5		3.0		ns
$t_{ASU}$	Array clock setup time		2.5		3.0		ns
$t_{AH}$	Array clock hold time		2.0		2.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
$t_{ACH}$	Array clock high time		3.0		3.0		ns
$t_{ACL}$	Array clock low time		3.0		3.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			6.6		8.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
$t_{ACNT}$	Minimum array clock period			6.6		8.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
$f_{MAX}$	Maximum clock frequency	(6)	200		166.7		MHz

**Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.5		1.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.5		1.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			5.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.8		0.8	ns
$t_{LAD}$	Logic array delay			5.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.5		2.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		2.5	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.5		6.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		5.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		5.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		5.0		5.0	ns
$t_{SU}$	Register setup time		2.0		3.0		ns
$t_H$	Register hold time		3.0		3.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.5		0.5		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			5.0		5.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0	ns
$t_{PRE}$	Register preset time			3.0		3.0	ns
$t_{CLR}$	Register clear time			3.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		11.0	ns

**Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			1.0		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			1.0		2.0	ns
$t_{FIN}$	Fast input delay	(2)		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			7.0		7.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0	ns
$t_{LAD}$	Logic array delay			7.0		5.0	ns
$t_{LAC}$	Logic control array delay			5.0		5.0	ns
$t_{IOE}$	Internal output enable delay	(2)		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
$t_{SU}$	Register setup time		1.0		4.0		ns
$t_H$	Register hold time		6.0		4.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	4.0		2.0		ns
$t_{FH}$	Register hold time of fast input	(2)	0.0		2.0		ns
$t_{RD}$	Register delay			2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			2.0		1.0	ns
$t_{IC}$	Array clock delay			5.0		5.0	ns
$t_{EN}$	Register enable time			7.0		5.0	ns
$t_{GLOB}$	Global control delay			2.0		0.0	ns
$t_{PRE}$	Register preset time			4.0		3.0	ns
$t_{CLR}$	Register clear time			4.0		3.0	ns
$t_{PIA}$	PIA delay			1.0		1.0	ns
$t_{LPA}$	Low-power adder	(8)		12.0		12.0	ns

**Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			2.0		2.0		3.0	ns
$t_{IO}$	I/O input pad and buffer delay			2.0		2.0		3.0	ns
$t_{FIN}$	Fast input delay	(2)		2.0		–		4.0	ns
$t_{SEXP}$	Shared expander delay			8.0		10.0		9.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0		2.0	ns
$t_{LAD}$	Logic array delay			6.0		6.0		8.0	ns
$t_{LAC}$	Logic control array delay			6.0		6.0		8.0	ns
$t_{IOE}$	Internal output enable delay	(2)		3.0		–		4.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		5.0		–		6.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		8.0		–		9.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.0		10.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		7.0		–		11.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		10.0		–		14.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		6.0		6.0		10.0	ns
$t_{SU}$	Register setup time		4.0		4.0		4.0		ns
$t_H$	Register hold time		4.0		4.0		5.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	2.0		–		4.0		ns
$t_{FH}$	Register hold time of fast input	(2)	2.0		–		3.0		ns
$t_{RD}$	Register delay			1.0		1.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.0		1.0	ns
$t_{IC}$	Array clock delay			6.0		6.0		8.0	ns
$t_{EN}$	Register enable time			6.0		6.0		8.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0		3.0	ns
$t_{PRE}$	Register preset time			4.0		4.0		4.0	ns
$t_{CLR}$	Register clear time			4.0		4.0		4.0	ns
$t_{PIA}$	PIA delay			2.0		2.0		3.0	ns
$t_{LPA}$	Low-power adder	(8)		13.0		15.0		15.0	ns

**Table 27. EPM7032S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 28. EPM7032S Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.3		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.3		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.1		2.5		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.6		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		1.4		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.3		4.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.3		4.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		1.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		0.4		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		0.9		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		5.4		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		1.3		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.5		3.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		1.8		1.7		3.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.7		0.8		0.5		ns
$t_{RD}$	Register delay			1.2		1.6		1.9		2.0	ns
$t_{COMB}$	Combinatorial delay			0.9		1.1		1.4		2.0	ns
$t_{IC}$	Array clock delay			2.7		3.4		4.2		5.0	ns
$t_{EN}$	Register enable time			2.6		3.3		4.0		5.0	ns
$t_{GLOB}$	Global control delay			1.6		1.4		1.7		1.0	ns
$t_{PRE}$	Register preset time			2.0		2.4		3.0		3.0	ns
$t_{CLR}$	Register clear time			2.0		2.4		3.0		3.0	ns



**Table 29. EPM7064S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.6		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.2		3.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.2		3.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		3.0		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.0		3.0		ns

**Table 34. EPM7160S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{CLR}$	Register clear time			2.4		3.0		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		1.6		2.0		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 35 and 36 show the EPM7192S AC operating conditions.

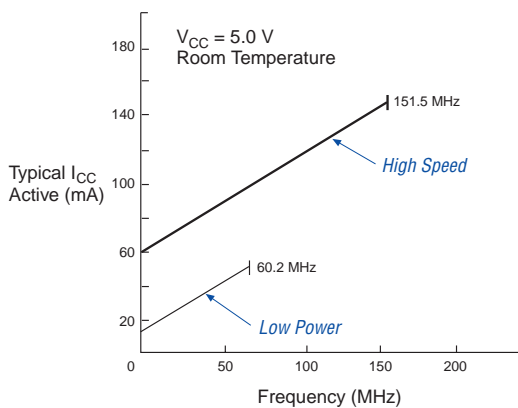
**Table 35. EPM7192S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		4.1		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		1.0		2.0		4.0		ns

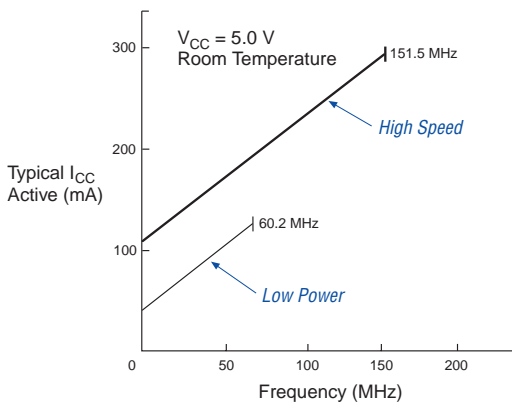
Figure 14 shows typical supply current versus frequency for MAX 7000 devices.

Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 1 of 2)

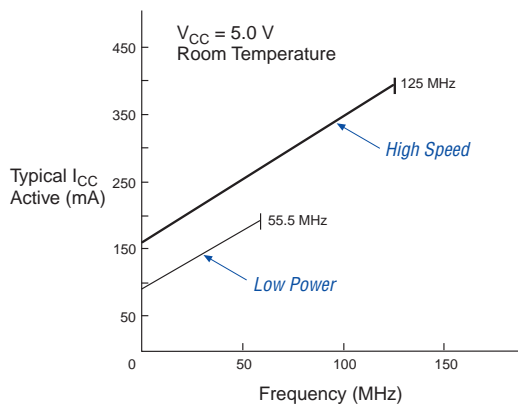
EPM7032



EPM7064

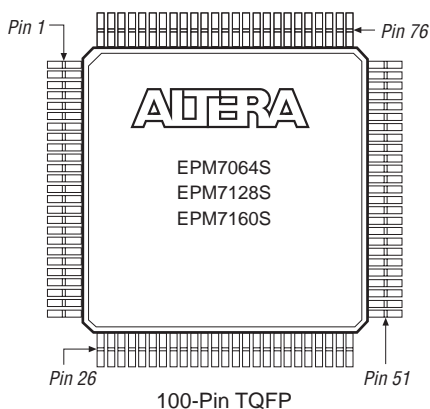
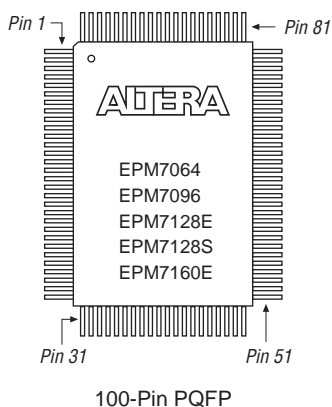


EPM7096



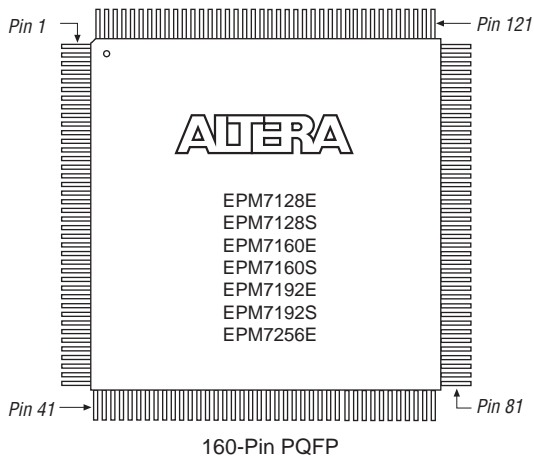
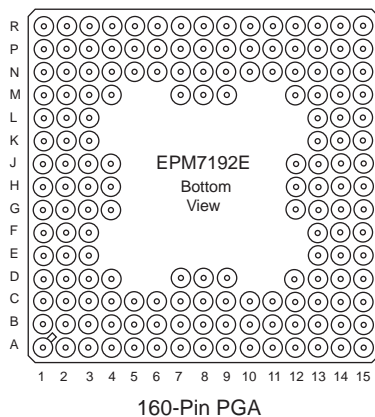
**Figure 19. 100-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.



**Figure 20. 160-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.





*Notes:*