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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	10
Number of Macrocells	160
Number of Gates	3200
Number of I/O	84
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7160sti100-10n">https://www.e-xfl.com/product-detail/intel/epm7160sti100-10n</a>

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera’s Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera’s second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

**Table 3. MAX 7000 Speed Grades**

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See [Table 5](#).

**Table 5. MAX 7000 Maximum User I/O Pins** *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 (2)	100				
EPM7160E					64	84		104				
EPM7160S					64		84 (2)	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 (2)		164		164
EPM7256S											164 (2)	164

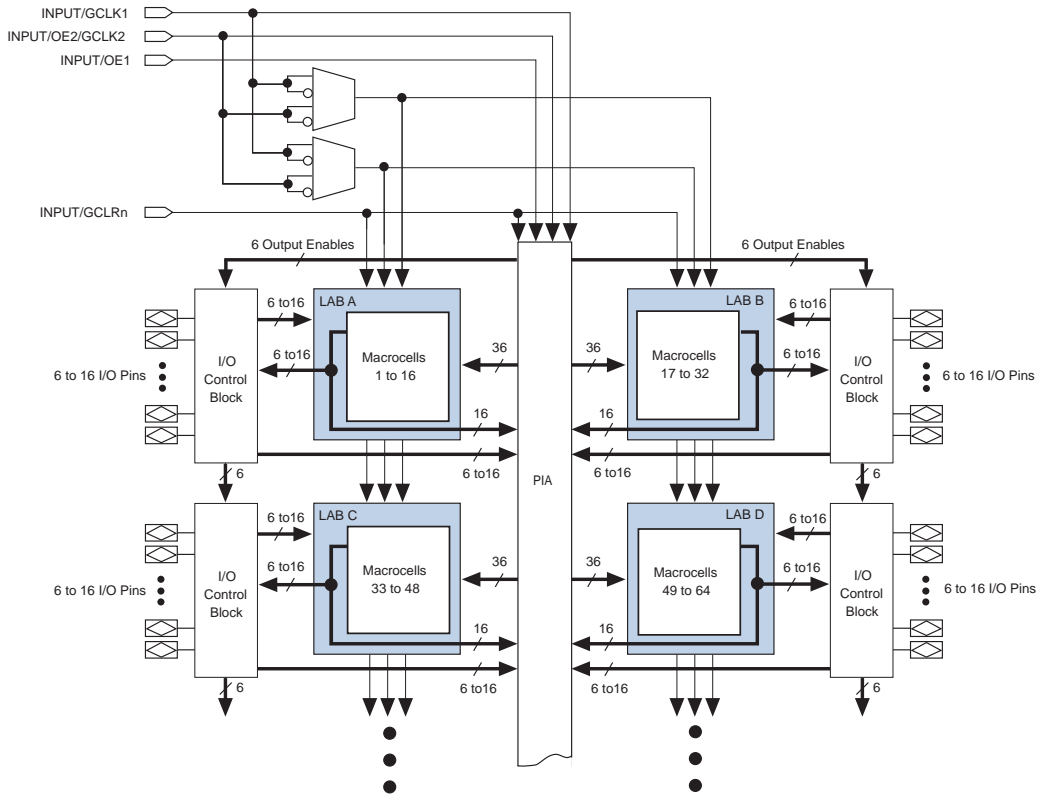
**Notes:**

- (1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.
- (2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the [Operating Requirements for Altera Devices Data Sheet](#).

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

Figure 2. MAX 7000E & MAX 7000S Device Block Diagram



### Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

### Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

## Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

**Figure 7. PIA Routing**



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

## I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or  $V_{CC}$ . Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.



For more information on using the Jam language, refer to *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

The ISP circuitry in MAX 7000S devices is compatible with IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

## Programming Sequence

During in-system programming, instructions, addresses, and data are shifted into the MAX 7000S device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data.

Programming a pattern into the device requires the following six ISP stages. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6.

1. *Enter ISP.* The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode. The enter ISP stage requires 1 ms.
2. *Check ID.* Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Bulk Erase.* Erasing the device in-system involves shifting in the instructions to erase the device and applying one erase pulse of 100 ms.
4. *Program.* Programming the device in-system involves shifting in the address and data and then applying the programming pulse to program the EEPROM cells. This process is repeated for each EEPROM address.
5. *Verify.* Verifying an Altera device in-system involves shifting in addresses, applying the read pulse to verify the EEPROM cells, and shifting out the data for comparison. This process is repeated for each EEPROM address.
6. *Exit ISP.* An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode. The exit ISP stage requires 1 ms.

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

**Table 10. MAX 7000S Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EPM7032S	1 (1)
EPM7064S	1 (1)
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

**Note:**

- (1) This device does not support JTAG boundary-scan testing. Selecting either the EXTTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

**Table 11. 32-Bit MAX 7000 Device IDCODE** *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

**Notes:**

- (1) The most significant bit (MSB) is on the left.
- (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.



Figure 9 shows the timing requirements for the JTAG signals.

**Figure 9. MAX 7000 JTAG Waveforms**

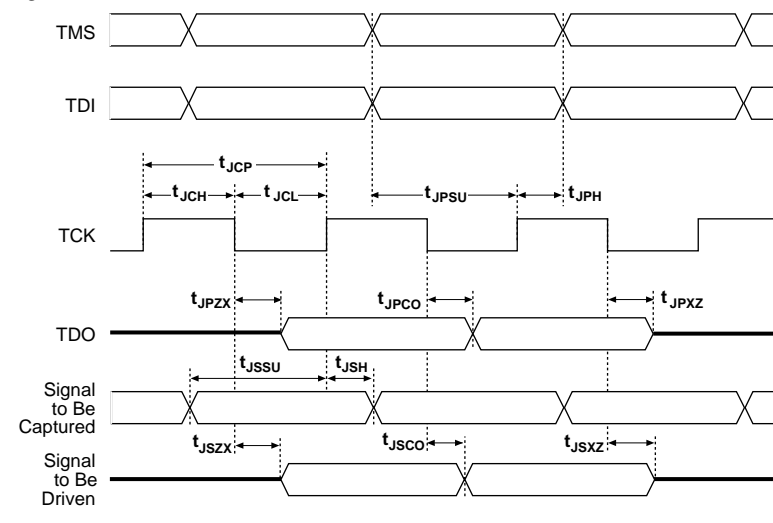


Table 12 shows the JTAG timing parameters and values for MAX 7000S devices.

Symbol	Parameter	Min	Max	Unit
$t_{JCP}$	TCK clock period	100		ns
$t_{JCH}$	TCK clock high time	50		ns
$t_{JCL}$	TCK clock low time	50		ns
$t_{JPSU}$	JTAG port setup time	20		ns
$t_{JPH}$	JTAG port hold time	45		ns
$t_{JPCO}$	JTAG port clock to output		25	ns
$t_{JPZX}$	JTAG port high impedance to valid output		25	ns
$t_{JPXZ}$	JTAG port valid output to high impedance		25	ns
$t_{JSSU}$	Capture register setup time	20		ns
$t_{JSH}$	Capture register hold time	45		ns
$t_{JSCO}$	Update register clock to output		25	ns
$t_{JSZX}$	Update register high impedance to valid output		25	ns
$t_{JSXZ}$	Update register valid output to high impedance		25	ns



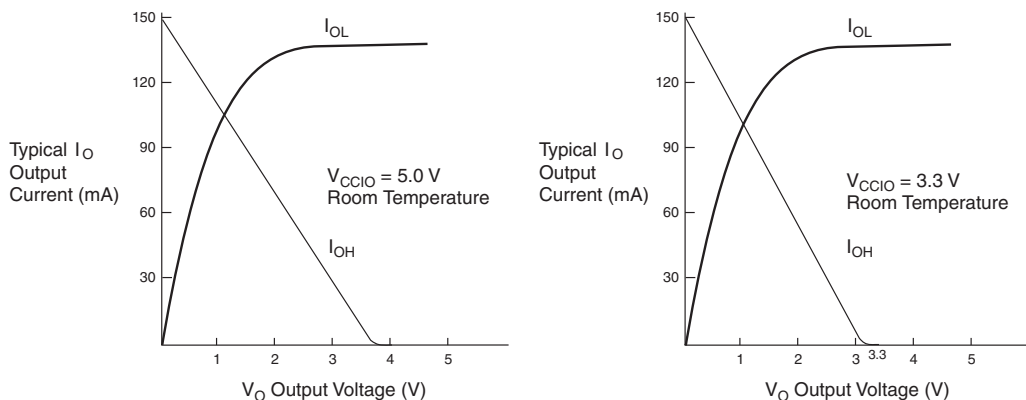
For more information, see [Application Note 39 \(IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices\)](#).

**Notes to tables:**

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage on I/O pins is  $-0.5\text{ V}$  and on 4 dedicated input pins is  $-0.3\text{ V}$ . During transitions, the inputs may undershoot to  $-2.0\text{ V}$  or overshoot to  $7.0\text{ V}$  for input currents less than  $100\text{ mA}$  and periods shorter than  $20\text{ ns}$ .
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4)  $V_{CC}$  must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed  $300\text{ }\mu\text{s}$ . The sufficient  $V_{CCINT}$  voltage level for POR is  $4.5\text{ V}$ . The device is fully initialized within the POR time after  $V_{CCINT}$  reaches the sufficient POR voltage level.
- (6)  $3.3\text{-V}$  I/O operation is not available for 44-pin packages.
- (7) The  $V_{CCISF}$  parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is  $-0.3\text{ V}$ .
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The  $I_{OH}$  parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The  $I_{OL}$  parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically  $-60\text{ }\mu\text{A}$ .
- (13) Capacitance is measured at  $25^\circ\text{ C}$  and is sample-tested only. The  $\text{OE}1$  pin has a maximum capacitance of  $20\text{ pF}$ .

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

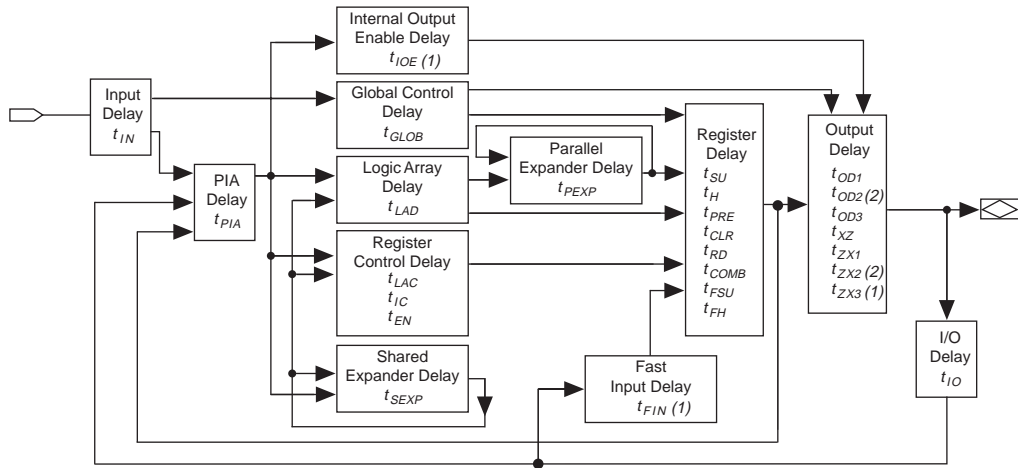
**Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices**



**Timing Model**

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Figure 12. MAX 7000 Timing Model

**Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).

Table 21. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
$t_{SU}$	Global clock setup time		7.0		8.0		ns
$t_H$	Global clock hold time		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Global clock hold time of fast input	(2)	0.5		0.5		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		5.0		5	ns
$t_{CH}$	Global clock high time		4.0		4.0		ns
$t_{CL}$	Global clock low time		4.0		4.0		ns
$t_{ASU}$	Array clock setup time		2.0		3.0		ns
$t_{AH}$	Array clock hold time		3.0		3.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
$t_{ACH}$	Array clock high time		4.0		4.0		ns
$t_{ACL}$	Array clock low time		4.0		4.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			10.0		10.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
$t_{ACNT}$	Minimum array clock period			10.0		10.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
$f_{MAX}$	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 23. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
$t_{SU}$	Global clock setup time		7.0		10.0		ns
$t_H$	Global clock hold time		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input	(2)	3.0		3.0		ns
$t_{FH}$	Global clock hold time of fast input	(2)	0.0		0.0		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
$t_{CH}$	Global clock high time		4.0		4.0		ns
$t_{CL}$	Global clock low time		4.0		4.0		ns
$t_{ASU}$	Array clock setup time		3.0		4.0		ns
$t_{AH}$	Array clock hold time		4.0		4.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
$t_{ACH}$	Array clock high time		5.0		5.0		ns
$t_{ACL}$	Array clock low time		5.0		5.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			11.0		11.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
$t_{ACNT}$	Minimum array clock period			11.0		11.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
$f_{MAX}$	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 25. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
$t_{PD2}$	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
$t_{SU}$	Global clock setup time		11.0		11.0		12.0		ns
$t_H$	Global clock hold time		0.0		0.0		0.0		ns
$t_{FSU}$	Global clock setup time of fast input	(2)	3.0		–		5.0		ns
$t_{FH}$	Global clock hold time of fast input	(2)	0.0		–		0.0		ns
$t_{CO1}$	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
$t_{CH}$	Global clock high time		5.0		6.0		6.0		ns
$t_{CL}$	Global clock low time		5.0		6.0		6.0		ns
$t_{ASU}$	Array clock setup time		4.0		4.0		5.0		ns
$t_{AH}$	Array clock hold time		4.0		4.0		5.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
$t_{ACH}$	Array clock high time		6.0		6.5		8.0		ns
$t_{ACL}$	Array clock low time		6.0		6.5		8.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(3)	6.0		6.5		8.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			13.0		13.0		16.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(5)	76.9		76.9		62.5		MHz
$t_{ACNT}$	Minimum array clock period			13.0		13.0		16.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(5)	76.9		76.9		62.5		MHz
$f_{MAX}$	Maximum clock frequency	(6)	100		83.3		83.3		MHz

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{PD1}$	Input to non-registered output	$C1 = 35\text{ pF}$	5.0		6.0		7.5		10.0	ns	
$t_{PD2}$	I/O input to non-registered output	$C1 = 35\text{ pF}$	5.0		6.0		7.5		10.0	ns	
$t_{SU}$	Global clock setup time		2.9		4.0		5.0		7.0	ns	
$t_H$	Global clock hold time		0.0		0.0		0.0		0.0	ns	
$t_{FSU}$	Global clock setup time of fast input		2.5		2.5		2.5		3.0	ns	
$t_{FH}$	Global clock hold time of fast input		0.0		0.0		0.0		0.5	ns	
$t_{CO1}$	Global clock to output delay	$C1 = 35\text{ pF}$	3.2		3.5		4.3		5.0	ns	
$t_{CH}$	Global clock high time		2.0		2.5		3.0		4.0	ns	
$t_{CL}$	Global clock low time		2.0		2.5		3.0		4.0	ns	
$t_{ASU}$	Array clock setup time		0.7		0.9		1.1		2.0	ns	
$t_{AH}$	Array clock hold time		1.8		2.1		2.7		3.0	ns	
$t_{ACO1}$	Array clock to output delay	$C1 = 35\text{ pF}$	5.4		6.6		8.2		10.0	ns	
$t_{ACH}$	Array clock high time		2.5		2.5		3.0		4.0	ns	
$t_{ACL}$	Array clock low time		2.5		2.5		3.0		4.0	ns	
$t_{CPPW}$	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0	ns	
$t_{ODH}$	Output data hold time after clock	$C1 = 35\text{ pF}$ (3)	1.0		1.0		1.0		1.0	ns	
$t_{CNT}$	Minimum global clock period		5.7		7.0		8.6		10.0	ns	
$f_{CNT}$	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0	MHz	
$t_{ACNT}$	Minimum array clock period		5.7		7.0		8.6		10.0	ns	

**Table 29. EPM7064S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
$t_{ACH}$	Array clock high time		2.5		2.5		3.0		4.0		ns
$t_{ACL}$	Array clock low time		2.5		2.5		3.0		4.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			5.7		7.1		8.0		10.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
$t_{ACNT}$	Minimum array clock period			5.7		7.1		8.0		10.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
$f_{MAX}$	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.6		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.2		3.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.2		3.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		3.0		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.0		3.0		ns



Table 33. EPM7160S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{ACNT}$	Minimum array clock period			6.7		8.2		10.0		13.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(4)	149.3		122.0		100.0		76.9		MHz
$f_{MAX}$	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			2.6		3.2		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.6		4.3		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.3		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.8		3.4		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.8		3.4		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.9		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.9		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.0		1.2		2.0		4.0		ns
$t_H$	Register hold time		1.6		2.0		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
$t_{RD}$	Register delay			1.3		1.6		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.3		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		3.5		5.0		6.0	ns
$t_{EN}$	Register enable time			2.8		3.4		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.0		2.4		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.4		3.0		3.0		4.0	ns

Table 35. EPM7192S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_{AH}$	Array clock hold time		1.8		3.0		4.0		ns
$t_{ACO1}$	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
$t_{ACH}$	Array clock high time		3.0		4.0		6.0		ns
$t_{ACL}$	Array clock low time		3.0		4.0		6.0		ns
$t_{CPPW}$	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
$t_{ODH}$	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
$t_{CNT}$	Minimum global clock period			8.0		10.0		13.0	ns
$f_{CNT}$	Maximum internal global clock frequency	(4)	125.0		100.0		76.9		MHz
$t_{ACNT}$	Minimum array clock period			8.0		10.0		13.0	ns
$f_{ACNT}$	Maximum internal array clock frequency	(4)	125.0		100.0		76.9		MHz
$f_{MAX}$	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

Table 36. EPM7192S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			3.2		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			4.2		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.2		0.8		1.0	ns
$t_{LAD}$	Logic array delay			3.1		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			3.1		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.9		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		7.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.1		2.0		4.0		ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

## Power Consumption

Supply power (P) versus frequency ( $f_{MAX}$  in MHz) for MAX 7000 devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The  $P_{IO}$  value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in [Application Note 74 \(Evaluating Power for Altera Devices\)](#).

The  $I_{CCINT}$  value, which depends on the switching frequency and the application logic, is calculated with the following equation:

$$I_{CCINT} = A \times MC_{TON} + B \times (MC_{DEV} - MC_{TON}) + C \times MC_{USED} \times f_{MAX} \times \text{tog}_{LC}$$

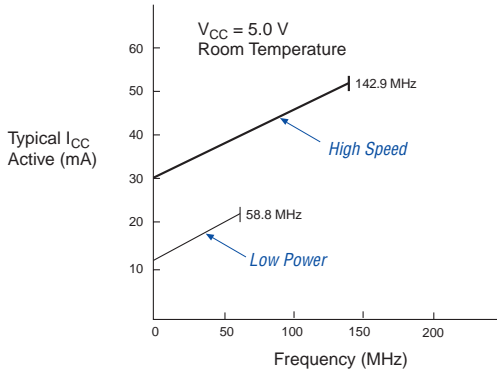
The parameters in this equation are shown below:

$MC_{TON}$	=	Number of macrocells with the Turbo Bit option turned on, as reported in the MAX+PLUS II Report File (.rpt)
$MC_{DEV}$	=	Number of macrocells in the device
$MC_{USED}$	=	Total number of macrocells in the design, as reported in the MAX+PLUS II Report File (.rpt)
$f_{MAX}$	=	Highest clock frequency to the device
$\text{tog}_{LC}$	=	Average ratio of logic cells toggling at each clock (typically 0.125)
A, B, C	=	Constants, shown in <a href="#">Table 39</a>

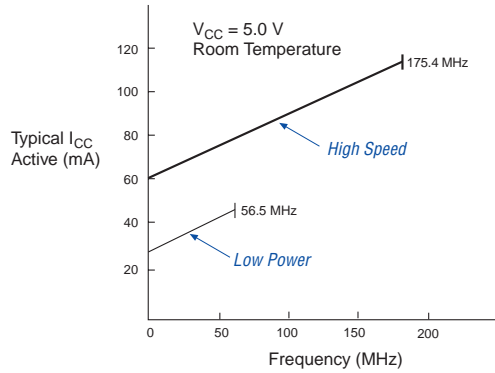
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 1 of 2)

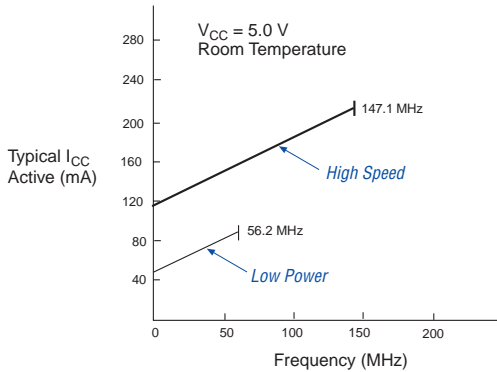
EPM7032S



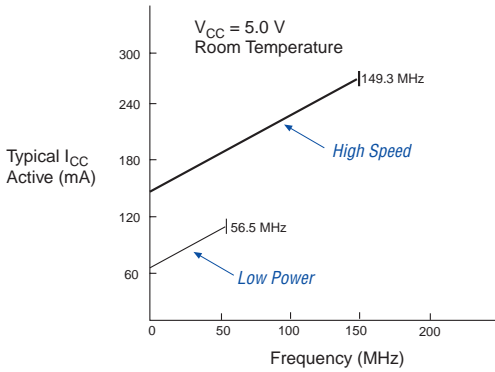
EPM7064S



EPM7128S

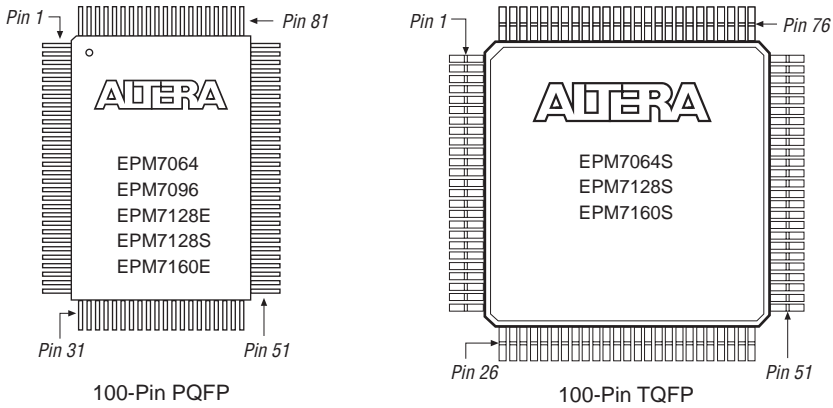


EPM7160S



**Figure 19. 100-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.



**Figure 20. 160-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

