



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	EE PLD
Delay Time tpd(1) Max	15 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	12
Number of Macrocells	192
Number of Gates	3750
Number of I/O	124
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7192eqc160-15yy

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See [Table 4](#).

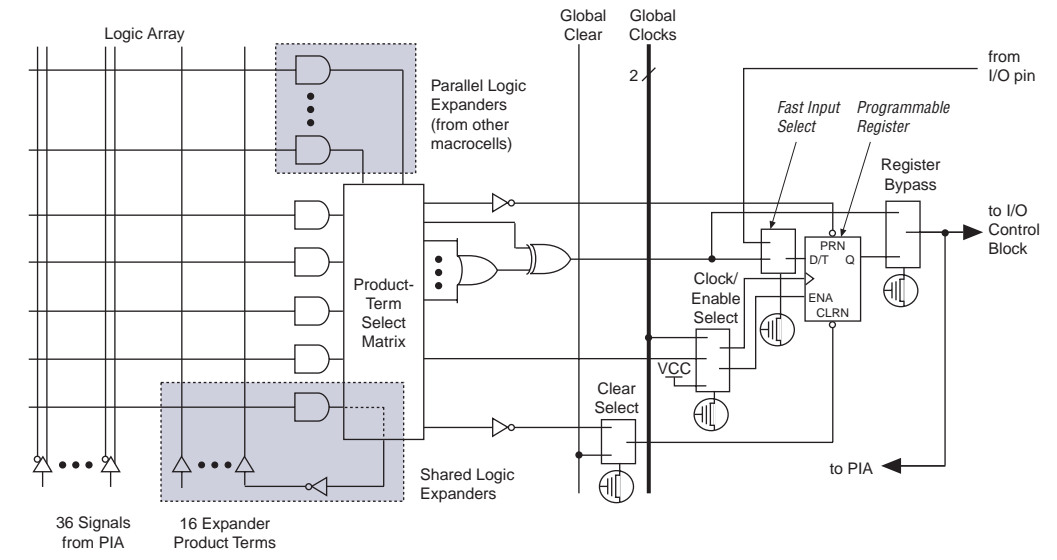
Table 4. MAX 7000 Device Features			
Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ ⁽¹⁾
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface ⁽²⁾	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:

- (1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
- (2) The MultiVolt I/O interface is not available in 44-pin packages.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

Figure 4. MAX 7000E & MAX 7000S Device Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In EPM7032, EPM7064, and EPM7096 devices, the global clock signal is available from a dedicated clock pin, GCLK1, as shown in [Figure 1](#). In MAX 7000E and MAX 7000S devices, two global clock signals are available. As shown in [Figure 2](#), these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in [Figures 3 and 4](#), the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in the device will be set to a low state.

All MAX 7000E and MAX 7000S I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be driven to an input D flipflop with an extremely fast (2.5 ns) input setup time.

Expander Product Terms

Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000 architecture also allows both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

By using an external 5.0-V pull-up resistor, output pins on MAX 7000S devices can be set to meet 5.0-V CMOS input voltages. When V_{CCIO} is 3.3 V, setting the open drain option will turn off the output pull-up transistor, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages. When V_{CCIO} is 5.0 V, setting the output drain option is not necessary because the pull-up transistor will already turn off when the pin exceeds approximately 3.8 V, allowing the external pull-up resistor to pull the output high enough to meet 5.0-V CMOS input voltages.

Slew-Rate Control

The output buffer for each MAX 7000E and MAX 7000S I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. In MAX 7000E devices, when the Turbo Bit is turned off, the slew rate is set for low noise performance. For MAX 7000S devices, each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis.

Programming with External Hardware

MAX 7000 devices can be programmed on Windows-based PCs with the Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs a continuity check to ensure adequate electrical contact between the adapter and the device.



For more information, see the [Altera Programming Hardware Data Sheet](#).

The Altera development system can use text- or waveform-format test vectors created with the Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation. Moreover, Data I/O, BP Microsystems, and other programming hardware manufacturers also provide programming support for Altera devices.



For more information, see the [Programming Hardware Manufacturers](#).

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. [Table 9](#) describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 9. MAX 7000 JTAG Instructions

JTAG Instruction	Devices	Description
SAMPLE/PRELOAD	EPM7128S EPM7160S EPM7192S EPM7256S	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	EPM7128S EPM7160S EPM7192S EPM7256S	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ISP Instructions	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (.jam), Jam Byte-Code file (.jbc), or Serial Vector Format file (.svf) via an embedded processor or test equipment.

The instruction register length of MAX 7000S devices is 10 bits. Tables 10 and 11 show the boundary-scan register length and device IDCODE information for MAX 7000S devices.

Table 10. MAX 7000S Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032S	1 (1)
EPM7064S	1 (1)
EPM7128S	288
EPM7160S	312
EPM7192S	360
EPM7256S	480

Note:

- (1) This device does not support JTAG boundary-scan testing. Selecting either the EXTEST or SAMPLE/PRELOAD instruction will select the one-bit bypass register.

Table 11. 32-Bit MAX 7000 Device IDCODE Note (1)

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) (2)
EPM7032S	0000	0111 0000 0011 0010	00001101110	1
EPM7064S	0000	0111 0000 0110 0100	00001101110	1
EPM7128S	0000	0111 0001 0010 1000	00001101110	1
EPM7160S	0000	0111 0001 0110 0000	00001101110	1
EPM7192S	0000	0111 0001 1001 0010	00001101110	1
EPM7256S	0000	0111 0010 0101 0110	00001101110	1

Notes:

- (1) The most significant bit (MSB) is on the left.
 (2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	$V_{CCINT} + 0.5$	V
V_{IL}	Low-level input voltage		-0.5 (8)	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 4.75$ V (10)	2.4		V
	3.3-V high-level TTL output voltage	$I_{OH} = -4$ mA DC, $V_{CCIO} = 3.00$ V (10)	2.4		V
	3.3-V high-level CMOS output voltage	$I_{OH} = -0.1$ mA DC, $V_{CCIO} = 3.0$ V (10)	$V_{CCIO} - 0.2$		V
V_{OL}	5.0-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 4.75$ V (11)		0.45	V
	3.3-V low-level TTL output voltage	$I_{OL} = 12$ mA DC, $V_{CCIO} = 3.00$ V (11)		0.45	V
	3.3-V low-level CMOS output voltage	$I_{OL} = 0.1$ mA DC, $V_{CCIO} = 3.0$ V (11)		0.2	V
I_I	Leakage current of dedicated input pins	$V_I = -0.5$ to 5.5 V (11)	-10	10	μ A
I_{OZ}	I/O pin tri-state output off-state current	$V_I = -0.5$ to 5.5 V (11), (12)	-40	40	μ A

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		12	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		15	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*

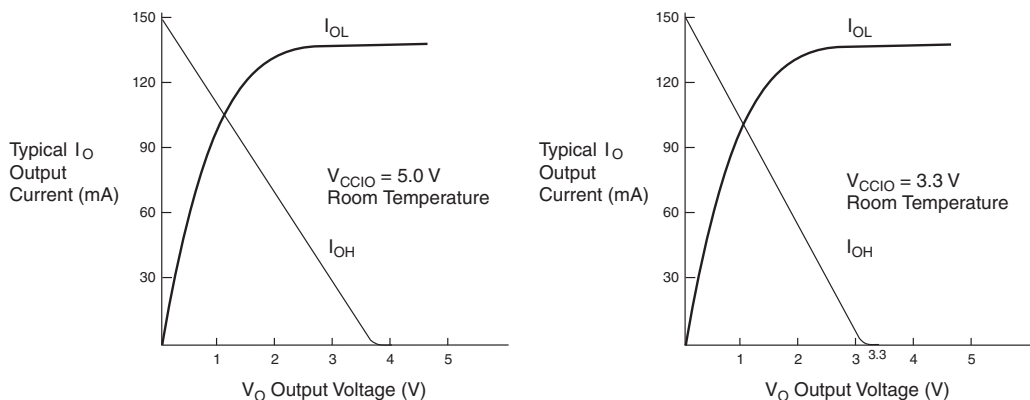
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	$V_{IN} = 0$ V, $f = 1.0$ MHz		10	pF
$C_{I/O}$	I/O pin capacitance	$V_{OUT} = 0$ V, $f = 1.0$ MHz		10	pF

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage on I/O pins is -0.5 V and on 4 dedicated input pins is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) V_{CC} must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed 300 μ s. The sufficient V_{CCINT} voltage level for POR is 4.5 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
- (6) 3.3 -V I/O operation is not available for 44-pin packages.
- (7) The V_{CCISP} parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is -0.3 V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically -60 μ A.
- (13) Capacitance is measured at 25° C and is sample-tested only. The $\text{OE}1$ pin has a maximum capacitance of 20 pF.

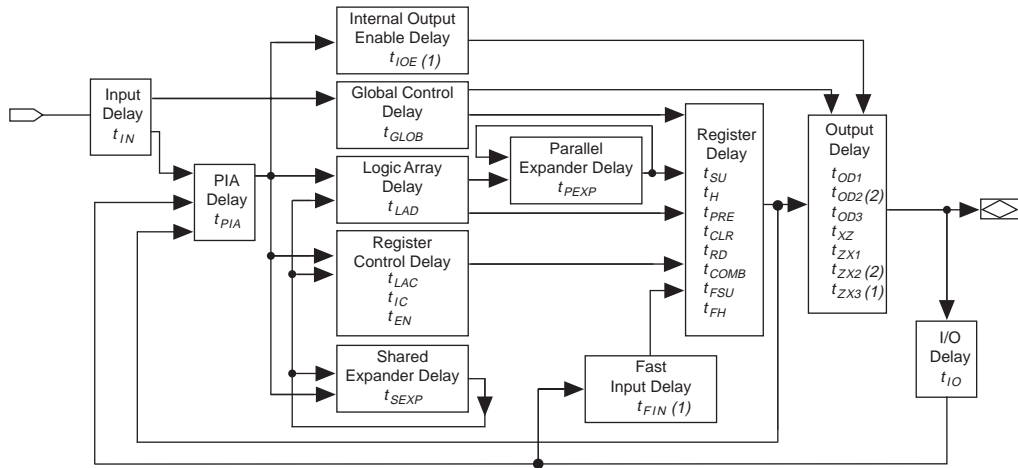
Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Figure 12. MAX 7000 Timing Model**Notes:**

- (1) Only available in MAX 7000E and MAX 7000S devices.
- (2) Not available in 44-pin devices.

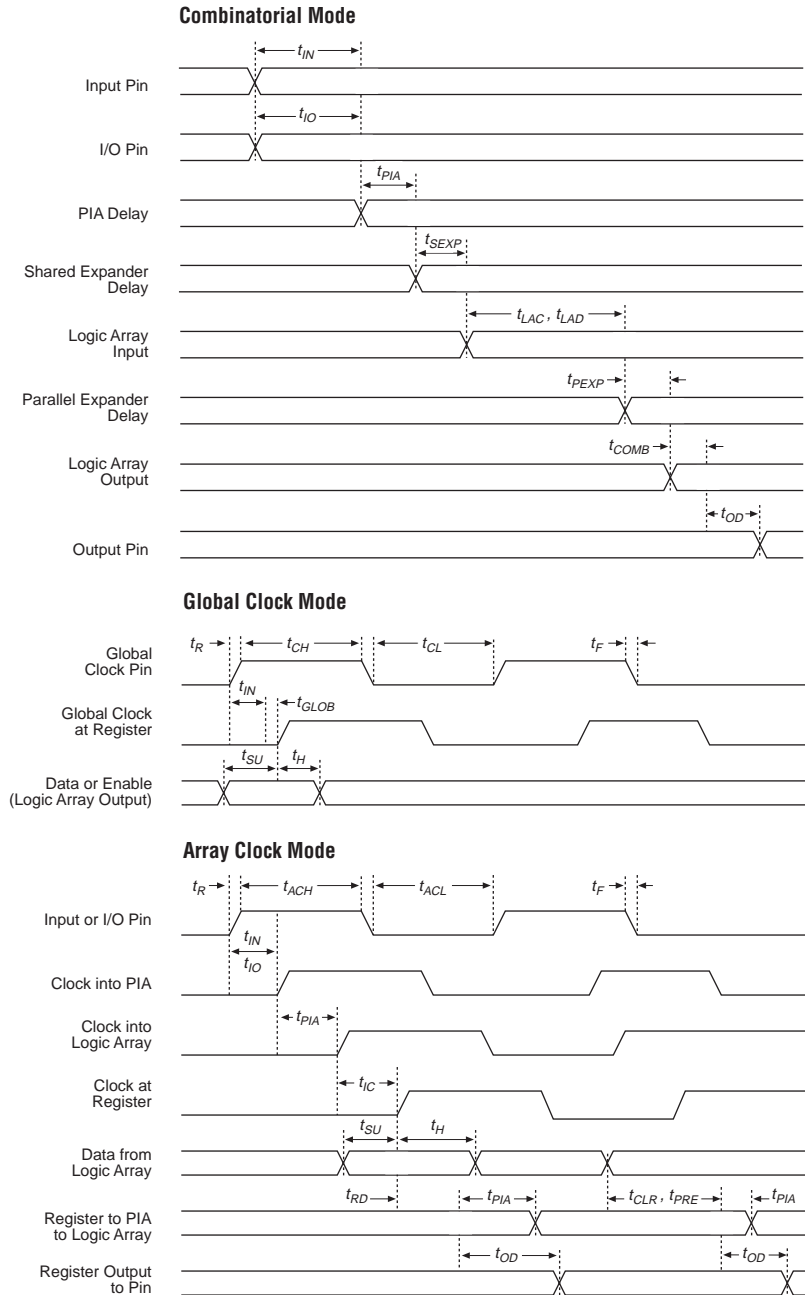
The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 13 shows the internal timing relationship of internal and external delay parameters.



For more information, see [Application Note 94 \(Understanding MAX 7000 Timing\)](#).

Figure 13. Switching Waveforms

t_R & $t_F < 3$ ns.
Inputs are driven at 3 V
for a logic high and 0 V
for a logic low. All timing
characteristics are
measured at 1.5 V.



Tables 19 through 26 show the MAX 7000 and MAX 7000E AC operating conditions.

Table 19. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	-6 Speed Grade		-7 Speed Grade		Unit
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_H	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

Table 20. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade -6		Speed Grade -7		Unit
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.5	ns
t_{FIN}	Fast input delay	(2)		0.8		1.0	ns
t_{SEXP}	Shared expander delay			3.5		4.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			2.0		3.0	ns
t_{LAC}	Logic control array delay			2.0		3.0	ns
t_{OE}	Internal output enable delay	(2)				2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		2.0		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		7.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		4.0		4.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off, $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		4.0		4.0	ns
t_{SU}	Register setup time		3.0		3.0		ns
t_H	Register hold time		1.5		2.0		ns
t_{FSU}	Register setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Register hold time of fast input	(2)	0.5		0.5		ns
t_{RD}	Register delay			0.8		1.0	ns
t_{COMB}	Combinatorial delay			0.8		1.0	ns
t_{JC}	Array clock delay			2.5		3.0	ns
t_{EN}	Register enable time			2.0		3.0	ns
t_{GLOB}	Global control delay			0.8		1.0	ns
t_{PRE}	Register preset time			2.0		2.0	ns
t_{CLR}	Register clear time			2.0		2.0	ns
t_{PIA}	PIA delay			0.8		1.0	ns
t_{LPA}	Low-power adder	(8)		10.0		10.0	ns

Table 23. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{SU}	Global clock setup time		7.0		10.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		3.0		4.0		ns
t _{AH}	Array clock hold time		4.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t _{ACH}	Array clock high time		5.0		5.0		ns
t _{ACL}	Array clock low time		5.0		5.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			11.0		11.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t _{ACNT}	Minimum array clock period			11.0		11.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	(7)		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		10.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} , and t_{CPPW} parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t _{SU}	Global clock setup time		2.9		3.6		6.0		7.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
t _{CH}	Global clock high time		2.0		2.5		3.0		4.0		ns
t _{CL}	Global clock low time		2.0		2.5		3.0		4.0		ns
t _{ASU}	Array clock setup time		0.7		0.9		3.0		2.0		ns
t _{AH}	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t _{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t _{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t _{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_H	Register hold time		1.7		2.0		2.0		3.0		ns

Tables 37 and 38 show the EPM7256S AC operating conditions.

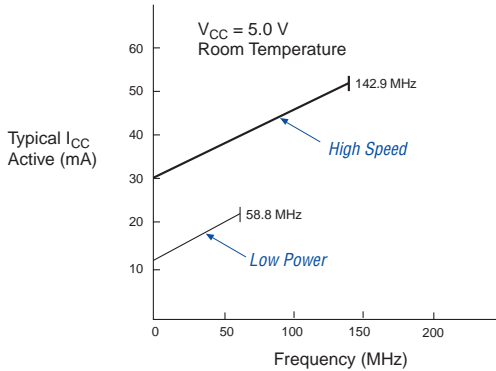
Table 37. EPM7256S External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.9		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t _{AH}	Array clock hold time		1.9		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			7.8		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			7.8		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

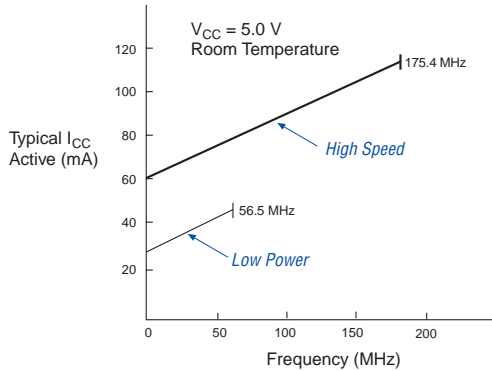
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

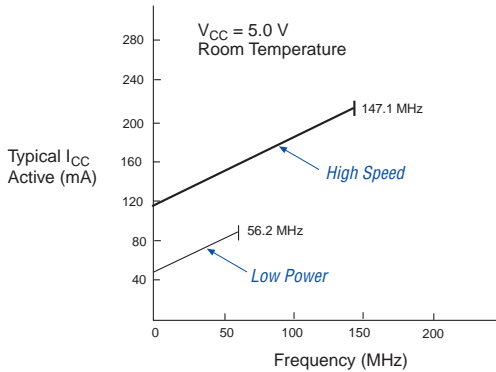
EPM7032S



EPM7064S



EPM7128S



EPM7160S

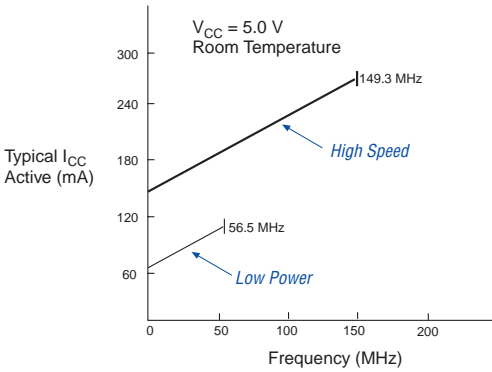
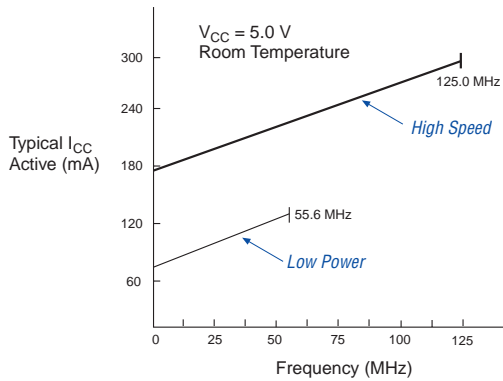
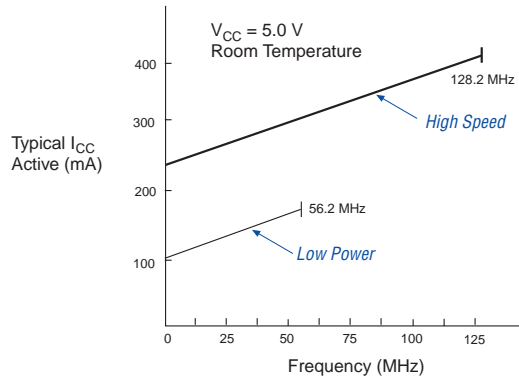


Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)

EPM7192S

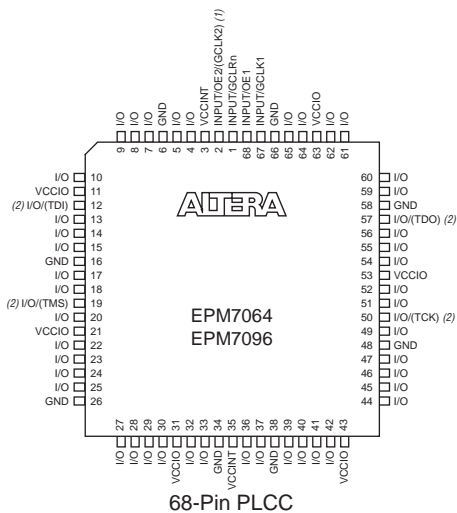


EPM7256S



Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figure 17. 68-Pin Package Pin-Out Diagram*Package outlines not drawn to scale.***Notes:**

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).