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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256sqc160-12

Table 2. MAX 7000S Device Features

Feature	EPM7032S	EPM7064S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
Usable gates	600	1,250	2,500	3,200	3,750	5,000
Macrocells	32	64	128	160	192	256
Logic array blocks	2	4	8	10	12	16
Maximum user I/O pins	36	68	100	104	124	164
t_{PD} (ns)	5	5	6	6	7.5	7.5
t_{SU} (ns)	2.9	2.9	3.4	3.4	4.1	3.9
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3
t_{CO1} (ns)	3.2	3.2	4	3.9	4.7	4.7
f_{CNT} (MHz)	175.4	175.4	147.1	149.3	125.0	128.2

…and More Features

- Open-drain output option in MAX 7000S devices
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for a reduction of over 50% in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- 44 to 208 pins available in plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and 1.0-mm thin quad flat pack (TQFP) packages
- Programmable security bit for protection of proprietary designs
- 3.3-V or 5.0-V operation
  - MultiVolt™ I/O interface operation, allowing devices to interface with 3.3-V or 5.0-V devices (MultiVolt I/O operation is not available in 44-pin packages)
  - Pin compatible with low-voltage MAX 7000A and MAX 7000B devices
- Enhanced features available in MAX 7000E and MAX 7000S devices
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by Altera's development system for Windows-based PCs and Sun SPARCstation, and HP 9000 Series 700/800 workstations

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See Table 4.

Table 4. MAX 7000 Device Features

Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ *(1)*
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface *(2)*	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:
(1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
(2) The MultiVolt I/O interface is not available in 44-pin packages.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. The MAX 7000 architecture easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000 devices are available in a wide range of packages, including PLCC, PGA, PQFP, RQFP, and TQFP packages. See Table 5.

Table 5. MAX 7000 Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	100-Pin TQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin PQFP	208-Pin RQFP
EPM7032	36	36	36									
EPM7032S	36		36									
EPM7064	36		36	52	68	68						
EPM7064S	36		36		68		68					
EPM7096				52	64	76						
EPM7128E					68	84		100				
EPM7128S					68	84	84 *(2)*	100				
EPM7160E					64	84		104				
EPM7160S					64		84 *(2)*	104				
EPM7192E								124	124			
EPM7192S								124				
EPM7256E								132 *(2)*		164		164
EPM7256S											164 *(2)*	164

Notes:

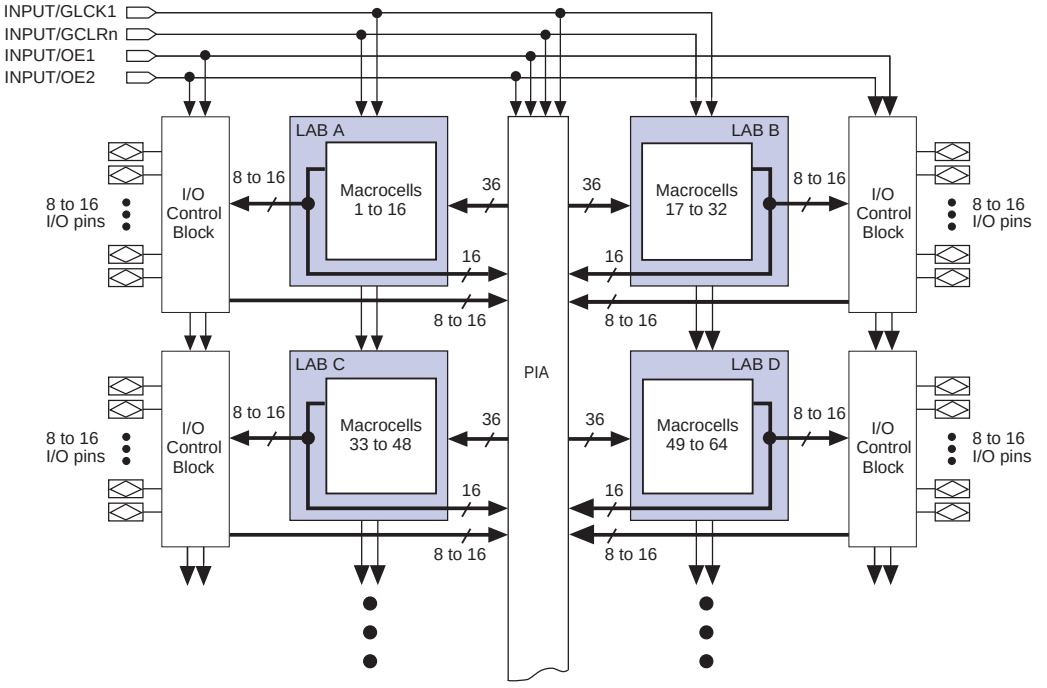
(1) When the JTAG interface in MAX 7000S devices is used for either boundary-scan testing or for ISP, four I/O pins become JTAG pins.

(2) Perform a complete thermal analysis before committing a design to this device package. For more information, see the *Operating Requirements for Altera Devices Data Sheet*.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of EPM7032, EPM7064, and EPM7096 devices.

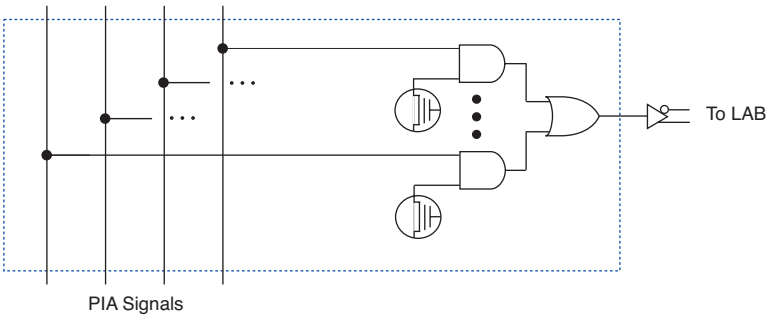
Figure 1. EPM7032, EPM7064 & EPM7096 Device Block Diagram



Programmable Interconnect Array

Logic is routed between LABs via the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



While the routing delays of channel-based routing schemes in masked or FPGAs are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 8 shows the I/O control block for the MAX 7000 family. The I/O control block of EPM7032, EPM7064, and EPM7096 devices has two global output enable signals that are driven by two dedicated active-low output enable pins (OE1 and OE2). The I/O control block of MAX 7000E and MAX 7000S devices has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

Programming a Single MAX 7000S Device

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where: t_{PROG} = Programming time
t_{PPULSE} = Sum of the fixed times to erase, program, and verify the EEPROM cells
$Cycle_{PTCK}$ = Number of TCK cycles to program a device
f_{TCK} = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where: t_{VER} = Verify time
t_{VPULSE} = Sum of the fixed times to verify the EEPROM cells
$Cycle_{VTCK}$ = Number of TCK cycles to verify a device

Table 15. MAX 7000 5.0-V Device DC Operating Conditions *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5 *(8)*	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(10)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(10)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.0 V *(10)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(11)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(11)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V*(11)*		0.2	V
I_I	Leakage current of dedicated input pins	V_I = –0.5 to 5.5 V *(11)*	–10	10	µA
I_{OZ}	I/O pin tri-state output off-state current	V_I = –0.5 to 5.5 V *(11)*, *(12)*	–40	40	µA

Table 16. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 17. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

Table 18. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (13)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Table 21. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t_{SU}	Global clock setup time		7.0		8.0		ns
t_{H}	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t_{CH}	Global clock high time		4.0		4.0		ns
t_{CL}	Global clock low time		4.0		4.0		ns
t_{ASU}	Array clock setup time		2.0		3.0		ns
t_{AH}	Array clock hold time		3.0		3.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t_{ACH}	Array clock high time		4.0		4.0		ns
t_{ACL}	Array clock low time		4.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	4.0		4.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		ns
t_{CNT}	Minimum global clock period			10.0		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	100.0		100.0		MHz
t_{ACNT}	Minimum array clock period			10.0		10.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	100.0		100.0		MHz
f_{MAX}	Maximum clock frequency	*(6)*	125.0		125.0		MHz

Table 22. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.5		1.0	ns
t_{IO}	I/O input pad and buffer delay			0.5		1.0	ns
t_{FIN}	Fast input delay	*(2)*		1.0		1.0	ns
t_{SEXP}	Shared expander delay			5.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	*(2)*		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		1.5		2.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.0		2.5	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		5.5		6.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		5.0		5.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		5.0	ns
t_{SU}	Register setup time		2.0		3.0		ns
t_{H}	Register hold time		3.0		3.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	3.0		3.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.5		0.5		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			5.0		5.0	ns
t_{GLOB}	Global control delay			1.0		1.0	ns
t_{PRE}	Register preset time			3.0		3.0	ns
t_{CLR}	Register clear time			3.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	*(8)*		11.0		11.0	ns

Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t_{FIN}	Fast input delay	*(2)*		1.0		1.0	ns
t_{SEXP}	Shared expander delay			7.0		7.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0	ns
t_{LAD}	Logic array delay			7.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	*(2)*		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		1.0		3.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		2.0		4.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		5.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		7.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0	ns
t_{SU}	Register setup time		1.0		4.0		ns
t_{H}	Register hold time		6.0		4.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	4.0		2.0		ns
t_{FH}	Register hold time of fast input	*(2)*	0.0		2.0		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			7.0		5.0	ns
t_{GLOB}	Global control delay			2.0		0.0	ns
t_{PRE}	Register preset time			4.0		3.0	ns
t_{CLR}	Register clear time			4.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	*(8)*		12.0		12.0	ns

Table 25. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15.0		15.0		20.0	ns
t_{SU}	Global clock setup time		11.0		11.0		12.0		ns
t_{H}	Global clock hold time		0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	*(2)*	3.0		–		5.0		ns
t_{FH}	Global clock hold time of fast input	*(2)*	0.0		–		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8.0		8.0		12.0	ns
t_{CH}	Global clock high time		5.0		6.0		6.0		ns
t_{CL}	Global clock low time		5.0		6.0		6.0		ns
t_{ASU}	Array clock setup time		4.0		4.0		5.0		ns
t_{AH}	Array clock hold time		4.0		4.0		5.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15.0		15.0		20.0	ns
t_{ACH}	Array clock high time		6.0		6.5		8.0		ns
t_{ACL}	Array clock low time		6.0		6.5		8.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	*(3)*	6.0		6.5		8.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(4)*	1.0		1.0		1.0		ns
t_{CNT}	Minimum global clock period			13.0		13.0		16.0	ns
f_{CNT}	Maximum internal global clock frequency	*(5)*	76.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13.0		13.0		16.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(5)*	76.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*(6)*	100		83.3		83.3		MHz

Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			2.0		2.0		3.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		3.0	ns
t_{FIN}	Fast input delay	*(2)*		2.0		–		4.0	ns
t_{SEXP}	Shared expander delay			8.0		10.0		9.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0		2.0	ns
t_{LAD}	Logic array delay			6.0		6.0		8.0	ns
t_{LAC}	Logic control array delay			6.0		6.0		8.0	ns
t_{IOE}	Internal output enable delay	*(2)*		3.0		–		4.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		5.0		–		6.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		8.0		–		9.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF		6.0		6.0		10.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *(7)*		7.0		–		11.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *(2)*		10.0		–		14.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		6.0		10.0	ns
t_{SU}	Register setup time		4.0		4.0		4.0		ns
t_{H}	Register hold time		4.0		4.0		5.0		ns
t_{FSU}	Register setup time of fast input	*(2)*	2.0		–		4.0		ns
t_{FH}	Register hold time of fast input	*(2)*	2.0		–		3.0		ns
t_{RD}	Register delay			1.0		1.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		1.0	ns
t_{IC}	Array clock delay			6.0		6.0		8.0	ns
t_{EN}	Register enable time			6.0		6.0		8.0	ns
t_{GLOB}	Global control delay			1.0		1.0		3.0	ns
t_{PRE}	Register preset time			4.0		4.0		4.0	ns
t_{CLR}	Register clear time			4.0		4.0		4.0	ns
t_{PIA}	PIA delay			2.0		2.0		3.0	ns
t_{LPA}	Low-power adder	*(8)*		13.0		15.0		15.0	ns

Table 28. EPM7032S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PIA}	PIA delay	*(7)*		1.1		1.1		1.4		1.0	ns
t_{LPA}	Low-power adder	*(8)*		12.0		10.0		10.0		11.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.
(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

Tables 29 and 30 show the EPM7064S AC operating conditions.

Table 29. EPM7064S External Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$\mathbf{t_{PD1}}$	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
$\mathbf{t_{PD2}}$	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
$\mathbf{t_{SU}}$	Global clock setup time		2.9		3.6		6.0		7.0		ns
$\mathbf{t_{H}}$	Global clock hold time		0.0		0.0		0.0		0.0		ns
$\mathbf{t_{FSU}}$	Global clock setup time of fast input		2.5		2.5		3.0		3.0		ns
$\mathbf{t_{FH}}$	Global clock hold time of fast input		0.0		0.0		0.5		0.5		ns
$\mathbf{t_{CO1}}$	Global clock to output delay	C1 = 35 pF		3.2		4.0		4.5		5.0	ns
$\mathbf{t_{CH}}$	Global clock high time		2.0		2.5		3.0		4.0		ns
$\mathbf{t_{CL}}$	Global clock low time		2.0		2.5		3.0		4.0		ns
$\mathbf{t_{ASU}}$	Array clock setup time		0.7		0.9		3.0		2.0		ns
$\mathbf{t_{AH}}$	Array clock hold time		1.8		2.1		2.0		3.0		ns

Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_H	Register hold time		1.7		3.0		4.0		ns
t_{FSU}	Register setup time of fast input		2.3		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.7		0.5		1.0		ns
t_{RD}	Register delay			1.4		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.2		2.0		1.0	ns
t_{IC}	Array clock delay			3.2		5.0		6.0	ns
t_{EN}	Register enable time			3.1		5.0		6.0	ns
t_{GLOB}	Global control delay			2.5		1.0		1.0	ns
t_{PRE}	Register preset time			2.7		3.0		4.0	ns
t_{CLR}	Register clear time			2.7		3.0		4.0	ns
t_{PIA}	PIA delay	*(7)*		2.4		1.0		2.0	ns
t_{LPA}	Low-power adder	*(8)*		10.0		11.0		13.0	ns

Notes to tables:

(1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.

(2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.

(3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.

(4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.

(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$ for commercial and industrial use.

(7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.

(8) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, $\mathbf{t_{ACL}}$, and $\mathbf{t_{CPPW}}$ parameters for macrocells running in the low-power mode.

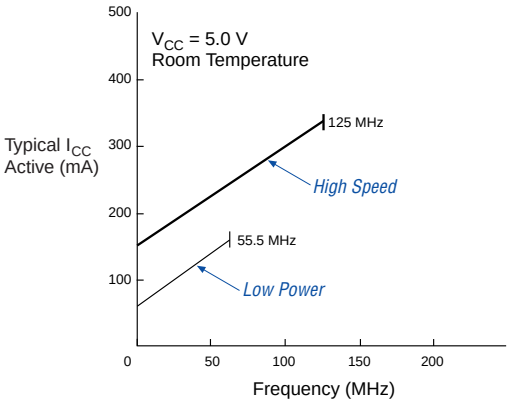
Table 39. MAX 7000 I_{CC} Equation Constants

Device	A	B	C
EPM7032	1.87	0.52	0.144
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S	0.93	0.40	0.040
EPM7064S	0.93	0.40	0.040
EPM7128S	0.93	0.40	0.040
EPM7160S	0.93	0.40	0.040
EPM7192S	0.93	0.40	0.040
EPM7256S	0.93	0.40	0.040

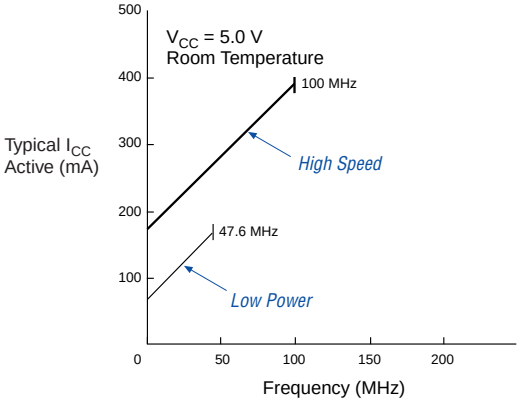
This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 14. I_{CC} vs. Frequency for MAX 7000 Devices (Part 2 of 2)

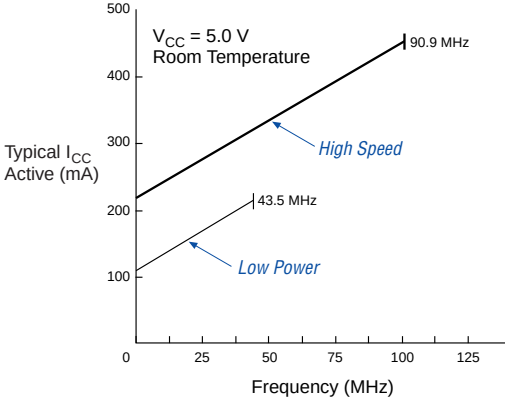
EPM7128E



EPM7160E



EPM7192E



EPM7256E

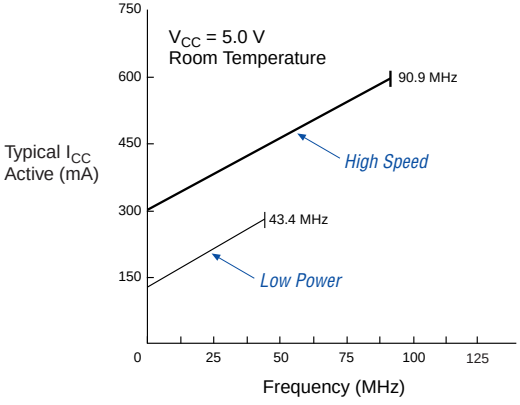


Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 1 of 2)

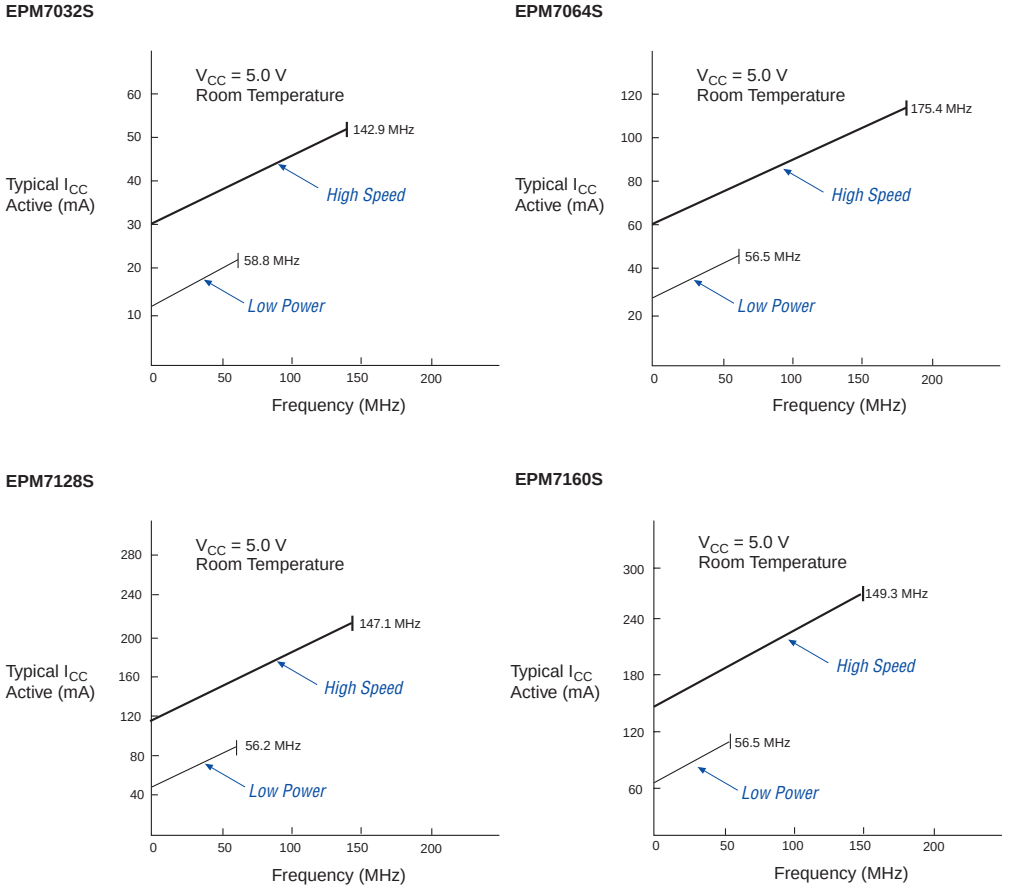
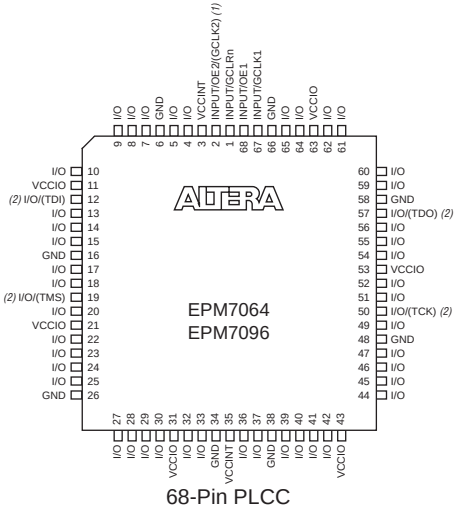


Figure 17. 68-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

(1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.

(2) JTAG ports are available in MAX 7000S devices only.

Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added Tables 6 through 8.
- Added "Programming Sequence" section on page 17 and "Programming Times" section on page 18.

Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on page 16.

Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added *Note (5)* on page 28.

Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the "Open-Drain Output Option (MAX 7000S Devices Only)" section on page 20.

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