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### Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

### Applications of Embedded - CPLDs

#### Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/epm7256src208-10">https://www.e-xfl.com/product-detail/intel/epm7256src208-10</a>

- Additional design entry and simulation support provided by EDIF 2.0.0 and 3.0.0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, and VeriBest
- Programming support
  - Altera's Master Programming Unit (MPU) and programming hardware from third-party manufacturers program all MAX 7000 devices
  - The BitBlaster™ serial download cable, ByteBlasterMV™ parallel port download cable, and MasterBlaster™ serial/universal serial bus (USB) download cable program MAX 7000S devices

## General Description

The MAX 7000 family of high-density, high-performance PLDs is based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000 family provides 600 to 5,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 175.4 MHz. MAX 7000S devices in the -5, -6, -7, and -10 speed grades as well as MAX 7000 and MAX 7000E devices in -5, -6, -7, -10P, and -12P speed grades comply with the PCI Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 2.2*. See [Table 3](#) for available speed grades.

**Table 3. MAX 7000 Speed Grades**

Device	Speed Grade									
	-5	-6	-7	-10P	-10	-12P	-12	-15	-15T	-20
EPM7032		✓	✓		✓		✓	✓	✓	
EPM7032S	✓	✓	✓		✓					
EPM7064		✓	✓		✓		✓	✓		
EPM7064S	✓	✓	✓		✓					
EPM7096			✓		✓		✓	✓		
EPM7128E			✓	✓	✓		✓	✓		✓
EPM7128S		✓	✓		✓			✓		
EPM7160E				✓	✓		✓	✓		✓
EPM7160S		✓	✓		✓			✓		
EPM7192E						✓	✓	✓		✓
EPM7192S			✓		✓			✓		
EPM7256E						✓	✓	✓		✓
EPM7256S			✓		✓			✓		

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E and MAX 7000S devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The software provides EDIF 2.0.0 and 3.0.0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The software runs on Windows-based PCs, as well as Sun SPARCstation, and HP 9000 Series 700/800 workstations.



For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* and the *Quartus Programmable Logic Development System & Software Data Sheet*.

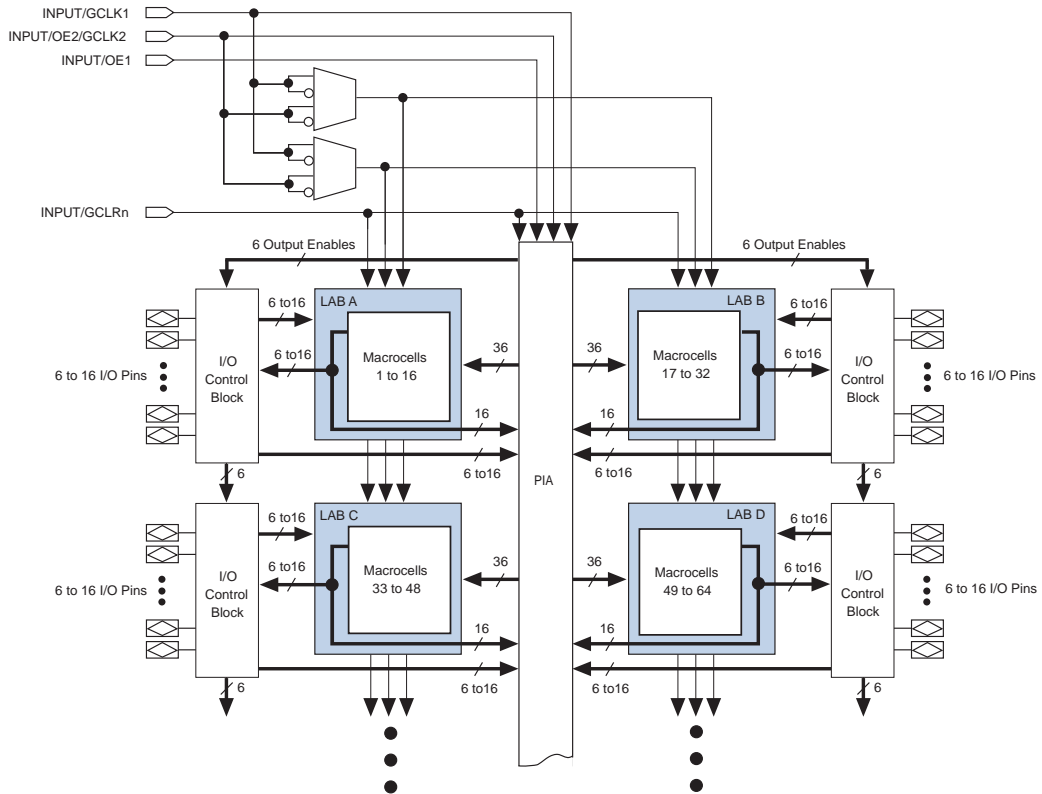
## Functional Description

The MAX 7000 architecture includes the following elements:

- Logic array blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

Figure 2 shows the architecture of MAX 7000E and MAX 7000S devices.

**Figure 2. MAX 7000E & MAX 7000S Device Block Diagram**

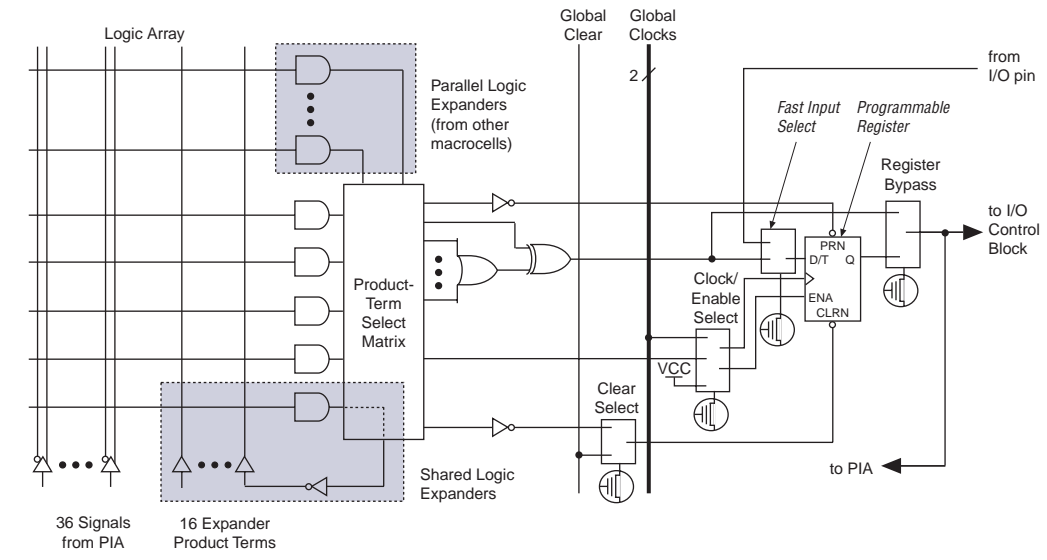


## Logic Array Blocks

The MAX 7000 device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

Figure 4 shows a MAX 7000E and MAX 7000S device macrocell.

**Figure 4. MAX 7000E & MAX 7000S Device Macrocell**



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register clear, preset, clock, and clock enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The Altera development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the Altera development software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

## Programming Times

The time required to implement each of the six programming stages can be broken into the following two elements:

- A pulse time to erase, program, or read the EEPROM cells.
- A shifting time based on the test clock (TCK) frequency and the number of TCK cycles to shift instructions, address, and data into the device.

By combining the pulse and shift times for each of the programming stages, the program or verify time can be derived as a function of the TCK frequency, the number of devices, and specific target device(s). Because different ISP-capable devices have a different number of EEPROM cells, both the total fixed and total variable times are unique for a single device.

### *Programming a Single MAX 7000S Device*

The time required to program a single MAX 7000S device in-system can be calculated from the following formula:

$$t_{PROG} = t_{PPULSE} + \frac{Cycle_{PTCK}}{f_{TCK}}$$

where:  $t_{PROG}$  = Programming time  
 $t_{PPULSE}$  = Sum of the fixed times to erase, program, and verify the EEPROM cells  
 $Cycle_{PTCK}$  = Number of TCK cycles to program a device  
 $f_{TCK}$  = TCK frequency

The ISP times for a stand-alone verification of a single MAX 7000S device can be calculated from the following formula:

$$t_{VER} = t_{VPULSE} + \frac{Cycle_{VTCK}}{f_{TCK}}$$

where:  $t_{VER}$  = Verify time  
 $t_{VPULSE}$  = Sum of the fixed times to verify the EEPROM cells  
 $Cycle_{VTCK}$  = Number of TCK cycles to verify a device

The programming times described in [Tables 6 through 8](#) are associated with the worst-case method using the enhanced ISP algorithm.

**Table 6. MAX 7000S  $t_{PULSE}$  &  $Cycle_{TCK}$  Values**

Device	Programming		Stand-Alone Verification	
	$t_{PULSE}$ (s)	$Cycle_{PTCK}$	$t_{VPULSE}$ (s)	$Cycle_{VTCK}$
EPM7032S	4.02	342,000	0.03	200,000
EPM7064S	4.50	504,000	0.03	308,000
EPM7128S	5.11	832,000	0.03	528,000
EPM7160S	5.35	1,001,000	0.03	640,000
EPM7192S	5.71	1,192,000	0.03	764,000
EPM7256S	6.43	1,603,000	0.03	1,024,000

[Tables 7](#) and [8](#) show the in-system programming and stand alone verification times for several common test clock frequencies.

**Table 7. MAX 7000S In-System Programming Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	4.06	4.09	4.19	4.36	4.71	5.73	7.44	10.86	s
EPM7064S	4.55	4.60	4.76	5.01	5.51	7.02	9.54	14.58	s
EPM7128S	5.19	5.27	5.52	5.94	6.77	9.27	13.43	21.75	s
EPM7160S	5.45	5.55	5.85	6.35	7.35	10.35	15.36	25.37	s
EPM7192S	5.83	5.95	6.30	6.90	8.09	11.67	17.63	29.55	s
EPM7256S	6.59	6.75	7.23	8.03	9.64	14.45	22.46	38.49	s

**Table 8. MAX 7000S Stand-Alone Verification Times for Different Test Clock Frequencies**

Device	$f_{TCK}$								Units
	10 MHz	5 MHz	2 MHz	1 MHz	500 kHz	200 kHz	100 kHz	50 kHz	
EPM7032S	0.05	0.07	0.13	0.23	0.43	1.03	2.03	4.03	s
EPM7064S	0.06	0.09	0.18	0.34	0.64	1.57	3.11	6.19	s
EPM7128S	0.08	0.14	0.29	0.56	1.09	2.67	5.31	10.59	s
EPM7160S	0.09	0.16	0.35	0.67	1.31	3.23	6.43	12.83	s
EPM7192S	0.11	0.18	0.41	0.79	1.56	3.85	7.67	15.31	s
EPM7256S	0.13	0.24	0.54	1.06	2.08	5.15	10.27	20.51	s

## Design Security

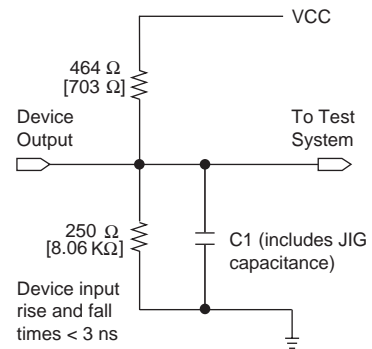
All MAX 7000 devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

## Generic Testing

Each MAX 7000 device is functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in [Figure 10](#). Test patterns can be used and then erased during early stages of the production flow.

**Figure 10. MAX 7000 AC Test Conditions**

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V devices and outputs. Numbers without brackets are for 3.3-V devices and outputs.*



## QFP Carrier & Development Socket

MAX 7000 and MAX 7000E devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.



For detailed information and carrier dimensions, refer to the [QFP Carrier & Development Socket Data Sheet](#).



MAX 7000S devices are not shipped in carriers.



## Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

**Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings** *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	Supply voltage	With respect to ground (2)	–2.0	7.0	V
$V_I$	DC input voltage		–2.0	7.0	V
$I_{OUT}$	DC output current, per pin		–25	25	mA
$T_{STG}$	Storage temperature	No bias	–65	150	°C
$T_{AMB}$	Ambient temperature	Under bias	–65	135	°C
$T_J$	Junction temperature	Ceramic packages, under bias		150	°C
		PQFP and RQFP packages, under bias		135	°C

**Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CCINT}$	Supply voltage for internal logic and input buffers	(3), (4), (5)	4.75 (4.50)	5.25 (5.50)	V
$V_{CCIO}$	Supply voltage for output drivers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	(3), (4), (6)	3.00 (3.00)	3.60 (3.60)	V
$V_{CCISP}$	Supply voltage during ISP	(7)	4.75	5.25	V
$V_I$	Input voltage		–0.5 (8)	$V_{CCINT} + 0.5$	V
$V_O$	Output voltage		0	$V_{CCIO}$	V
$T_A$	Ambient temperature	For commercial use	0	70	°C
		For industrial use	–40	85	°C
$T_J$	Junction temperature	For commercial use	0	90	°C
		For industrial use	–40	105	°C
$t_R$	Input rise time			40	ns
$t_F$	Input fall time			40	ns

**Table 26. MAX 7000 & MAX 7000E Internal Timing Parameters** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-15		-15T		-20		
			Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			2.0		2.0		3.0	ns
$t_{IO}$	I/O input pad and buffer delay			2.0		2.0		3.0	ns
$t_{FIN}$	Fast input delay	(2)		2.0		—		4.0	ns
$t_{SEXP}$	Shared expander delay			8.0		10.0		9.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.0		2.0	ns
$t_{LAD}$	Logic array delay			6.0		6.0		8.0	ns
$t_{LAC}$	Logic control array delay			6.0		6.0		8.0	ns
$t_{IOE}$	Internal output enable delay	(2)		3.0		—		4.0	ns
$t_{OD1}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		4.0		4.0		5.0	ns
$t_{OD2}$	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		5.0		—		6.0	ns
$t_{OD3}$	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		8.0		—		9.0	ns
$t_{ZX1}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0\text{ V}$	$C1 = 35\text{ pF}$		6.0		6.0		10.0	ns
$t_{ZX2}$	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3\text{ V}$	$C1 = 35\text{ pF}$ (7)		7.0		—		11.0	ns
$t_{ZX3}$	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0\text{ V}$ or $3.3\text{ V}$	$C1 = 35\text{ pF}$ (2)		10.0		—		14.0	ns
$t_{XZ}$	Output buffer disable delay	$C1 = 5\text{ pF}$		6.0		6.0		10.0	ns
$t_{SU}$	Register setup time		4.0		4.0		4.0		ns
$t_H$	Register hold time		4.0		4.0		5.0		ns
$t_{FSU}$	Register setup time of fast input	(2)	2.0		—		4.0		ns
$t_{FH}$	Register hold time of fast input	(2)	2.0		—		3.0		ns
$t_{RD}$	Register delay			1.0		1.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.0		1.0	ns
$t_{IC}$	Array clock delay			6.0		6.0		8.0	ns
$t_{EN}$	Register enable time			6.0		6.0		8.0	ns
$t_{GLOB}$	Global control delay			1.0		1.0		3.0	ns
$t_{PRE}$	Register preset time			4.0		4.0		4.0	ns
$t_{CLR}$	Register clear time			4.0		4.0		4.0	ns
$t_{PIA}$	PIA delay			2.0		2.0		3.0	ns
$t_{LPA}$	Low-power adder	(8)		13.0		15.0		15.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This parameter applies to MAX 7000E devices only.
- (3) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (4) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (5) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (6) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (7) Operating conditions:  $V_{CCIO} = 3.3 \text{ V} \pm 10\%$  for commercial and industrial use.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$ , and  $t_{CPPW}$  parameters for macrocells running in the low-power mode.

Tables 27 and 28 show the EPM7032S AC operating conditions.

**Table 27. EPM7032S External Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		5.0		6.0		7.5		10.0	ns
t <sub>SU</sub>	Global clock setup time		2.9		4.0		5.0		7.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		2.5		2.5		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.0		0.0		0.5		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		3.2		3.5		4.3		5.0	ns
t <sub>CH</sub>	Global clock high time		2.0		2.5		3.0		4.0		ns
t <sub>CL</sub>	Global clock low time		2.0		2.5		3.0		4.0		ns
t <sub>ASU</sub>	Array clock setup time		0.7		0.9		1.1		2.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.1		2.7		3.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.6		8.2		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.0		8.6		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		142.9		116.3		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.0		8.6		10.0	ns

**Table 29. EPM7064S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t <sub>ACH</sub>	Array clock high time		2.5		2.5		3.0		4.0		ns
t <sub>ACL</sub>	Array clock low time		2.5		2.5		3.0		4.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t <sub>ACNT</sub>	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

**Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
$t_{FIN}$	Fast input delay			2.2		2.6		1.0		1.0	ns
$t_{SEXP}$	Shared expander delay			3.1		3.8		4.0		5.0	ns
$t_{PEXP}$	Parallel expander delay			0.9		1.1		0.8		0.8	ns
$t_{LAD}$	Logic array delay			2.6		3.2		3.0		5.0	ns
$t_{LAC}$	Logic control array delay			2.5		3.2		3.0		5.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.8		2.0		2.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
$t_{SU}$	Register setup time		0.8		1.0		3.0		2.0		ns
$t_H$	Register hold time		1.7		2.0		2.0		3.0		ns

Tables 31 and 32 show the EPM7128S AC operating conditions.

Table 31. EPM7128S External Timing Parameters      Note (1)											
Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>PD1</sub>	Input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>PD2</sub>	I/O input to non-registered output	C1 = 35 pF		6.0		7.5		10.0		15.0	ns
t <sub>SU</sub>	Global clock setup time		3.4		6.0		7.0		11.0		ns
t <sub>H</sub>	Global clock hold time		0.0		0.0		0.0		0.0		ns
t <sub>FSU</sub>	Global clock setup time of fast input		2.5		3.0		3.0		3.0		ns
t <sub>FH</sub>	Global clock hold time of fast input		0.0		0.5		0.5		0.0		ns
t <sub>CO1</sub>	Global clock to output delay	C1 = 35 pF		4.0		4.5		5.0		8.0	ns
t <sub>CH</sub>	Global clock high time		3.0		3.0		4.0		5.0		ns
t <sub>CL</sub>	Global clock low time		3.0		3.0		4.0		5.0		ns
t <sub>ASU</sub>	Array clock setup time		0.9		3.0		2.0		4.0		ns
t <sub>AH</sub>	Array clock hold time		1.8		2.0		5.0		4.0		ns
t <sub>ACO1</sub>	Array clock to output delay	C1 = 35 pF		6.5		7.5		10.0		15.0	ns
t <sub>ACH</sub>	Array clock high time		3.0		3.0		4.0		6.0		ns
t <sub>ACL</sub>	Array clock low time		3.0		3.0		4.0		6.0		ns
t <sub>CPPW</sub>	Minimum pulse width for clear and preset	(2)	3.0		3.0		4.0		6.0		ns
t <sub>ODH</sub>	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t <sub>CNT</sub>	Minimum global clock period			6.8		8.0		10.0		13.0	ns
f <sub>CNT</sub>	Maximum internal global clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
t <sub>ACNT</sub>	Minimum array clock period			6.8		8.0		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	147.1		125.0		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

**Table 33. EPM7160S External Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>ACNT</sub>	Minimum array clock period			6.7		8.2		10.0		13.0	ns
f <sub>ACNT</sub>	Maximum internal array clock frequency	(4)	149.3		122.0		100.0		76.9		MHz
f <sub>MAX</sub>	Maximum clock frequency	(5)	166.7		166.7		125.0		100.0		MHz

**Table 34. EPM7160S Internal Timing Parameters (Part 1 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{IO}$	I/O input pad and buffer delay			0.2		0.3		0.5		2.0	ns
$t_{FIN}$	Fast input delay			2.6		3.2		1.0		2.0	ns
$t_{SEXP}$	Shared expander delay			3.6		4.3		5.0		8.0	ns
$t_{PEXP}$	Parallel expander delay			1.0		1.3		0.8		1.0	ns
$t_{LAD}$	Logic array delay			2.8		3.4		5.0		6.0	ns
$t_{LAC}$	Logic control array delay			2.8		3.4		5.0		6.0	ns
$t_{IOE}$	Internal output enable delay			0.7		0.9		2.0		3.0	ns
$t_{OD1}$	Output buffer and pad delay	C1 = 35 pF		0.4		0.5		1.5		4.0	ns
$t_{OD2}$	Output buffer and pad delay	C1 = 35 pF (6)		0.9		1.0		2.0		5.0	ns
$t_{OD3}$	Output buffer and pad delay	C1 = 35 pF		5.4		5.5		5.5		8.0	ns
$t_{ZX1}$	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
$t_{ZX2}$	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
$t_{ZX3}$	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
$t_{XZ}$	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
$t_{SU}$	Register setup time		1.0		1.2		2.0		4.0		ns
$t_H$	Register hold time		1.6		2.0		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		1.9		2.2		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.6		0.8		0.5		1.0		ns
$t_{RD}$	Register delay			1.3		1.6		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.0		1.3		2.0		1.0	ns
$t_{IC}$	Array clock delay			2.9		3.5		5.0		6.0	ns
$t_{EN}$	Register enable time			2.8		3.4		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.0		2.4		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.4		3.0		3.0		4.0	ns

**Table 36. EPM7192S Internal Timing Parameters (Part 2 of 2)** *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
$t_H$	Register hold time		1.7		3.0		4.0		ns
$t_{FSU}$	Register setup time of fast input		2.3		3.0		2.0		ns
$t_{FH}$	Register hold time of fast input		0.7		0.5		1.0		ns
$t_{RD}$	Register delay			1.4		2.0		1.0	ns
$t_{COMB}$	Combinatorial delay			1.2		2.0		1.0	ns
$t_{IC}$	Array clock delay			3.2		5.0		6.0	ns
$t_{EN}$	Register enable time			3.1		5.0		6.0	ns
$t_{GLOB}$	Global control delay			2.5		1.0		1.0	ns
$t_{PRE}$	Register preset time			2.7		3.0		4.0	ns
$t_{CLR}$	Register clear time			2.7		3.0		4.0	ns
$t_{PIA}$	PIA delay	(7)		2.4		1.0		2.0	ns
$t_{LPA}$	Low-power adder	(8)		10.0		11.0		13.0	ns

**Notes to tables:**

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The  $t_{LPA}$  parameter must be added to this minimum width if the clear or reset signal incorporates the  $t_{LAD}$  parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The  $f_{MAX}$  values represent the highest frequency for pipelined data.
- (6) Operating conditions:  $V_{CCIO} = 3.3\text{ V} \pm 10\%$  for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The  $t_{LPA}$  parameter must be added to the  $t_{LAD}$ ,  $t_{LAC}$ ,  $t_{IC}$ ,  $t_{EN}$ ,  $t_{SEXP}$ ,  $t_{ACL}$  and  $t_{CPW}$  parameters for macrocells running in the low-power mode.

**Table 39. MAX 7000  $I_{CC}$  Equation Constants**

Device	A	B	C
EPM7032	1.87	0.52	0.144
EPM7064	1.63	0.74	0.144
EPM7096	1.63	0.74	0.144
EPM7128E	1.17	0.54	0.096
EPM7160E	1.17	0.54	0.096
EPM7192E	1.17	0.54	0.096
EPM7256E	1.17	0.54	0.096
EPM7032S	0.93	0.40	0.040
EPM7064S	0.93	0.40	0.040
EPM7128S	0.93	0.40	0.040
EPM7160S	0.93	0.40	0.040
EPM7192S	0.93	0.40	0.040
EPM7256S	0.93	0.40	0.040

This calculation provides an  $I_{CC}$  estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual  $I_{CC}$  values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Figure 14.  $I_{CC}$  vs. Frequency for MAX 7000 Devices (Part 2 of 2)

EPM7128E



EPM7160E



EPM7192E



EPM7256E



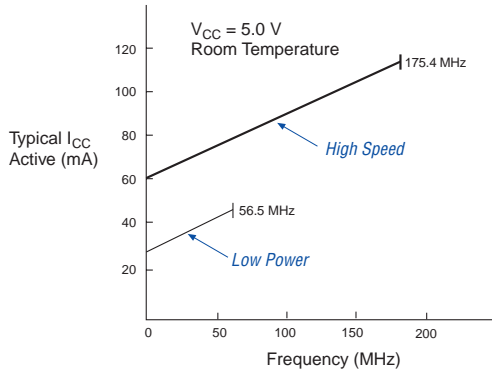
Figure 15 shows typical supply current versus frequency for MAX 7000S devices.

**Figure 15.  $I_{CC}$  vs. Frequency for MAX 7000S Devices (Part 1 of 2)**

**EPM7032S**



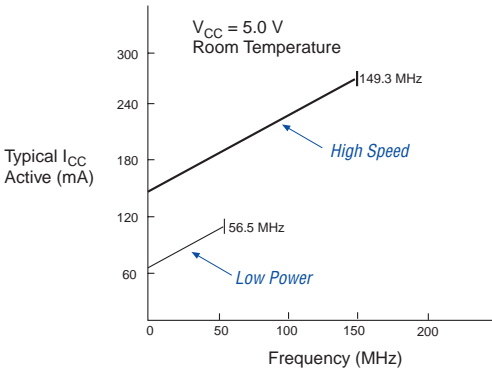
**EPM7064S**



**EPM7128S**

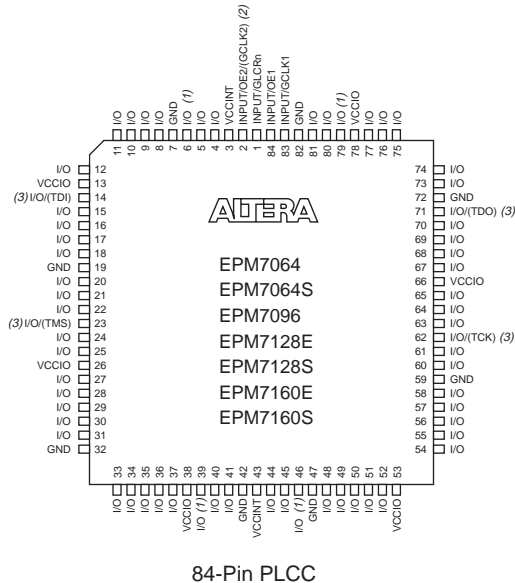


**EPM7160S**



**Figure 18. 84-Pin Package Pin-Out Diagram**

Package outline not drawn to scale.

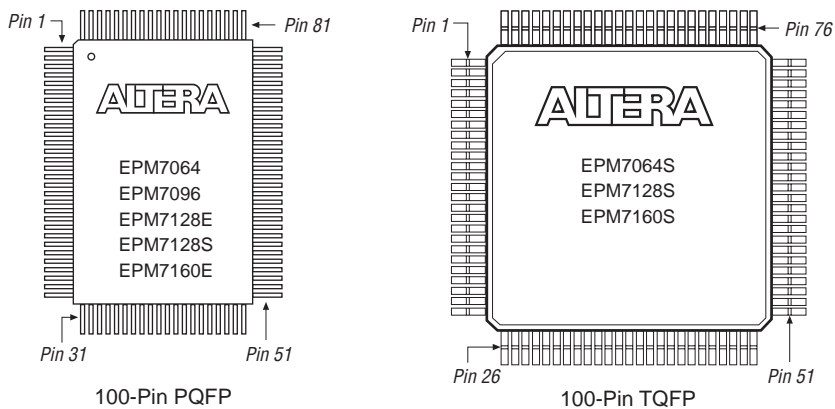


**Notes:**

- (1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096, EPM7160E, and EPM7160S devices.
- (2) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (3) JTAG ports are available in MAX 7000S devices only.

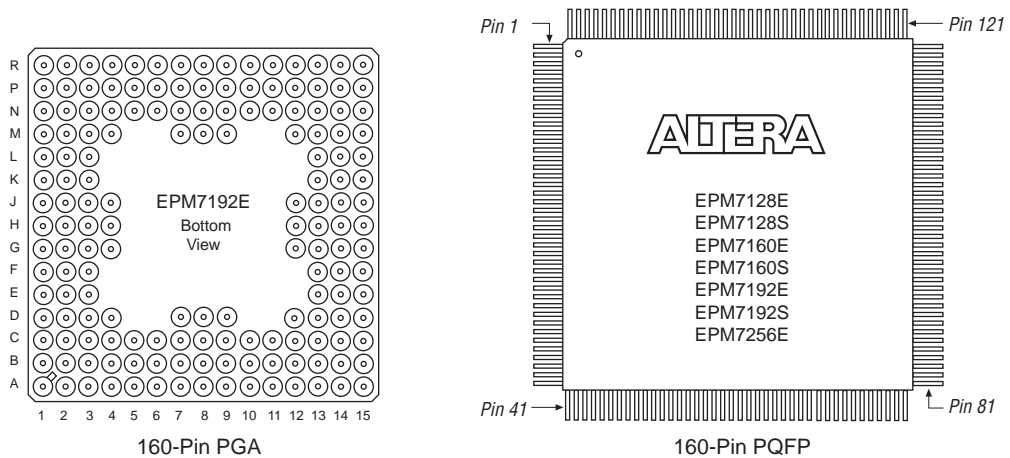
**Figure 19. 100-Pin Package Pin-Out Diagram**

*Package outline not drawn to scale.*



**Figure 20. 160-Pin Package Pin-Out Diagram**

*Package outline not drawn to scale.*





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