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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	16
Number of Macrocells	256
Number of Gates	5000
Number of I/O	164
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP Exposed Pad
Supplier Device Package	208-RQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm7256src208-7es

The MAX 7000E devices—including the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices—have several enhanced features: additional global clocking, additional output enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

In-system programmable MAX 7000 devices—called MAX 7000S devices—include the EPM7032S, EPM7064S, EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices. MAX 7000S devices have the enhanced features of MAX 7000E devices as well as JTAG BST circuitry in devices with 128 or more macrocells, ISP, and an open-drain output option. See [Table 4](#).

Table 4. MAX 7000 Device Features			
Feature	EPM7032 EPM7064 EPM7096	All MAX 7000E Devices	All MAX 7000S Devices
ISP via JTAG interface			✓
JTAG BST circuitry			✓ ⁽¹⁾
Open-drain output option			✓
Fast input registers		✓	✓
Six global output enables		✓	✓
Two global clocks		✓	✓
Slew-rate control		✓	✓
MultiVolt interface ⁽²⁾	✓	✓	✓
Programmable register	✓	✓	✓
Parallel expanders	✓	✓	✓
Shared expanders	✓	✓	✓
Power-saving mode	✓	✓	✓
Security bit	✓	✓	✓
PCI-compliant devices available	✓	✓	✓

Notes:

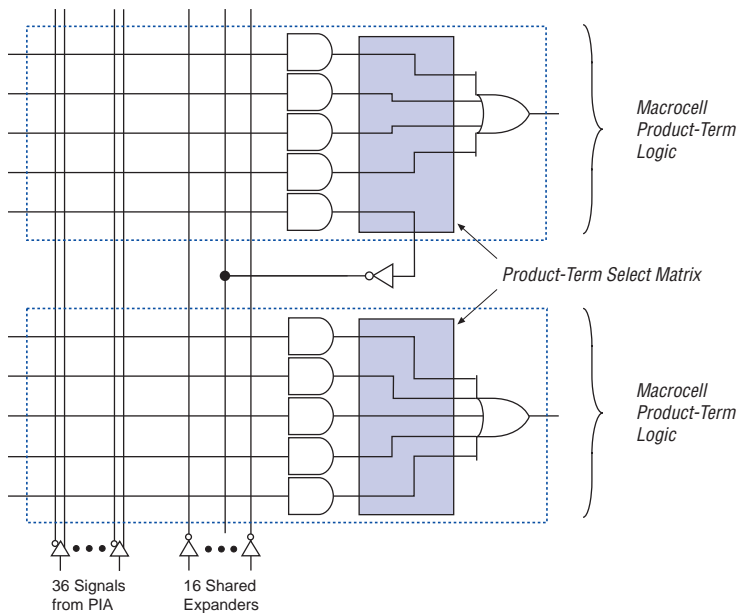
- (1) Available only in EPM7128S, EPM7160S, EPM7192S, and EPM7256S devices only.
- (2) The MultiVolt I/O interface is not available in 44-pin packages.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

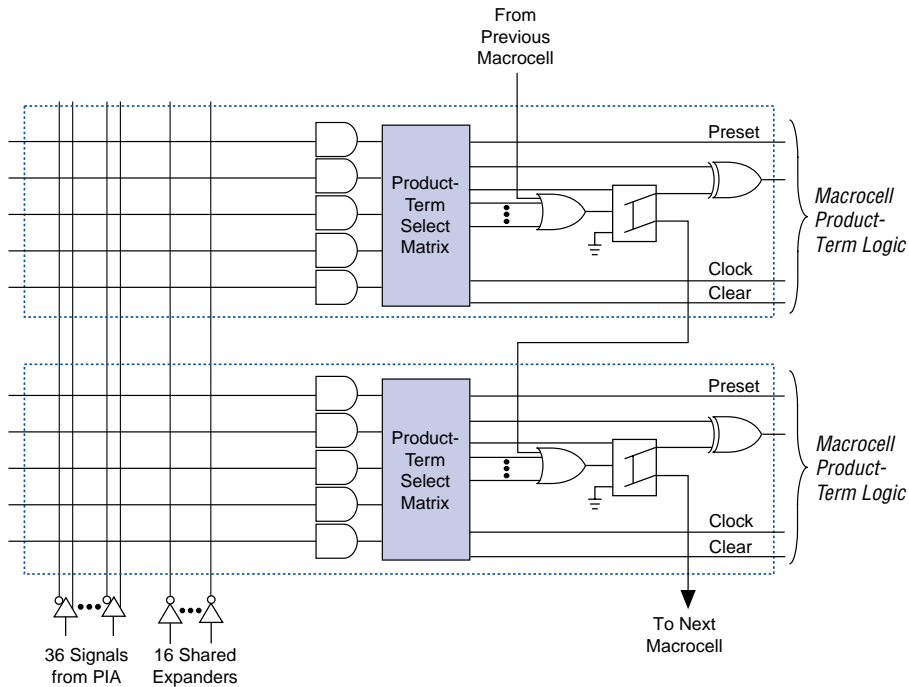
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The compiler can allocate up to three sets of up to five parallel expanders automatically to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 through 8 and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC} , the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000S devices are in-system programmable via an industry-standard 4-pin Joint Test Action Group (JTAG) interface (IEEE Std. 1149.1-1990). ISP allows quick, efficient iterations during design development and debugging cycles. The MAX 7000S architecture internally generates the high programming voltage required to program EEPROM cells, allowing in-system programming with only a single 5.0 V power supply. During in-system programming, the I/O pins are tri-stated and pulled-up to eliminate board conflicts. The pull-up value is nominally 50 k Ω .

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard in-circuit test equipment before they are programmed. MAX 7000S devices can be programmed by downloading the information via in-circuit testers (ICT), embedded processors, or the Altera MasterBlaster, ByteBlasterMV, ByteBlaster, BitBlaster download cables. (The ByteBlaster cable is obsolete and is replaced by the ByteBlasterMV cable, which can program and configure 2.5-V, 3.3-V, and 5.0-V devices.) Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling and allows devices to be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. Because some in-circuit testers cannot support an adaptive algorithm, Altera offers devices tested with a constant algorithm. Devices tested to the constant algorithm have an "F" suffix in the ordering code.

The Jam™ Standard Test and Programming Language (STAPL) can be used to program MAX 7000S devices with in-circuit testers, PCs, or embedded processor.

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (i.e., with the Turbo Bit™ option turned on) or low-power (i.e., with the Turbo Bit option turned off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , and t_{SEXP} , t_{ACL} , and t_{CPPW} parameters.

Output Configuration

MAX 7000 device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

MAX 7000 devices—except 44-pin devices—support the MultiVolt I/O interface feature, which allows MAX 7000 devices to interface with systems that have differing supply voltages. The 5.0-V devices in all packages can be set for 3.3-V or 5.0-V I/O pin operation. These devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCINT pins must always be connected to a 5.0-V power supply. With a 5.0-V VCCINT level, input voltage thresholds are at TTL levels, and are therefore compatible with both 3.3-V and 5.0-V inputs.

The VCCIO pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When VCCIO is connected to a 3.3-V supply, the output high is 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with VCCIO levels lower than 4.75 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1} .

Open-Drain Output Option (MAX 7000S Devices Only)

MAX 7000S devices provide an optional open-drain (functionally equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000 devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. [Table 9](#) describes the JTAG instructions supported by the MAX 7000 family. The pin-out tables (see the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information) show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 9. MAX 7000 JTAG Instructions

JTAG Instruction	Devices	Description
SAMPLE/PRELOAD	EPM7128S EPM7160S EPM7192S EPM7256S	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	EPM7128S EPM7160S EPM7192S EPM7256S	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
ISP Instructions	EPM7032S EPM7064S EPM7128S EPM7160S EPM7192S EPM7256S	These instructions are used when programming MAX 7000S devices via the JTAG ports with the MasterBlaster, ByteBlasterMV, BitBlaster download cable, or using a Jam File (.jam), Jam Byte-Code file (.jbc), or Serial Vector Format file (.svf) via an embedded processor or test equipment.

Operating Conditions

Tables 13 through 18 provide information about absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for 5.0-V MAX 7000 devices.

Table 13. MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground (2)	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Ceramic packages, under bias		150	°C
		PQFP and RQFP packages, under bias		135	°C

Table 14. MAX 7000 5.0-V Device Recommended Operating Conditions

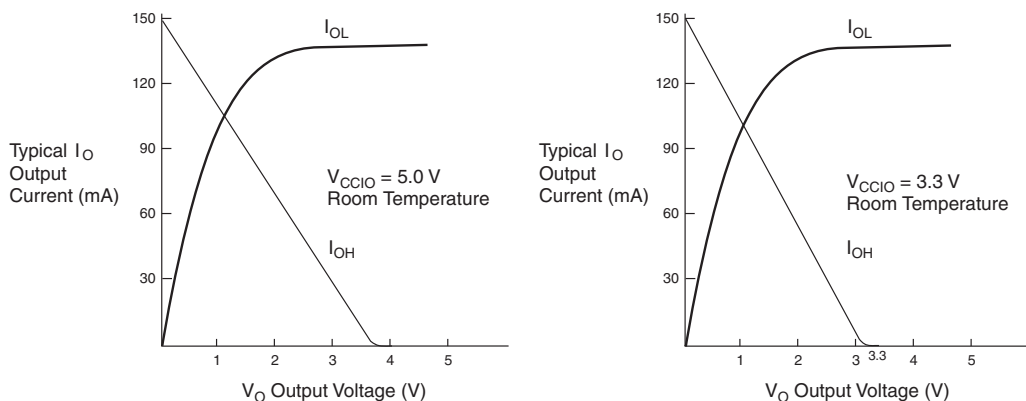
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	(3), (4), (5)	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	(3), (4)	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	(3), (4), (6)	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during ISP	(7)	4.75	5.25	V
V_I	Input voltage		–0.5 (8)	$V_{CCINT} + 0.5$	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	°C
		For industrial use	–40	85	°C
T_J	Junction temperature	For commercial use	0	90	°C
		For industrial use	–40	105	°C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Notes to tables:

- (1) See the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Minimum DC input voltage on I/O pins is -0.5 V and on 4 dedicated input pins is -0.3 V. During transitions, the inputs may undershoot to -2.0 V or overshoot to 7.0 V for input currents less than 100 mA and periods shorter than 20 ns.
- (3) Numbers in parentheses are for industrial-temperature-range devices.
- (4) V_{CC} must rise monotonically.
- (5) The POR time for all 7000S devices does not exceed 300 μ s. The sufficient V_{CCINT} voltage level for POR is 4.5 V. The device is fully initialized within the POR time after V_{CCINT} reaches the sufficient POR voltage level.
- (6) 3.3 -V I/O operation is not available for 44-pin packages.
- (7) The V_{CCISP} parameter applies only to MAX 7000S devices.
- (8) During in-system programming, the minimum DC input voltage is -0.3 V.
- (9) These values are specified under the MAX 7000 recommended operating conditions in [Table 14 on page 26](#).
- (10) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
- (11) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL, PCI, or CMOS output current.
- (12) When the JTAG interface is enabled in MAX 7000S devices, the input leakage current on the JTAG pins is typically -60 μ A.
- (13) Capacitance is measured at 25° C and is sample-tested only. The $\text{OE}1$ pin has a maximum capacitance of 20 pF.

Figure 11 shows the typical output drive characteristics of MAX 7000 devices.

Figure 11. Output Drive Characteristics of 5.0-V MAX 7000 Devices



Timing Model

MAX 7000 device timing can be analyzed with the Altera software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in [Figure 12](#). MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The Altera software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for a device-wide performance evaluation.

Table 21. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-10P)		MAX 7000 (-10) MAX 7000E (-10)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		10.0		10.0	ns
t _{SU}	Global clock setup time		7.0		8.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		5.0		5	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		2.0		3.0		ns
t _{AH}	Array clock hold time		3.0		3.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		10.0		10.0	ns
t _{ACH}	Array clock high time		4.0		4.0		ns
t _{ACL}	Array clock low time		4.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	4.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			10.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	100.0		100.0		MHz
t _{ACNT}	Minimum array clock period			10.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	100.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 23. MAX 7000 & MAX 7000E External Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		12.0		12.0	ns
t _{SU}	Global clock setup time		7.0		10.0		ns
t _H	Global clock hold time		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input	(2)	3.0		3.0		ns
t _{FH}	Global clock hold time of fast input	(2)	0.0		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		6.0		6.0	ns
t _{CH}	Global clock high time		4.0		4.0		ns
t _{CL}	Global clock low time		4.0		4.0		ns
t _{ASU}	Array clock setup time		3.0		4.0		ns
t _{AH}	Array clock hold time		4.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		12.0		12.0	ns
t _{ACH}	Array clock high time		5.0		5.0		ns
t _{ACL}	Array clock low time		5.0		5.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(3)	5.0		5.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t _{CNT}	Minimum global clock period			11.0		11.0	ns
f _{CNT}	Maximum internal global clock frequency	(5)	90.9		90.9		MHz
t _{ACNT}	Minimum array clock period			11.0		11.0	ns
f _{ACNT}	Maximum internal array clock frequency	(5)	90.9		90.9		MHz
f _{MAX}	Maximum clock frequency	(6)	125.0		125.0		MHz

Table 24. MAX 7000 & MAX 7000E Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade				Unit
			MAX 7000E (-12P)		MAX 7000 (-12) MAX 7000E (-12)		
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.0		2.0	ns
t_{IO}	I/O input pad and buffer delay			1.0		2.0	ns
t_{FIN}	Fast input delay	(2)		1.0		1.0	ns
t_{SEXP}	Shared expander delay			7.0		7.0	ns
t_{PEXP}	Parallel expander delay			1.0		1.0	ns
t_{LAD}	Logic array delay			7.0		5.0	ns
t_{LAC}	Logic control array delay			5.0		5.0	ns
t_{IOE}	Internal output enable delay	(2)		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		1.0		3.0	ns
t_{OD2}	Output buffer and pad delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		2.0		4.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		5.0		7.0	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 5.0$ V	$C1 = 35$ pF		6.0		6.0	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off $V_{CCIO} = 3.3$ V	$C1 = 35$ pF (7)		7.0		7.0	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on $V_{CCIO} = 5.0$ V or 3.3 V	$C1 = 35$ pF (2)		10.0		10.0	ns
t_{XZ}	Output buffer disable delay	$C1 = 5$ pF		6.0		6.0	ns
t_{SU}	Register setup time		1.0		4.0		ns
t_H	Register hold time		6.0		4.0		ns
t_{FSU}	Register setup time of fast input	(2)	4.0		2.0		ns
t_{FH}	Register hold time of fast input	(2)	0.0		2.0		ns
t_{RD}	Register delay			2.0		1.0	ns
t_{COMB}	Combinatorial delay			2.0		1.0	ns
t_{IC}	Array clock delay			5.0		5.0	ns
t_{EN}	Register enable time			7.0		5.0	ns
t_{GLOB}	Global control delay			2.0		0.0	ns
t_{PRE}	Register preset time			4.0		3.0	ns
t_{CLR}	Register clear time			4.0		3.0	ns
t_{PIA}	PIA delay			1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		12.0	ns

Table 29. EPM7064S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t _{ACO1}	Array clock to output delay	C1 = 35 pF		5.4		6.7		7.5		10.0	ns
t _{ACH}	Array clock high time		2.5		2.5		3.0		4.0		ns
t _{ACL}	Array clock low time		2.5		2.5		3.0		4.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	2.5		2.5		3.0		4.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			5.7		7.1		8.0		10.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
t _{ACNT}	Minimum array clock period			5.7		7.1		8.0		10.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	175.4		140.8		125.0		100.0		MHz
f _{MAX}	Maximum clock frequency	(5)	250.0		200.0		166.7		125.0		MHz

Table 30. EPM7064S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.2		0.5		0.5	ns
t_{FIN}	Fast input delay			2.2		2.6		1.0		1.0	ns
t_{SEXP}	Shared expander delay			3.1		3.8		4.0		5.0	ns
t_{PEXP}	Parallel expander delay			0.9		1.1		0.8		0.8	ns
t_{LAD}	Logic array delay			2.6		3.2		3.0		5.0	ns
t_{LAC}	Logic control array delay			2.5		3.2		3.0		5.0	ns
t_{IOE}	Internal output enable delay			0.7		0.8		2.0		2.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.2		0.3		2.0		1.5	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.7		0.8		2.5		2.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.2		5.3		7.0		5.5	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		4.0		5.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		4.5		5.5	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0		5.0	ns
t_{SU}	Register setup time		0.8		1.0		3.0		2.0		ns
t_H	Register hold time		1.7		2.0		2.0		3.0		ns

Table 30. EPM7064S Internal Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-5		-6		-7		-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{FSU}	Register setup time of fast input		1.9		1.8		3.0		3.0		ns
t_{FH}	Register hold time of fast input		0.6		0.7		0.5		0.5		ns
t_{RD}	Register delay			1.2		1.6		1.0		2.0	ns
t_{COMB}	Combinatorial delay			0.9		1.0		1.0		2.0	ns
t_{IC}	Array clock delay			2.7		3.3		3.0		5.0	ns
t_{EN}	Register enable time			2.6		3.2		3.0		5.0	ns
t_{GLOB}	Global control delay			1.6		1.9		1.0		1.0	ns
t_{PRE}	Register preset time			2.0		2.4		2.0		3.0	ns
t_{CLR}	Register clear time			2.0		2.4		2.0		3.0	ns
t_{PIA}	PIA delay	(7)		1.1		1.3		1.0		1.0	ns
t_{LPA}	Low-power adder	(8)		12.0		11.0		10.0		11.0	ns

Notes to tables:

- (1) These values are specified under the recommended operating conditions shown in Table 14. See Figure 13 for more information on switching waveforms.
- (2) This minimum pulse width for preset and clear applies for both global clear and array controls. The t_{LPA} parameter must be added to this minimum width if the clear or reset signal incorporates the t_{LAD} parameter into the signal path.
- (3) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
- (4) These parameters are measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
- (5) The f_{MAX} values represent the highest frequency for pipelined data.
- (6) Operating conditions: $V_{CCIO} = 3.3\text{ V} \pm 10\%$ for commercial and industrial use.
- (7) For EPM7064S-5, EPM7064S-6, EPM7128S-6, EPM7160S-6, EPM7160S-7, EPM7192S-7, and EPM7256S-7 devices, these values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
- (8) The t_{LPA} parameter must be added to the t_{LAD} , t_{LAC} , t_{IC} , t_{EN} , t_{SEXP} , t_{ACL} and t_{CPW} parameters for macrocells running in the low-power mode.

Table 32. EPM7128S Internal Timing Parameters *Note (1)*

Symbol	Parameter	Conditions	Speed Grade								Unit
			-6		-7		-10		-15		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.2		0.5		0.5		2.0	ns
t_{FIN}	Fast input delay			2.6		1.0		1.0		2.0	ns
t_{SEXP}	Shared expander delay			3.7		4.0		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.1		0.8		0.8		1.0	ns
t_{LAD}	Logic array delay			3.0		3.0		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.0		3.0		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.7		2.0		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.4		2.0		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		0.9		2.5		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.4		7.0		5.5		8.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.0		3.0		2.0		4.0		ns
t_H	Register hold time		1.7		2.0		5.0		4.0		ns
t_{FSU}	Register setup time of fast input		1.9		3.0		3.0		2.0		ns
t_{FH}	Register hold time of fast input		0.6		0.5		0.5		1.0		ns
t_{RD}	Register delay			1.4		1.0		2.0		1.0	ns
t_{COMB}	Combinatorial delay			1.0		1.0		2.0		1.0	ns
t_{IC}	Array clock delay			3.1		3.0		5.0		6.0	ns
t_{EN}	Register enable time			3.0		3.0		5.0		6.0	ns
t_{GLOB}	Global control delay			2.0		1.0		1.0		1.0	ns
t_{PRE}	Register preset time			2.4		2.0		3.0		4.0	ns
t_{CLR}	Register clear time			2.4		2.0		3.0		4.0	ns
t_{PIA}	PIA delay	(7)		1.4		1.0		1.0		2.0	ns
t_{LPA}	Low-power adder	(8)		11.0		10.0		11.0		13.0	ns

Table 35. EPM7192S External Timing Parameters (Part 2 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t _{AH}	Array clock hold time		1.8		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			8.0		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	125.0		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			8.0		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	125.0		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

Table 36. EPM7192S Internal Timing Parameters (Part 1 of 2) *Note (1)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.3		0.5		2.0	ns
t_{IO}	I/O input pad and buffer delay			0.3		0.5		2.0	ns
t_{FIN}	Fast input delay			3.2		1.0		2.0	ns
t_{SEXP}	Shared expander delay			4.2		5.0		8.0	ns
t_{PEXP}	Parallel expander delay			1.2		0.8		1.0	ns
t_{LAD}	Logic array delay			3.1		5.0		6.0	ns
t_{LAC}	Logic control array delay			3.1		5.0		6.0	ns
t_{IOE}	Internal output enable delay			0.9		2.0		3.0	ns
t_{OD1}	Output buffer and pad delay	C1 = 35 pF		0.5		1.5		4.0	ns
t_{OD2}	Output buffer and pad delay	C1 = 35 pF (6)		1.0		2.0		5.0	ns
t_{OD3}	Output buffer and pad delay	C1 = 35 pF		5.5		5.5		7.0	ns
t_{ZX1}	Output buffer enable delay	C1 = 35 pF		4.0		5.0		6.0	ns
t_{ZX2}	Output buffer enable delay	C1 = 35 pF (6)		4.5		5.5		7.0	ns
t_{ZX3}	Output buffer enable delay	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.0		6.0	ns
t_{SU}	Register setup time		1.1		2.0		4.0		ns

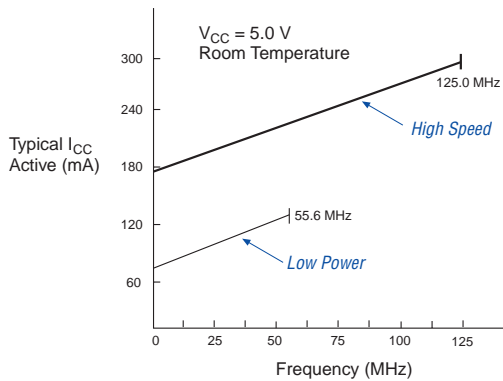
Tables 37 and 38 show the EPM7256S AC operating conditions.

Table 37. EPM7256S External Timing Parameters *Note (1)*

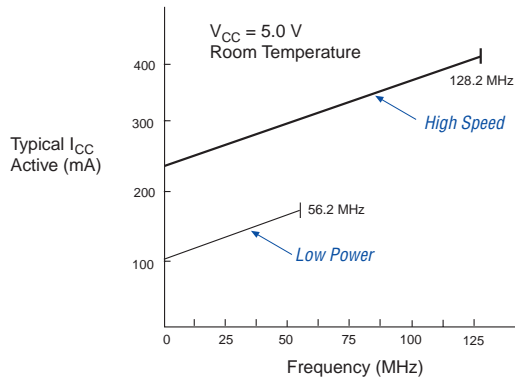
Symbol	Parameter	Conditions	Speed Grade						Unit
			-7		-10		-15		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{PD2}	I/O input to non-registered output	C1 = 35 pF		7.5		10.0		15.0	ns
t _{SU}	Global clock setup time		3.9		7.0		11.0		ns
t _H	Global clock hold time		0.0		0.0		0.0		ns
t _{FSU}	Global clock setup time of fast input		3.0		3.0		3.0		ns
t _{FH}	Global clock hold time of fast input		0.0		0.5		0.0		ns
t _{CO1}	Global clock to output delay	C1 = 35 pF		4.7		5.0		8.0	ns
t _{CH}	Global clock high time		3.0		4.0		5.0		ns
t _{CL}	Global clock low time		3.0		4.0		5.0		ns
t _{ASU}	Array clock setup time		0.8		2.0		4.0		ns
t _{AH}	Array clock hold time		1.9		3.0		4.0		ns
t _{ACO1}	Array clock to output delay	C1 = 35 pF		7.8		10.0		15.0	ns
t _{ACH}	Array clock high time		3.0		4.0		6.0		ns
t _{ACL}	Array clock low time		3.0		4.0		6.0		ns
t _{CPPW}	Minimum pulse width for clear and preset	(2)	3.0		4.0		6.0		ns
t _{ODH}	Output data hold time after clock	C1 = 35 pF (3)	1.0		1.0		1.0		ns
t _{CNT}	Minimum global clock period			7.8		10.0		13.0	ns
f _{CNT}	Maximum internal global clock frequency	(4)	128.2		100.0		76.9		MHz
t _{ACNT}	Minimum array clock period			7.8		10.0		13.0	ns
f _{ACNT}	Maximum internal array clock frequency	(4)	128.2		100.0		76.9		MHz
f _{MAX}	Maximum clock frequency	(5)	166.7		125.0		100.0		MHz

Figure 15. I_{CC} vs. Frequency for MAX 7000S Devices (Part 2 of 2)

EPM7192S



EPM7256S



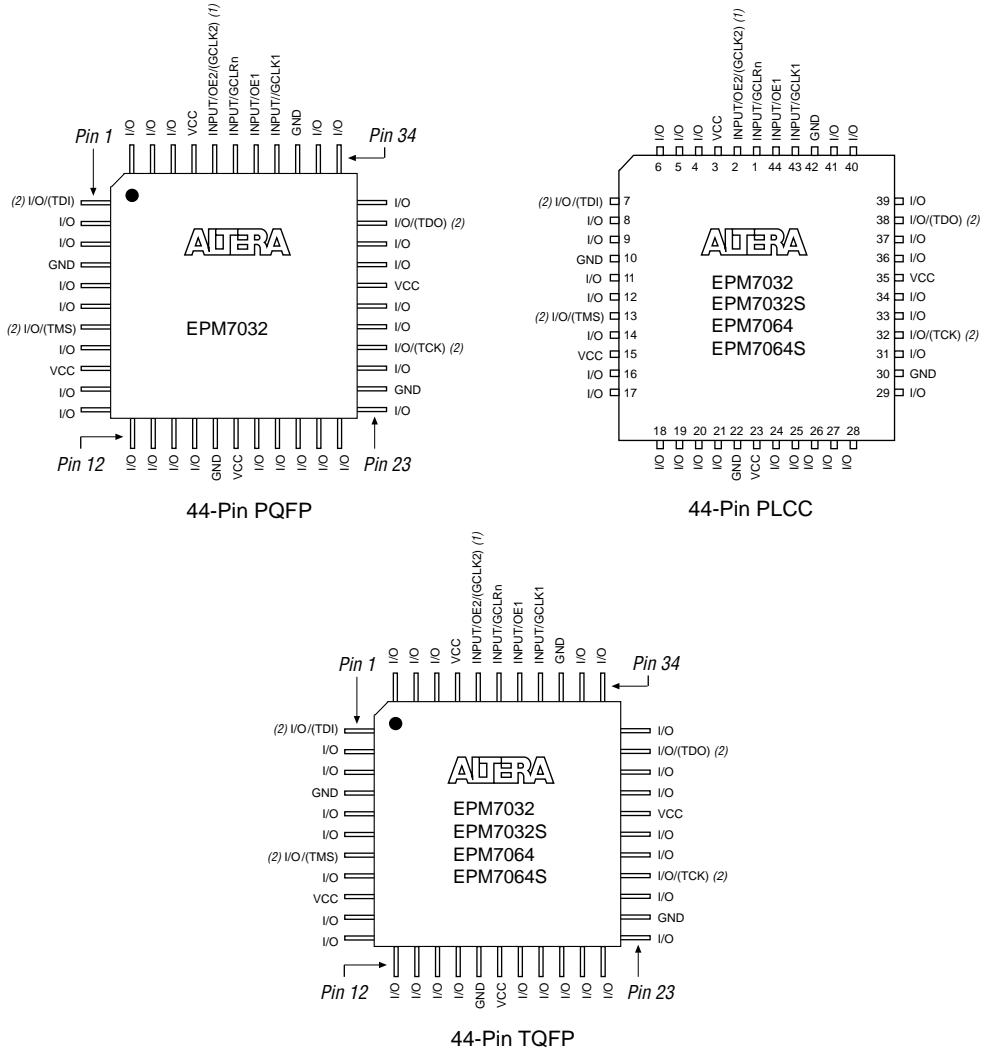
Device Pin-Outs

See the Altera web site (<http://www.altera.com>) or the *Altera Digital Library* for pin-out information.

Figures 16 through 22 show the package pin-out diagrams for MAX 7000 devices.

Figure 16. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



Notes:

- (1) The pin functions shown in parenthesis are only available in MAX 7000E and MAX 7000S devices.
- (2) JTAG ports are available in MAX 7000S devices only.

Revision History

The information contained in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7 supersedes information published in previous versions. The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

Version 6.7

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.7:

- Reference to *AN 88: Using the Jam Language for ISP & ICR via an Embedded Processor* has been replaced by *AN 122: Using Jam STAPL for ISP & ICR via an Embedded Processor*.

Version 6.6

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.6:

- Added [Tables 6](#) through [8](#).
- Added “[Programming Sequence](#)” section on [page 17](#) and “[Programming Times](#)” section on [page 18](#).

Version 6.5

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.5:

- Updated text on [page 16](#).

Version 6.4

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.4:

- Added [Note \(5\)](#) on [page 28](#).

Version 6.3

The following changes were made in the *MAX 7000 Programmable Logic Device Family Data Sheet* version 6.3:

- Updated the “[Open-Drain Output Option \(MAX 7000S Devices Only\)](#)” section on [page 20](#).



Notes: