**Welcome to E-XFL.COM**

**Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

**Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 17110 |
| Number of Logic Elements/Cells | 362000 |
| Total RAM Bits | 19822592 |
| Number of I/O | 704 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agtfd3h3f40i5n |

| Parameter | Symbol | Condition | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

(The $V_{CCIO}$ (V) spans the columns 1.2 through 3.3.)

## OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

### Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination ($R_S$ OCT) and on-chip parallel termination ($R_T$ OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | −I3, −C4 | −I5, −C5 | −C6 | |
| 25-$\Omega$ $R_S$ | Internal series termination with calibration (25-$\Omega$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |
| 50-$\Omega$ $R_S$ | Internal series termination with calibration (50-$\Omega$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |
| 34-$\Omega$ and 40-$\Omega$ $R_S$ | Internal series termination with calibration (34-$\Omega$ and 40-$\Omega$ setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 | ±15 | ±15 | ±15 | % |
| 48-$\Omega$, 60-$\Omega$, and 80-$\Omega$ $R_S$ | Internal series termination with calibration (48-$\Omega$, 60-$\Omega$, and 80-$\Omega$ setting) | $V_{CCIO}$ = 1.2 | ±15 | ±15 | ±15 | % |
| 50-$\Omega$ $R_T$ | Internal parallel termination with calibration (50-$\Omega$ setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 | −10 to +40 | −10 to +40 | −10 to +40 | % |
| 20-$\Omega$, 30-$\Omega$, 40-$\Omega$,60-$\Omega$, and 120-$\Omega$ $R_T$ | Internal parallel termination with calibration (20-$\Omega$, 30-$\Omega$, 40-$\Omega$, 60-$\Omega$, and 120-$\Omega$ setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 | −10 to +40 | −10 to +40 | −10 to +40 | % |

| Symbol | Description | $V_{CCIO}$ (V) | Value | Unit |
|--------|-------------|-----------|-------|------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.35 | 0.200 | |
| | | 1.25 | 0.200 | |
| | | 1.2 | 0.317 | |

## Pin Capacitance

**Table 1-11: Pin Capacitance for Arria V Devices**

| Symbol | Description | Maximum | Unit |
|--------|-------------|---------|------|
| $C_{IOTB}$ | Input capacitance on top/bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on left/right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output/feedback pins | 6 | pF |
| $C_{IOVREF}$ | Input capacitance on $V_{REF}$ pins | 48 | pF |

## Hot Socketing

**Table 1-12: Hot Socketing Specifications for Arria V Devices**

| Symbol | Description | Maximum | Unit |
|--------|-------------|---------|------|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 | µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8[10] | mA |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter (TX) pin | 100 | mA |

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 16 | — | — | 9.56 | 7.73 | 6.49 | — | — | dB |
| 17 | — | — | 10.43 | 8.39 | 7.02 | — | — | dB |
| 18 | — | — | 11.23 | 9.03 | 7.52 | — | — | dB |
| 19 | — | — | 12.18 | 9.7 | 8.02 | — | — | dB |
| 20 | — | — | 13.17 | 10.34 | 8.59 | — | — | dB |
| 21 | — | — | 14.2 | 11.1 | — | — | — | dB |
| 22 | — | — | 15.38 | 11.87 | — | — | — | dB |
| 23 | — | — | — | 12.67 | — | — | — | dB |
| 24 | — | — | — | 13.48 | — | — | — | dB |
| 25 | — | — | — | 14.37 | — | — | — | dB |
| 26 | — | — | — | — | — | — | — | dB |
| 27 | — | — | — | — | — | — | — | dB |
| 28 | — | — | — | — | — | — | — | dB |
| 29 | — | — | — | — | — | — | — | dB |
| 30 | — | — | — | — | — | — | — | dB |
| 31 | — | — | — | — | — | — | — | dB |

**Related Information**

**SPICE Models for Altera Devices**
Provides the Arria V HSSI HSPICE models.

## Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

**Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps**
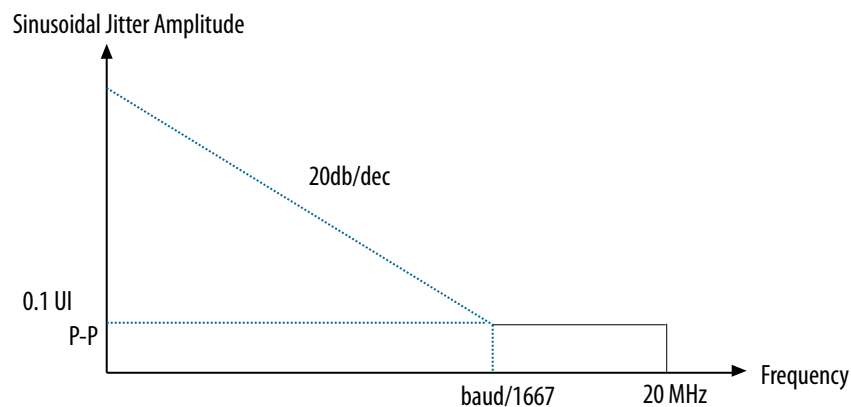


## DLL Frequency Range Specifications

**Table 1-43: DLL Frequency Range Specifications for Arria V Devices**

| Parameter | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| DLL operating frequency range | 200 – 667 | 200 – 667 | 200 – 667 | MHz |

## DQS Logic Block Specifications

**Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t$_{DQS\_PSERR}$) for Arria V Devices**

This error specification is the absolute maximum and minimum error.

| Number of DQS Delay Buffer | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| 2 | 40 | 80 | 80 | ps |

**Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals**
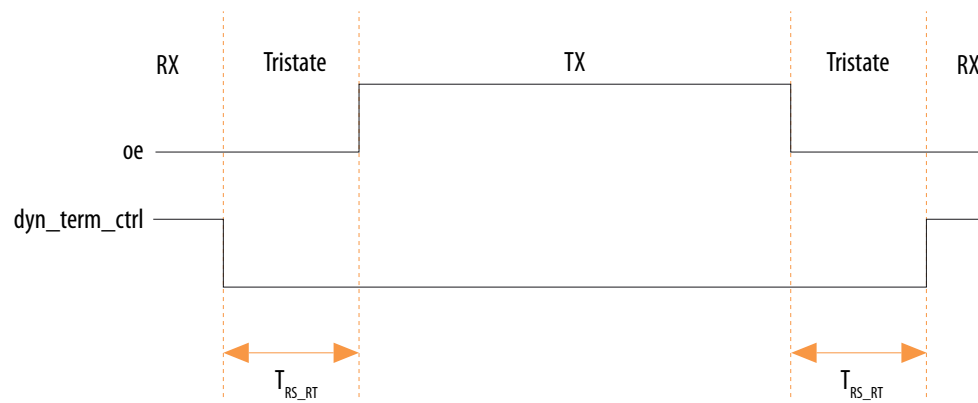


## Duty Cycle Distortion (DCD) Specifications

**Table 1-47: Worst-Case DCD on Arria V I/O Pins**

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

| Symbol | −I3, −C4 | | −C5, −I5 | | −C6 | | Unit |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

# HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

## HPS Clock Performance

### Table 1-48: HPS Clock Performance for Arria V Devices

| Symbol/Description | −I3 | −C4 | −C5, −I5 | −C6 | Unit |
|---|---|---|---|---|---|
| mpu_base_clk (microprocessor unit clock) | 1050 | 925 | 800 | 700 | MHz |
| main_base_clk (L3/L4 interconnect clock) | 400 | 400 | 400 | 350 | MHz |
| h2f_user0_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user1_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user2_clk | 200 | 200 | 200 | 160 | MHz |

## HPS PLL Specifications

### HPS PLL VCO Frequency Range

### Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

| Description | Speed Grade | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VCO range | −C5, −I5, −C6 | 320 | 1,600 | MHz |
| | −C4 | 320 | 1,850 | MHz |
| | −I3 | 320 | 2,100 | MHz |

### HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

**Related Information**

**Clock Select, Booting and Configuration chapter**
Provides more information about the clock range for different values of clock select (CSEL).

| Symbol | Description | Min | Max | Unit |
|--------|-------------|-----|-----|------|
| $T_{dh}$[89] | Data to write enable hold time | 5 | — | ns |
| $T_{cea}$ | Chip enable to data access time | — | 25 | ns |
| $T_{rea}$ | Read enable to data access time | — | 16 | ns |
| $T_{rhz}$ | Read enable to data high impedance | — | 100 | ns |
| $T_{rr}$ | Ready to read enable low | 20 | — | ns |

**Figure 1-17: NAND Command Latch Timing Diagram**
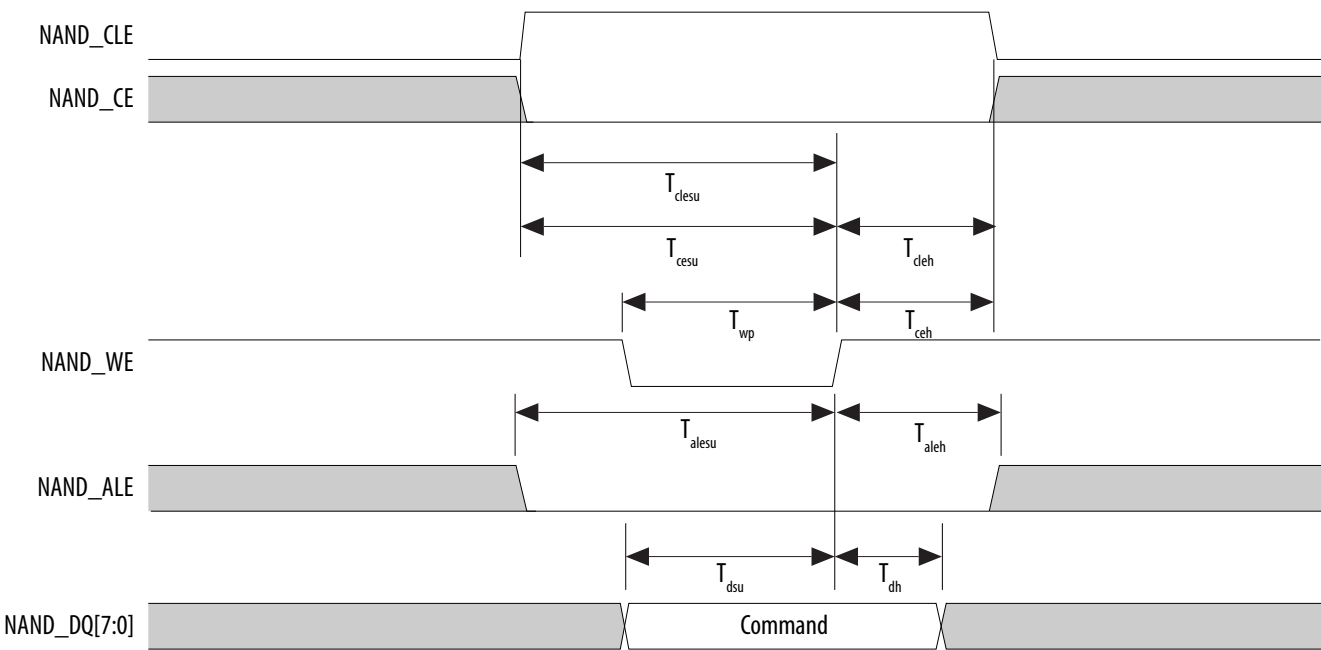
**Figure 1-20: NAND Data Read Timing Diagram**
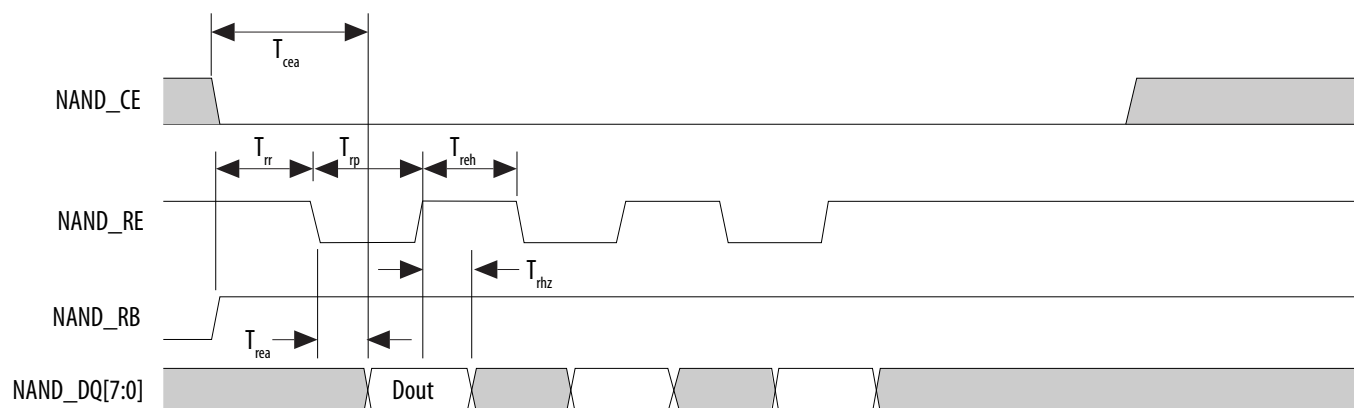


## ARM Trace Timing Characteristics

**Table 1-61: ARM Trace Timing Requirements for Arria V Devices**

Most debugging tools have a mechanism to adjust the capture point of trace data.

| Description | Min | Max | Unit |
|---|---|---|---|
| CLK clock period | 12.5 | — | ns |
| CLK maximum duty cycle | 45 | 55 | % |
| CLK to D0 –D7 output data delay | −1 | 1 | ns |

## UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

## GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 μs. The pulse width is based on a debounce clock frequency of 1 MHz.

## FPP Configuration Timing when DCLK-to-DATA[] >1

### Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------|-----------|---------|---------|------|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506[98] | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506[99] | µs |
| $t_{CF2CK}$[100] | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$[100] | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | $N - 1/f_{DCLK}$[101] | — | s |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/ ×16) | — | 125 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode[102] | 175 | 437 | µs |

[98] This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

[99] This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

[100] If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

[101] $N$ is the DCLK-to-DATA[] ratio and $f_{DCLK}$ is the DCLK frequency of the system.

[102] The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

| Term | Definition |
|------|------------|
| PLL specifications | Diagram of PLL specifications |
| | |
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V device). |
| Sampling window (SW) | Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: |

**Diagram of PLL specifications**

Switchover

CLK  $4$

Core Clock

$f_{IN}$   N   $f_{INPFD}$

PFD   CP   LF   VCO   $f_{VCO}$

Counters C0..C17   $f_{OUT}$

CLKOUT Pins

$f_{OUT}$ _EXT

GCLK

RCLK

Delta Sigma Modulator

Legend

☐ Reconfigurable in User Mode

External Feedback

**Note:**
(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.

**Sampling window (SW) timing diagram**

Bit Time

| 0.5 x TCCS | RSKM | Sampling Window (SW) | RSKM | 0.5 x TCCS |

| Date | Version | Changes |
|------|---------|---------|
| January 2015 | 2015.01.30 | • Updated the description for $V_{CC\_AUX\_SHARED}$ to "HPS auxiliary power supply" in the following tables:<br>  • Absolute Maximum Ratings for Arria V Devices<br>  • HPS Power Supply Operating Conditions for Arria V SX and ST Devices<br>• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.<br>• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.<br>• Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for –I3 speed grade) and 462 MHz (for –C4 speed grade) to 400 MHz.<br>• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C5, –I5, and –C6 speed grades), 1,850 MHz (for –C4 speed grade), and 2,100 MHz (for –I3 speed grade).<br>• Changed the symbol for HPS PLL input jitter divide value from NR to N.<br>• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:<br>  • SPI Master Timing Requirements for Arria V Devices<br>  • SPI Slave Timing Requirements for Arria V Devices<br>• Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.<br>• Added HPS JTAG timing specifications.<br>• Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 13 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.<br>• Updated the value in the $V_{ICM}$ (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table. |

| Date | Version | Changes |
|---|---|---|
| November 2012 | 3.0 | • Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.<br>• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.<br>• Added HPS information:<br>   • Added "HPS Specifications" section.<br>   • Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.<br>   • Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.<br>   • Updated Table 3 and Table 5. |
| October 2012 | 2.4 | • Updated Arria V GX $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ minimum and maximum values, and data rate in Table 4.<br>• Added receiver $V_{ICM}$ (AC coupled) and $V_{ICM}$ (DC coupled) values, and transmitter $V_{OCM}$ (AC coupled) and $V_{OCM}$ (DC coupled) values in Table 20 and Table 21. |
| August 2012 | 2.3 | Updated the SERDES factor condition in Table 30. |
| July 2012 | 2.2 | • Updated the maximum voltage for $V_I$ (DC input voltage) in Table 1.<br>• Updated Table 20 to include the Arria V GX -I3 speed grade.<br>• Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.<br>• Updated the SERDES factor condition in Table 30.<br>• Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade. |
| June 2012 | 2.1 | Updated $V_{CCR\_GXBL/R}$, $V_{CCT\_GXBL/R}$, and $V_{CCL\_GXBL/R}$ values in Table 4. |

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration [146] | $V_{CCR\_GXB} = 1.0$ V ($V_{ICM} = 0.75$ V) | — | — | 1.8 | — | — | 1.8 | V |
| | $V_{CCR\_GXB} = 0.85$ V ($V_{ICM} = 0.6$ V) | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins [147][148] | — | 85 | — | — | 85 | — | — | mV |
| Differential on-chip termination resistors | 85−Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100−Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120−Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150−Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |

[146] The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to $4 \times$ (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

[147] The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

[148] Minimum eye opening of 85 mV is only for the unstressed input eye condition.

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## Typical VOD Settings

**Table 2-32: Typical V$_{OD}$ Setting for Arria V GZ Channel, TX Termination = 100 Ω**

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

| Symbol | V$_{OD}$ Setting | V$_{OD}$ Value (mV) | V$_{OD}$ Setting | V$_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 0 [166] | 0 | 32 | 640 |
| | 1 [166] | 20 | 33 | 660 |
| | 2 [166] | 40 | 34 | 680 |
| | 3 [166] | 60 | 35 | 700 |
| | 4 [166] | 80 | 36 | 720 |
| | 5 [166] | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| V$_{OD}$ **differential peak to peak typical** | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |

[166] If TX termination resistance = 100 Ω, this VOD setting is illegal.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{DUTY}$ | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | ps |

## Receiver High-Speed I/O Specifications

**Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Send Feedback

### OCT Calibration Block Specifications

**Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (See the figure below.) | — | 2.5 | — | ns |

**Figure 2-6: Timing Diagram for oe and dyn_term_ctrl Signals**
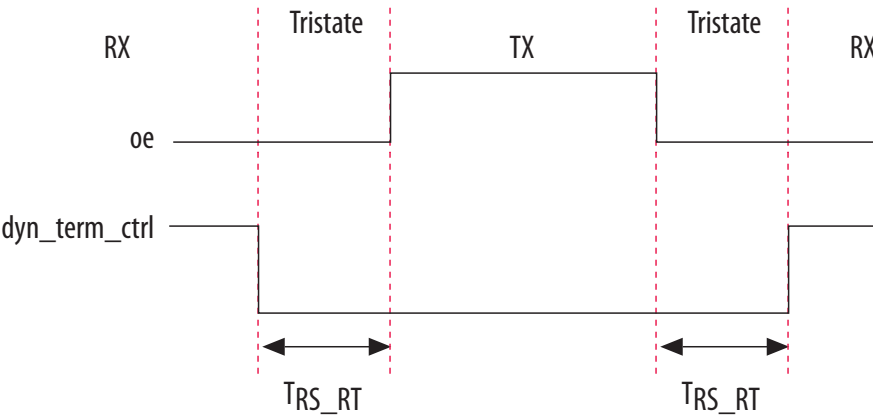
## Duty Cycle Distortion (DCD) Specifications

### Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

| Symbol | C3, I3L | | C4, I4 | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | % |

# Configuration Specification

## POR Specifications

### Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

| POR Delay | Minimum (ms) | Maximum (ms) |
|---|---|---|
| Fast | 4 | 12 [202] |
| Standard | 100 | 300 |

**Related Information**

**Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

---

[202] The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------|-----------|---------|---------|------|
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | $4 \times$ maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} +$ $(8576 \times$ CLKUSR period) [209] | — | — |

**Related Information**

- **DCLK-to-DATA[] Ratio (r) for FPP Configuration** on page 2-57
- **Configuration, Design Security, and Remote System Upgrades in Arria V Devices**

---

[208] The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

[209] To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

## Passive Serial Configuration Timing

### Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.
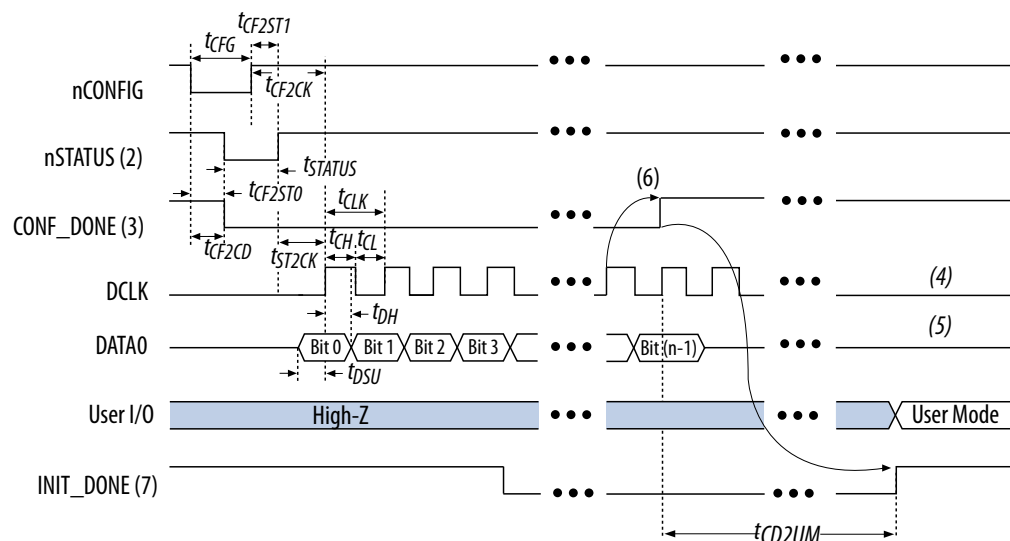


Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

| Term | Definition |
|---|---|
| $t_C$ | High-speed receiver and transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on the high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| $t_{OUTPJ\_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| $t_{OUTPJ\_DC}$ | Period jitter on the dedicated clock output driven by a PLL. |
| $t_{RISE}$ | Signal low-to-high transition time (20-80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(receiver input clock frequency multiplication factor) = $t_C/w$) |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |