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Intel - 5AGTFD7K3F40I3N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

2014.10	
Product Status	Obsolete
Number of LABs/CLBs	23780
Number of Logic Elements/Cells	504000
Total RAM Bits	27695104
Number of I/O	704
Number of Gates	-
Voltage - Supply	1.12V ~ 1.18V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agtfd7k3f40i3n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power		1.80	V
V _{CCR_GXB}	_GXB Receiver power		1.50	V
V _{CCT_GXB}	Transmitter power		1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage		3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	-0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	-0.50	3.25	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

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1-4 Recommended Operating Conditions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
	AC input voltage	4.1	11	%
		4.15	9	%
Vi (AC)		4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.



Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCL_GXBL}	GX and SX speed grades—clock network power (left side)	1 08/1 12	1 1/1 15(6)	1 14/1 18	V
V _{CCL_GXBR}	GX and SX speed grades—clock network power (right side)	1.00/ 1.12	1.1/1.13	1.14/1.10	v
V _{CCL_GXBL}	GT and ST speed grades—clock network power (left side)	117	1 20	1 22	V
V _{CCL_GXBR}	GT and ST speed grades—clock network power (right side)	1.17	1.20	1.23	v

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the power supply connection for different data rates.

HPS Power Supply Operating Conditions

Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
HPS core	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V	
V _{CC_HPS}	voltage and periphery circuitry power supply	-I3	1.12	1.15	1.18	V

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX Vor	Setting for Arria V Tran	sceiver Channels with	termination of 100 Ω

Symbol	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)	V _{OD} Setting ⁽⁵⁸⁾	V _{OD} Value (mV)
	6 ⁽⁵⁹⁾	120	34	680
	7 ⁽⁵⁹⁾	140	35	700
	8(59)	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V _{OD} differential peak-to-peak typical	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates \leq 5 Gbps.



Protocol	Sub-protocol	Data Rate (Mbps)
	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
Common Public Radio Interface (CPRI)	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII ⁽⁶⁰⁾	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
	OBSAI 768	768
ODSAL	OBSAI 1536	1,536
ODSAI	OBSAI 3072	3,072
	OBSAI 6144	6,144
	SDI 270 SD	270
Serial digital interface (SDI)	SDI 1485 HD	1,485
	SDI 2970 3G	2,970



⁽⁶⁰⁾ You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

Symbol/Description	-13	-C4	–C5, –I5	-C6	Unit
mpu_base_clk (microprocessor unit clock)	1050	925	800	700	MHz
main_base_clk (L3/L4 interconnect clock)	400	400	400	350	MHz
h2f_user0_clk	100	100	100	100	MHz
h2f_user1_clk	100	100	100	100	MHz
h2f_user2_clk	200	200	200	160	MHz

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

Description	Speed Grade	Minimum	Maximum	Unit
	-C5, -I5, -C6	320	1,600	MHz
VCO range	-C4	320	1,850	MHz
	-I3	320	2,100	MHz

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

Clock Select, Booting and Configuration chapter

Provides more information about the clock range for different values of clock select (CSEL).



Figure 1-19: NAND Data Write Timing Diagram







This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

Arria V Device Overview

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in -3 (fastest) and -4 core speed grades. Industrial devices are offered in -3L and -4 core speed grades. Arria V GZ devices are offered in -2 and -3 transceiver speed grades.

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

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2-4 Recommended Operating Conditions

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only $\sim 21\%$ over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~ 2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices
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Symbol	Description	Condition (V)	Overshoot Duration as % @ T」= 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)	AC input voltage	4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽¹¹⁴⁾	Typical	Maximum ⁽¹¹⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply ⁽¹¹⁵⁾	—	0.82	0.85	0.88	V

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.





⁽¹¹⁵⁾ The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
		0.82	0.85	0.88	
V _{CCR_GXBL} ⁽¹²¹⁾	Receiver analog power supply (left side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCR_GXBR} ⁽¹²¹⁾	Receiver analog power supply (right side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCT_GXBL} ⁽¹²¹⁾	Transmitter analog power supply (left side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
		0.82	0.85	0.88	
V _{CCT_GXBR} ⁽¹²¹⁾	Transmitter analog power supply (right side)	0.97	1.0	1.03	V
		1.03	1.05	1.07	
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V



⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

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	V _{IL(D}	_{C)} (V)	V _{IH(DC}	_{_)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	Ι (ma Δ)	I (m A)
i/O Standard	Min	Max	Min	Max	Max	Min	Max	Min	i _{ol} (mA)	I _{oh} (MA)
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCIO} – 0.28	13.4	-13.4
SSTL-15 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{ m CCIO}$	$0.8 \times V_{ m CCIO}$	8	-8
SSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{ m CCIO}$	$0.8 \times V_{ m CCIO}$	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	-
SSTL-125 Class I, II	_	V _{REF} – 0.85	V _{REF} + 0.85	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	_
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	—	_
HSTL-18 Class I		V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	$V_{\rm CCIO}$ – 0.4	8	-8
HSTL-18 Class II		V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.2	V _{REF} + 0.2	0.4	$V_{\rm CCIO}$ – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{ m CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{ m CCIO}$	16	-16
HSUL-12	—	V _{REF} – 0.13	V _{REF} + 0.13	_	V _{REF} - 0.22	V_{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	_

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I/O Standard	V _{CCIO} (V)		V _{DIF(DC)} (V)			$V_{X(AC)}(V)$			V _{CM(DC)} (V)			V _{DIF(AC)} (V)	
	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V _{CCIO} + 0.3		$0.5 \times V_{CCIO}$	_	$0.4 \times V_{\rm CCIO}$	0.5 × V _{CC} IO	$0.6 \times V_{CCIO}$	0.3	V _{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V _{CCIO} – 0.12	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	0.5 × V _{CC} IO	0.6 × V _{CCIO}	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	Vc	V _{CCIO} (V) ⁽¹²⁸⁾		V _{ID} (mV) ⁽¹²⁹⁾		V _{ICM(DC)} (V)		V _{OD} (V) ⁽¹³⁰⁾			V _{OCM} (V) ⁽¹³⁰⁾				
	Min	Тур	Max	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V	2 375 2 5 2 625	5 100 V _{CM} =		0.05	D _{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375			
(131)	2.373	2.5	2.025	100	1.25 V		1.05	D _{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS (132)	2.375	2.5	2.625	100						_	_			—	

⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.



⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

⁽¹³⁰⁾ RL range: $90 \le RL \le 110 \Omega$.

⁽¹³¹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

 $^{^{(132)}}$ There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

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Sumbol/Description	Conditions	Transce	eiver Speed (Grade 2	Transce	eiver Speed (Grade 3	Unit	
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max		
	100 Hz	—	_	-70	—	—	-70	dBc/Hz	
	1 kHz	—	—	-90		—	-90	dBc/Hz	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾	10 kHz	—	—	-100	_	—	-100	dBc/Hz	
	100 kHz	—	—	-110	_	—	-110	dBc/Hz	
	≥1 MHz	—	—	-120		—	-120	dBc/Hz	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	ps (rms)	
R _{REF}	—	—	1800 ±1%	_		1800 ±1%		Ω	

Related Information

Arria V Device Overview

For more information about device ordering codes.

Transceiver Clocks

Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Arria V GZ Device Datasheet

Altera Corporation



 $^{^{(141)}}$ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20 *log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.

Mode (164)	Transceiver	PMA Width	20	20	16	16	10	10	8	8
Mode	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
Desister	2	C3, I3L core speed grade	9.9	9	7.92	7.2	4.9	4.,5	3.92	3.6
icgistei	3	C4, I4 core speed grade	8.8	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Related Information

Operating Conditions on page 2-1

10G PCS Data Rate

Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices

Mode ⁽¹⁶⁵⁾	Transceiver Speed	PMA Width	64	40	40	40	32	32
Mode	Grade	PCS Width	64	66/67	50	40	64/66/67	32
FIFO	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92
Pagistar	2	C3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
Kegister	3	C4, I4 core speed grade	10.3125	10.3125	10.69	10.3125	9.92	9.92

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.



⁽¹⁶⁵⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol	Parameter	Min	Тур	Max	Unit
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Related Information

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mada	Performar	nce		Unit
Mode	C3, I3L	C4	14	Onit
Modes using One DSP Block				
Three 9 × 9	480	42	20	MHz
One 18 × 18	480	420	400	MHz
Two partial 18×18 (or 16×16)	480	420	MHz	
One 27 × 27	400	35	MHz	
One 36 × 18	400	35	50	MHz
One sum of two 18×18 (One sum of two 16×16)	400	35	50	MHz
One sum of square	400	35	50	MHz
One 18×18 plus $36 (a \times b) + c$	400	35	50	MHz
Modes using Two DSP Blocks				
Three 18 × 18	400	350		MHz
One sum of four 18×18	380	30	00	MHz



OCT Calibration Block Specifications

Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T _{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	—	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (See the figure below.)		2.5		ns

Figure 2-6: Timing Diagram for oe and dyn_term_ctrl Signals





Term	Definition		
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround		
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}		
f _{HSCLK}	Left and right PLL input clock frequency.		
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.		
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.		
J	High-speed I/O block—Deserialization factor (width of parallel data bus).		









Date	Version	Changes
July 2014	3.8	 Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	 Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	 Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	 Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	 Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.

