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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7362
Number of Logic Elements/Cells	156000
Total RAM Bits	11746304
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agtmc3d3f31i5n

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Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Core voltage power supply	-0.50	1.43	V
V _{CCP}	Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply	-0.50	1.43	V
V _{CCPGM}	Configuration pins power supply	-0.50	3.90	V
V _{CC_AUX}	Auxiliary supply	-0.50	3.25	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.50	3.90	V
V _{CCPD}	I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO}	I/O power supply	-0.50	3.90	V
V _{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	-0.50	1.80	V
V _{CCA_FPLL}	PLL analog power supply	-0.50	3.25	V
V _{CCA_GXB}	Transceiver high voltage power	-0.50	3.25	V
V _{CCH_GXB}	Transmitter output buffer power	-0.50	1.80	V
V _{CCR_GXB}	Receiver power	-0.50	1.50	V
V _{CCT_GXB}	Transmitter power	-0.50	1.50	V
V _{CCL_GXB}	Transceiver clock network power	-0.50	1.50	V
VI	DC input voltage	-0.50	3.80	V
V _{CC_HPS}	HPS core voltage and periphery circuitry power supply	-0.50	1.43	V
V _{CCPD_HPS}	HPS I/O pre-driver power supply	-0.50	3.90	V
V _{CCIO_HPS}	HPS I/O power supply	-0.50	3.90	V
V _{CCRSTCLK_HPS}	HPS reset and clock input pins power supply	-0.50	3.90	V



Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	-0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	-0.50	3.25	V
I _{OUT}	DC output current per pin	-25	40	mA
T _J	Operating junction temperature	-55	125	°C
T _{STG}	Storage temperature (no bias)	-65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

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Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCL_GXBL}	GX and SX speed grades—clock network power (left side)	1 08/1 12	1 1/1 15(6)	1 14/1 18	V
V _{CCL_GXBR}	GX and SX speed grades—clock network power (right side)	1.00/ 1.12	1.1/1.15	1.14/1.10	,
V _{CCL_GXBL}	GT and ST speed grades—clock network power (left side)	117	1 20	1 22	V
V _{CCL_GXBR}	GT and ST speed grades—clock network power (right side)	1.17	1.20	1.25	v

Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines

Provides more information about the power supply connection for different data rates.

HPS Power Supply Operating Conditions

Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

Symbol	Description	Condition	Minimum ⁽⁷⁾	Typical	Maximum ⁽⁷⁾	Unit
	HPS core	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V _{CC_HPS}	voltage and periphery circuitry power supply	-I3	1.12	1.15	1.18	V

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.



⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C.

Symbol	Description	V _{CCIO} (V)	Value	Unit
dR/dV		3.0	0.100	
		2.5	0.100	
	OCT variation with voltage without recalibration	1.8	0.100	
		1.5	0.100	%/mV
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	



Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

I/O Standard		V _{CCIO} (V)			V _{REF} (V) V _{TT} (V)		V _{TT} (V)		
i/O Stanuaru	Min	Тур	Max	Min	Тур	Мах	Min	Тур	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} - 0.04	V _{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95		V _{CCIO} /2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9		V _{CCIO} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$		V _{CCIO} /2	_
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	_		

Tuble 1 15, Single Ended SSTE, 15TE, and 15OE / O hererence voltage Specifications for Anna v Devices



Sumbol/Decertion	Condition	Т	Unit		
Symbol/Description	Condition	Min	Тур	Мах	Unit
Data rate (10-Gbps transceiver) ⁽⁴⁴⁾	—	0.611	_	10.3125	Gbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver $\mathrm{pin}^{\scriptscriptstyle{(45)}}$	—	_		1.2	V
Absolute $\mathrm{V}_{\mathrm{MIN}}$ for a receiver pin	—	-0.4		—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	_	_	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	_	_	_	2.2	V
Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾	—	100		_	mV
V _{ICM} (AC coupled)	—	_	750 ⁽⁴⁷⁾ /800	—	mV
V _{ICM} (DC coupled)	\leq 3.2Gbps ⁽⁴⁸⁾	670	700	730	mV
	85- Ω setting		Ω		
Differential on-chip termination	100- Ω setting		100		Ω
resistors	120- Ω setting		120		Ω
-	150-Ω setting		150		Ω
$t_{LTR}^{(49)}$	_	_		10	μs
$t_{LTD}^{(50)}$	—	4	—	—	μs

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.



⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

 $^{^{(47)}}$ The AC coupled $V_{\rm ICM}$ is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

 $^{^{(49)}}$ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

Symbol/Description	Condition	Tran	sceiver Speed Gra	Unit	
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	transceiver block transmitter ×6 PMA bonded mode el-to-channel skew			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit	
Symbol Description	Min	Max	onit	
Supported data range	0.611	10.3125	Gbps	
fPLL supported data range	611	3125	Mbps	

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



1-82 PS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(105)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽¹⁰⁵⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f_{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽¹⁰⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	_	_
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.



 $^{^{(105)}}$ If <code>nstatus</code> is monitored, follow the t_{ST2CK} specification. If <code>nstatus</code> is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰⁶⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

1-96 Document Revision History

Date	Version	Changes
June 2015	2015.06.16	 Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:
		True RSDS output standard: data rates of up to 360 Mbps
		 True mini-LVDS output standard: data rates of up to 400 Mbps
		 Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.
		Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.
		 Updated T_h location in I²C Timing Diagram.
		 Updared T_{wp} location in NAND Address Latch Timing Diagram.
		 Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.
		• Updated the maximum value for t _{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.
		• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.
		FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1
		 FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1
		AS Configuration Timing Waveform
		PS Configuration Timing Waveform



|--|

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transce	eiver Speed	Unit	
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	Onit
Rise time	Measure at $\pm 60 \text{ mV}$ of differential signal ⁽¹³⁸⁾	_	_	400	_	_	400	nc
Fall time	Measure at ±60 mV of differential signal ⁽¹³⁸⁾	—		400			400	ps
Duty cycle	_	45		55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express [®] (PCIe)	30		33	30	_	33	kHz
Spread-spectrum downspread	PCIe		0 to	_		0 to		%
			-0.5			-0.5		
On-chip termination resistors	—	_	100	_		100		Ω
Absolute V _{MAX}	Dedicated reference clock pin	—		1.6			1.6	V
	RX reference clock pin	_		1.2			1.2	
Absolute V _{MIN}	—	-0.4	_	_	-0.4	—	_	V
Peak-to-peak differential input voltage	—	200		1600	200	_	1600	mV
V _{ICM} (AC coupled)	Dedicated reference clock pin	1000/900/850 (139)			1000/900/850 (139)			mV
	RX reference clock pin	1.	0/0.9/0.85 (1	40)	1.0/0.9/0.85 ⁽¹⁴⁰⁾			mV
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250		550	250		550	mV



 ⁽¹³⁸⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.
 (139) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
 (140) This supply follows VCCR_GXB

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Sumbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit	
Symbol/Description	Conditions	Min	Тур	Мах	Min	Тур	Max		
	100 Hz	—	_	-70	_	_	-70	dBc/Hz	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾	1 kHz	—	—	-90		—	-90	dBc/Hz	
	10 kHz	—	—	-100	_	_	-100	dBc/Hz	
	100 kHz	—	—	-110	_	_	-110	dBc/Hz	
	≥1 MHz	—	—	-120		_	-120	dBc/Hz	
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾	10 kHz to 1.5 MHz (PCIe)	_	_	3	_	_	3	ps (rms)	
R _{REF}	_	—	1800 ±1%	_		1800 ±1%		Ω	

Related Information

Arria V Device Overview

For more information about device ordering codes.

Transceiver Clocks

Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Arria V Device Overview.

Arria V GZ Device Datasheet

Altera Corporation



 $^{^{(141)}}$ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20 *log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.

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Symbol	Parameter	Min	Тур	Max	Unit
t (171) (172)	Input clock cycle-to-cycle jitter (f_{REF} $\geq 100~MHz)$	—	—	0.15	UI (p-p)
'INCCJ',	Input clock cycle-to-cycle jitter ($f_{REF} < 100 \text{ MHz}$)	-750		+750	ps (p-p)
tourny p.c. ⁽¹⁷³⁾	Period Jitter for dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)			175	ps (p-p)
COUTPJ_DC	Period Jitter for dedicated clock output in integer PLL (f _{OUT} < 100 Mhz)	—		17.5	mUI (p-p)
. (173)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_		$25^{(176)},$ 17.5 ⁽¹⁷⁴⁾	mUI (p-p)
t	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
toutccj_dc ⁽¹⁷³⁾	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL (f _{OUT} < 100 MHz)	_		17.5	mUI (p-p)
t _{FOUTCCJ_DC} ⁽¹⁷³⁾	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	—		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)			$25^{(176)}, \\ 17.5^{(174)}$	mUI (p-p)

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps. ⁽¹⁷²⁾ The f_{REF} is fIN/N specification applies when N = 1.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be \geq 1200 MHz.



⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.999999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

Symbol	Parameter	Min	Тур	Max	Unit
k _{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f _{RES}	Resolution of VCO frequency ($f_{INPFD} = 100 \text{ MHz}$)	390625	5.96	0.023	Hz

Related Information

- Duty Cycle Distortion (DCD) Specifications on page 2-56
- DLL Range Specifications on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mada	Performar	nce		Unit	
Mode	C3, I3L	C4 I4		Onit	
Modes using One DSP Block					
Three 9 × 9	480	42	20	MHz	
One 18 × 18	480	420	400	MHz	
Two partial 18×18 (or 16×16)	480	420	400	MHz	
One 27 × 27	400	350		MHz	
One 36 × 18	400	350		MHz	
One sum of two 18×18 (One sum of two 16×16)	400	350		MHz	
One sum of square	400	350		MHz	
One 18×18 plus $36 (a \times b) + c$	400	350		MHz	
Modes using Two DSP Blocks					
Three 18 × 18	400	35	50	MHz	
One sum of four 18×18	380	30	00	MHz	



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Symbol	Conditions	C3, I3L		C4, I4			Unit	
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onic
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards ⁽¹⁷⁹⁾	Clock boost factor W = 1 to 40 $^{(180)}$	5	_	625	5	_	525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		625	5		525	MHz
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		420	5		420	MHz
f _{HSCLK_OUT} (output clock frequency)	—	5		625 (181)	5		525 (181)	MHz

Transmitter High-Speed I/O Specifications

Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



 $^{^{(179)}\,}$ This only applies to DPA and soft-CDR modes.

⁽¹⁸⁰⁾ Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

⁽¹⁸¹⁾ This is achieved by using the LVDS clock network.



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
Sampling Window	—	_		300	_		300	ps



DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 - 890	300 - 890	MHz

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$.

Speed Grade	Min	Мах	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -3 speed grade is ± 84 ps or ± 42 ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

Configuration Scheme	Decompression	Design Security	ty DCLK-to-DATA[] Ratio	
FPP ×8	Disabled	Disabled	1	
	Disabled	Enabled	1	
	Enabled	Disabled	2	
	Enabled	Enabled	2	
	Disabled	Disabled	1	
FDD v16	Disabled	Enabled	2	
111 ×10	Enabled	Disabled	4	
	Enabled	Enabled	4	
FPP ×32	Disabled	Disabled	1	
	Disabled	Enabled	4	
	Enabled	Disabled	8	
	Enabled	Enabled	8	





Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CF2CD}	nCONFIG low to CONF_DONE low	_	600	ns
t _{CF2ST0}	nconfig low to istatus low		600	ns
t _{CFG}	nCONFIG low pulse width	2		μs
t _{STATUS}	nSTATUS low pulse width	268	1,506 (205)	μs
t _{CF2ST1}	nCONFIG high to nSTATUS high		1,506 (206)	μs
t _{CF2CK} (207)	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t _{ST2CK} ⁽²	hstatus high to first rising edge of DCLK	2	_	μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	_	ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 imes 1/f_{ m MAX}$	_	s
t _{CL}	DCLK low time	$0.45 imes 1/f_{ m MAX}$	_	s
t _{CLK}	DCLK period	1/f _{MAX}	_	s
f _{MAX}	DCLK frequency (FPP ×8/×16)	_	125	MHz
	DCLK frequency (FPP ×32)		100	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽²⁰⁸⁾	175	437	μs

⁽²⁰⁵⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.



⁽²⁰⁶⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²⁰⁷⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Glossary

Table 2-68: Glossary





Term	Definition		
	Single-Ended WaveformVODPositive Channel (p) = VOHVCMNegative Channel (n) = VOLGroundGround		
	Differential Waveform V_{0D} V_{0D} V_{0D} V_{0D}		
f _{HSCLK}	Left and right PLL input clock frequency.		
f _{HSDR}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA.		
f _{hsdrdpa}	High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA.		
J	High-speed I/O block—Deserialization factor (width of parallel data bus).		



