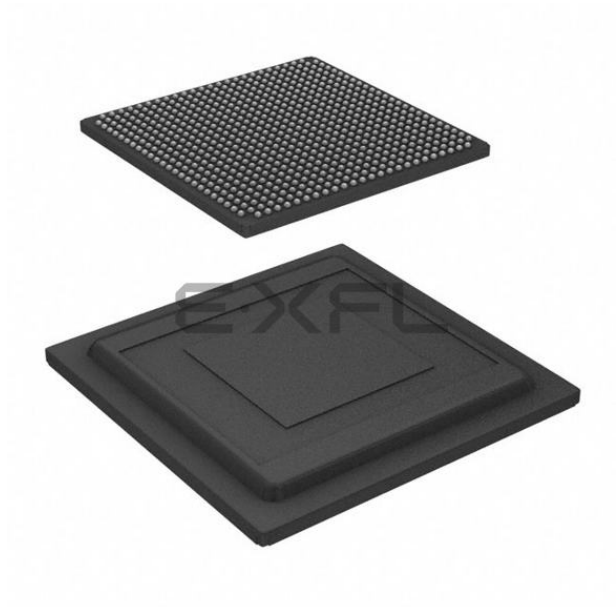

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7362
Number of Logic Elements/Cells	156000
Total RAM Bits	11746304
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba3d4f27c4n

Symbol	Description	Condition	Minimum[1]	Typical	Maximum[1]	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCBAT}[2]	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_{CCPD}[3]	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.
(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.
(3) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of ±5% and a temperature range of 0°C to 85°C.

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.100	%/mV
		2.5	0.100	
		1.8	0.100	
		1.5	0.100	
		1.35	0.150	
		1.25	0.150	
		1.2	0.150	

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Minimum differential eye opening at the receiver serial input pins[30]	—	100	—	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	0.7/0.75/ 0.8[31]	—	—	0.7/0.75/ 0.8 [31]	—	mV
V_{ICM} (DC coupled)	≤ 3.2Gbps[32]	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
t_{LTR}[33]	—	—	—	10	—	—	10	µs
t_{LTD}[34]	—	4	—	—	4	—	—	µs
t_{LTD_manual}[35]	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$[36]	—	15	—	—	15	—	—	µs
Programmable ppm detector[37]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000						ppm

(30) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled V_{ICM} = 700 mV for Arria V GX and SX in PCIe mode only. The AC coupled V_{ICM} = 750 mV for Arria V GT and ST in PCIe mode only.

(32) For standard protocol compliance, use AC coupling.

(33) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(34) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(35) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(36) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
t_{LTD_manual}[51]	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$[52]	—	15	—	—	µs
Programmable ppm detector[53]	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run length	—	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3[54] DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams.			

Table 1-29: Transmitter Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.5 V PCML				
Data rate (6-Gbps transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
V_{OCM} (AC coupled)	—	—	650	—	mV
V_{OCM} (DC coupled)	≤ 3.2 Gbps[48]	670	700	730	mV

(51) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.
(52) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.
(53) The rate match FIFO supports only up to ±300 ppm.
(54) The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

Table 1-38: Memory Block Performance Specifications for Arria V Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–I3, –C4	–I5, –C5	–C6	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Initialization

Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	T_{init}
CLKUSR[107]	PS and FPP	125	
	AS	100	
DCLK	PS and FPP	125	

Configuration Files

Table 1-72: Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

(107) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Remote System Upgrades

Table 1-74: Remote System Upgrade Circuitry Timing Specifications for Arria V Devices

Parameter	Minimum	Unit
$t_{RU\_nCONFIG}$ (110)	250	ns
$t_{RU\_nRSTIMER}$ (111)	250	ns

Related Information

- **Remote System Upgrade State Machine**
  Provides more information about configuration reset (RU_CONFIG) signal.
- **User Watchdog Timer**
  Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 1-75: User Watchdog Internal Oscillator Frequency Specifications for Arria V Devices

Parameter	Minimum	Typical	Maximum	Unit
User watchdog internal oscillator frequency	5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O timing and the Quartus Prime Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

(110) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.
(111) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

Term	Definition
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—Clock boost factor

Document Revision History

Date	Version	Changes

December 2016	2016.12.09	• Updated V_{ICM} (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table.
		• Added maximum specification for T_d in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table.
		• Updated T_{init} specifications in the following tables:
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices
		  • FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices
		  • AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices
		  • PS Timing Parameters for Arria V Devices

June 2016	2016.06.10	• Changed pin capacitance to maximum values.
		• Updated SPI Master Timing Requirements for Arria V Devices table.
		  • Added T_{su} and T_h specifications.
		  • Removed T_{dinmax} specifications.
		• Updated SPI Master Timing Diagram.
		• Updated T_{clk} spec from maximum to minimum in I^2C Timing Requirements for Arria V Devices table.

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade			
	C3	C4	I3L	I4
2	Yes	—	Yes	—
3	—	Yes	—	Yes

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Power supply for core voltage and periphery circuitry	–0.5	1.35	V
V_{CCPT}	Power supply for programmable power technology	–0.5	1.8	V
V_{CCPGM}	Power supply for configuration pins	–0.5	3.9	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	–0.5	3.4	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.9	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.9	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CCD_FPLL}	PLL digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.4	V

Symbol	Description	Condition	Minimum[114]	Typical	Maximum [114]	Unit
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard POR	200 µs	—	100 ms	—
		Fast POR	200 µs	—	4 ms	—

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

Symbol	Description	Minimum [118]	Typical	Maximum[118]	Unit
V_{CCA_GXBL} [119], [120]	Transceiver channel PLL power supply (left side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCA_GXBR} [119], [120]	Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(119) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(120) When using ATX PLLs, the supply must be 3.0 V.

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (124)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

Symbol	Description	V_{CCIO} Conditions (V) (125)	Value (126)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	k Ω
		2.5 ±5%	25	k Ω
		1.8 ±5%	25	k Ω
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	k Ω
		1.25 ±5%	25	k Ω
		1.2 ±5%	25	k Ω

(124) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.
(125) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(126) These specifications are valid with a ±10% tolerance to cover changes over PVT.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	—	—	650	—	—	650	—	mV
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	ps

Related Information

Arria V Device Overview

For more information about device ordering codes.

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

Symbol	V_{OD} Setting	V_{OD} Value (mV)	V_{OD} Setting	V_{OD} Value (mV)
V_{OD} **differential peak to peak typical**	0 (166)	0	32	640
	1 (166)	20	33	660
	2 (166)	40	34	680
	3 (166)	60	35	700
	4 (166)	80	36	720
	5 (166)	100	37	740
	6	120	38	760
	7	140	39	780
	8	160	40	800
	9	180	41	820
	10	200	42	840
	11	220	43	860
	12	240	44	880
	13	260	45	900
	14	280	46	920

(166) If TX termination resistance = 100 Ω,this VOD setting is illegal.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197)	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197)	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(198)	—	(200)	(198)	—	(200)	Mbps
	SERDES factor J = 2, uses DDR Registers	(198)	—	(199)	(198)	—	(199)	Mbps
	SERDES factor J = 1, uses SDR Register	(198)	—	(199)	(198)	—	(199)	Mbps

(192) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
DPA run length	—	—	—	10000	—	—	10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled

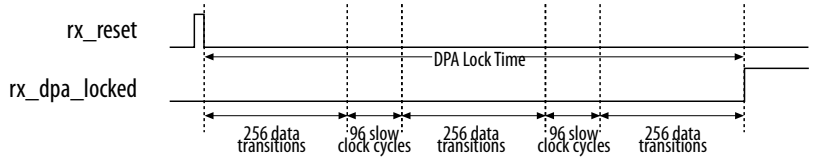


Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (201)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions

(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (201)	Maximum
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Soft CDR Mode High-Speed I/O Specifications

Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

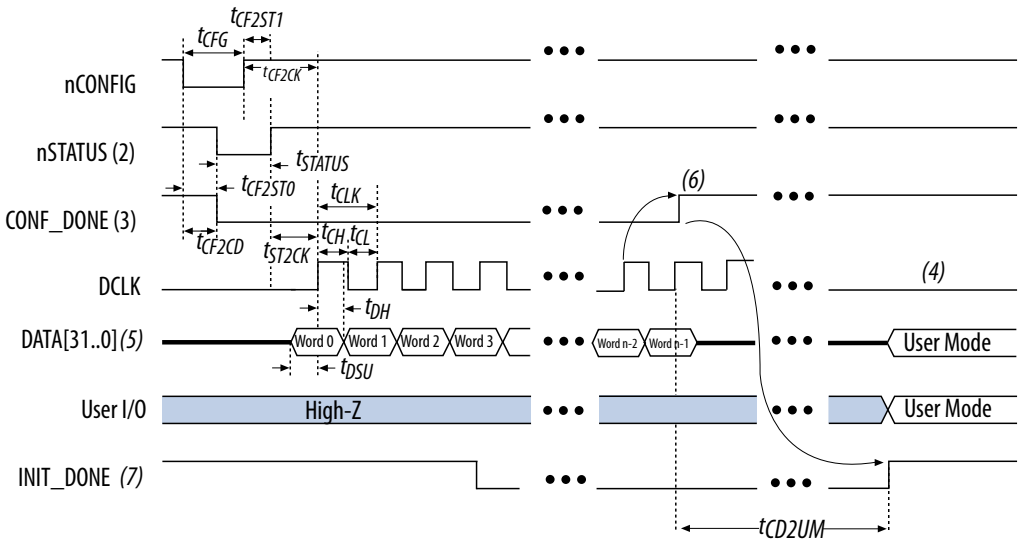
Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	± ppm

(201) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host.



Notes:
1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Date	Version	Changes
July 2014	3.8	• Updated Table 21. • Updated Table 22 V_{OCM} (DC Coupled) condition. • Updated the DCLK note to Figure 6, Figure 7, and Figure 9. • Added note to Table 5 and Table 6. • Added the DCLK specification to Table 50. • Added note to Table 51. • Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	• Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. • Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	• Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. • Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	• Added Table 23. • Updated Table 5, Table 22, Table 26, and Table 57. • Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	• Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. • Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.