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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	7362
Number of Logic Elements/Cells	156000
Total RAM Bits	11746304
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxba3d4f27c5n">https://www.e-xfl.com/product-detail/intel/5agxba3d4f27c5n</a>

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{OL}^{(14)} (mA)$	$I_{OH}^{(14)} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

### Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	$V_{CCIO} (V)$			$V_{SWING(DC)} (V)$		$V_{X(AC)} (V)$			$V_{SWING(AC)} (V)$	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

<sup>(14)</sup> To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the datasheet.

<sup>(15)</sup> The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew <sup>(39)</sup>	×N PMA bonded mode	—	—	500	—	—	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver Speed Grade 6		Unit
	Min	Max	Min	Max	
Supported data range	611	6553.6	611	3125	Mbps
fPLL supported data range	611	3125	611	3125	Mbps

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4 and 6		Unit
	Min	Max	
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

**Related Information**

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36
- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)  
Provides more information about the power supply connection for different data rates.

<sup>(39)</sup> This specification is only applicable to channels on one side of the device across two transceiver banks.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V <sub>OD</sub> Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

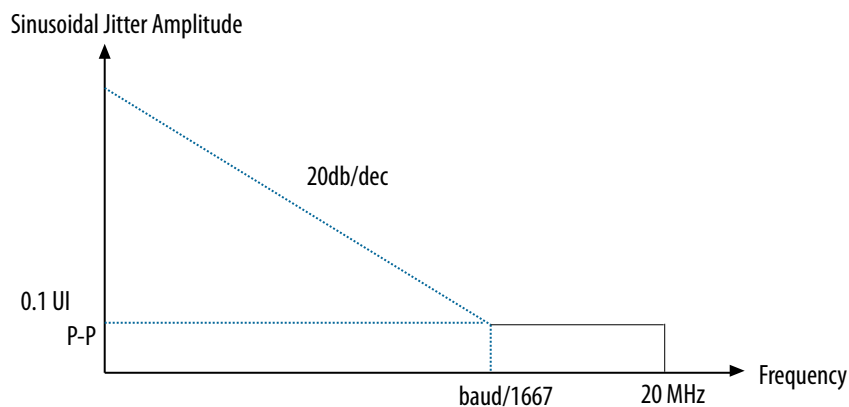
**Related Information****[SPICE Models for Altera Devices](#)**

Provides the Arria V HSSI HSPICE models.

**Transceiver Compliance Specification**

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



## DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit
DLL operating frequency range	200 – 667	200 – 667	200 – 667	MHz

## DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	-I3, -C4	-I5, -C5	-C6	Unit
2	40	80	80	ps

## Memory Output Clock Jitter Specifications

**Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices**

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

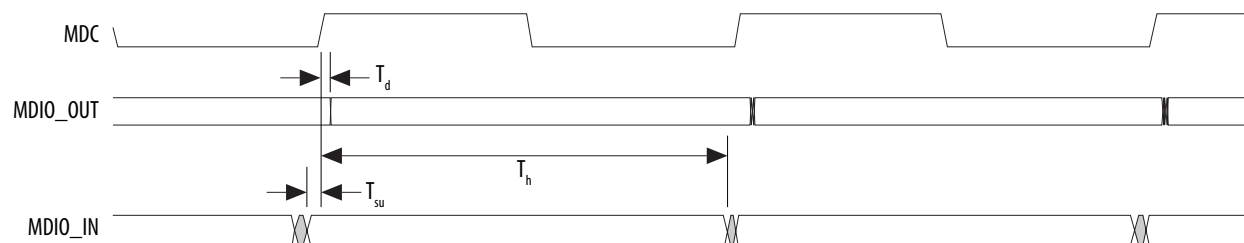
Parameter	Clock Network	Symbol	-I3, -C4		-I5, -C5		-C6		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	$t_{JIT(per)}$	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	$t_{JIT(cc)}$	63		90		94		ps

## OCT Calibration Block Specifications

**Table 1-46: OCT Calibration Block Specifications for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
$T_{OCTCAL}$	Number of OCTUSRCLK clock cycles required for $R_S$ OCT/ $R_T$ OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
$T_{RS\_RT}$	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT	—	2.5	—	ns

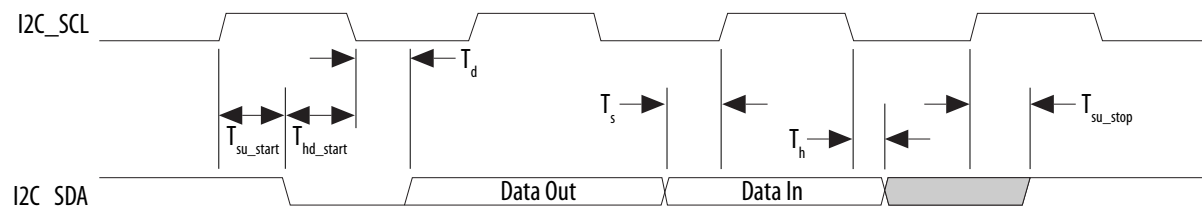
Figure 1-15: MDIO Timing Diagram



## I<sup>2</sup>C Timing Characteristics

Table 1-59: I<sup>2</sup>C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{clk}$	Serial clock (SCL) clock period	10	—	2.5	—	$\mu s$
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	$\mu s$
$T_{clklow}$	SCL low time	4	—	1.3	—	$\mu s$
$T_s$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	$\mu s$
$T_h$	Hold time for SCL to SDA data	0	3.45	0	0.9	$\mu s$
$T_d$	SCL to SDA output data delay	—	0.2	—	0.2	$\mu s$
$T_{su\_start}$	Setup time for a repeated start condition	4.7	—	0.6	—	$\mu s$
$T_{hd\_start}$	Hold time for a repeated start condition	4	—	0.6	—	$\mu s$
$T_{su\_stop}$	Setup time for a stop condition	4	—	0.6	—	$\mu s$

Figure 1-16: I<sup>2</sup>C Timing Diagram

## NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the c4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
$T_{wp}^{(89)}$	Write enable pulse width	10	—	ns
$T_{wh}^{(89)}$	Write enable hold time	7	—	ns
$T_{rp}^{(89)}$	Read enable pulse width	10	—	ns
$T_{reh}^{(89)}$	Read enable hold time	7	—	ns
$T_{clesu}^{(89)}$	Command latch enable to write enable setup time	10	—	ns
$T_{cleh}^{(89)}$	Command latch enable to write enable hold time	5	—	ns
$T_{cesu}^{(89)}$	Chip enable to write enable setup time	15	—	ns
$T_{ceh}^{(89)}$	Chip enable to write enable hold time	5	—	ns
$T_{alesu}^{(89)}$	Address latch enable to write enable setup time	10	—	ns
$T_{aleh}^{(89)}$	Address latch enable to write enable hold time	5	—	ns
$T_{dsu}^{(89)}$	Data to write enable setup time	10	—	ns

<sup>(89)</sup> Timing of the NAND interface is controlled through the NAND configuration registers.



Variant	Member Code	Active Serial <sup>(108)</sup>			Fast Passive Parallel <sup>(109)</sup>		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

**Related Information****Configuration Files** on page 1-83<sup>(108)</sup> DCLK frequency of 100 MHz using external CLKUSR.<sup>(109)</sup> Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
July 2014	3.8	<ul style="list-style-type: none"> <li>Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.</li> <li>Updated <math>V_{CC\_HPS}</math> specification in Table 5.</li> <li>Added a note in Table 19: Differential inputs are powered by <math>V_{CCPD}</math> which requires 2.5 V.</li> <li>Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21.</li> <li>Updated description in "HPS PLL Specifications" section.</li> <li>Updated VCO range maximum specification in Table 39.</li> <li>Updated <math>T_d</math> and <math>T_h</math> specifications in Table 45.</li> <li>Added <math>T_h</math> specification in Table 47 and Figure 13.</li> <li>Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.</li> <li>Removed "Remote update only in AS mode" specification in Table 58.</li> <li>Added DCLK device initialization clock source specification in Table 60.</li> <li>Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.</li> <li>Removed <math>f_{MAX\_RU\_CLK}</math> specification in Table 63.</li> </ul>
February 2014	3.7	<ul style="list-style-type: none"> <li>Updated <math>V_{CCRSTCLK\_HPS}</math> maximum specification in Table 1.</li> <li>Added <math>V_{CC\_AUX\_SHARED}</math> specification in Table 1.</li> </ul>
December 2013	3.6	<ul style="list-style-type: none"> <li>Added "HPS PLL Specifications".</li> <li>Added Table 24, Table 39, and Table 40.</li> <li>Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59.</li> <li>Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19.</li> <li>Removed table: GPIO Pulse Width for Arria V Devices.</li> </ul>

Date	Version	Changes
November 2012	3.0	<ul style="list-style-type: none"> <li>Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.</li> <li>Removed table: Transceiver Block Jitter Specifications for Arria V Devices.</li> <li>Added HPS information: <ul style="list-style-type: none"> <li>Added “HPS Specifications” section.</li> <li>Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.</li> <li>Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.</li> <li>Updated Table 3 and Table 5.</li> </ul> </li> </ul>
October 2012	2.4	<ul style="list-style-type: none"> <li>Updated Arria V GX <math>V_{CCR\_GXBL/R}</math>, <math>V_{CCT\_GXBL/R}</math>, and <math>V_{CCL\_GXBL/R}</math> minimum and maximum values, and data rate in Table 4.</li> <li>Added receiver <math>V_{ICM}</math> (AC coupled) and <math>V_{ICM}</math> (DC coupled) values, and transmitter <math>V_{OCM}</math> (AC coupled) and <math>V_{OCM}</math> (DC coupled) values in Table 20 and Table 21.</li> </ul>
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	<ul style="list-style-type: none"> <li>Updated the maximum voltage for <math>V_I</math> (DC input voltage) in Table 1.</li> <li>Updated Table 20 to include the Arria V GX -I3 speed grade.</li> <li>Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.</li> <li>Updated the SERDES factor condition in Table 30.</li> <li>Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.</li> </ul>
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$ , $V_{CCT\_GXBL/R}$ , and $V_{CCL\_GXBL/R}$ values in Table 4.

Symbol	Description	Condition	Minimum <sup>(114)</sup>	Typical	Maximum <sup>(114)</sup>	Unit
V <sub>I</sub>	DC input voltage	—	−0.5	—	3.6	V
V <sub>O</sub>	Output voltage	—	0	—	V <sub>CCIO</sub>	V
T <sub>J</sub>	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

### Recommended Transceiver Power Supply Operating Conditions

**Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices**

Symbol	Description	Minimum <sup>(118)</sup>	Typical	Maximum <sup>(118)</sup>	Unit
V <sub>CCA_GXBL</sub> (119), (120)	Transceiver channel PLL power supply (left side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V <sub>CCA_GXBR</sub> (119), (120)	Transceiver channel PLL power supply (right side)	2.85	3.0	3.15	V
		2.375	2.5	2.625	
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side)	0.82	0.85	0.88	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side)	0.82	0.85	0.88	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side)	0.82	0.85	0.88	V

<sup>(114)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(118)</sup> This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(119)</sup> This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

<sup>(120)</sup> When using ATX PLLs, the supply must be 3.0 V.

## Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB <sup>(122)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: <ul style="list-style-type: none"> <li>Data rate &gt; 10.3 Gbps.</li> <li>DFE is used.</li> </ul>	1.05	3.0	1.5	V
If ANY of the following conditions are true <sup>(123)</sup> : <ul style="list-style-type: none"> <li>ATX PLL is used.</li> <li>Data rate &gt; 6.5Gbps.</li> <li>DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.</li> </ul>	1.0			
If ALL of the following conditions are true: <ul style="list-style-type: none"> <li>ATX PLL is not used.</li> <li>Data rate ≤ 6.5Gbps.</li> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>	0.85	2.5		

## DC Characteristics

## Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

<sup>(122)</sup> If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to 0.85 V, they can be shared with the VCC core supply.

<sup>(123)</sup> Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100-Ω setting)	V <sub>CCIO</sub> = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{\text{OCT}} = R_{\text{SCAL}} \left( 1 + \left( \frac{dR}{dT} \times \Delta T \right) \pm \left( \frac{dR}{dV} \times \Delta V \right) \right)$$

Notes:

1. The R<sub>OCT</sub> value shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
2. R<sub>SCAL</sub> is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
5. dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
6. dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V<sub>CCIO</sub> range of ±5% and a temperature range of 0° to 85°C.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
$V_{ICM}$ (AC and DC coupled)	$V_{CCR\_GXB} = 0.85\text{ V}$ full bandwidth	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 0.85\text{ V}$ half bandwidth	—	600	—	—	600	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}$ full bandwidth	—	700	—	—	700	—	mV
	$V_{CCR\_GXB} = 1.0\text{ V}$ half bandwidth	—	700	—	—	700	—	mV
$t_{LTR}^{(149)}$	—	—	—	10	—	—	10	$\mu\text{s}$
$t_{LTD}^{(150)}$	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTD\_manual}^{(151)}$	—	4	—	—	4	—	—	$\mu\text{s}$
$t_{LTR\_LTD\_manual}^{(152)}$	—	15	—	—	15	—	—	$\mu\text{s}$
Programmable equalization (AC Gain)	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	dB

<sup>(149)</sup>  $t_{LTR}$  is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

<sup>(150)</sup>  $t_{LTD}$  is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

<sup>(151)</sup>  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.

<sup>(152)</sup>  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data rate range	VCO post-divider L = 2	8000	—	12500	8000	—	10312.5	Mbps
	L = 4	4000	—	6600	4000	—	6600	Mbps
	L = 8 <sup>(155)</sup>	2000	—	3300	2000	—	3300	Mbps
t <sub>pll_powerdown</sub> <sup>(156)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(157)</sup>	—	—	—	10	—	—	10	μs

#### Related Information

- [Arria V Device Overview](#)  
For more information about device ordering codes.
- [Transceiver Clocking in Arria V Devices](#)  
For more information about clocking ATX PLLs.
- [Dynamic Reconfiguration in Arria V Devices](#)  
For more information about reconfiguring ATX PLLs.

## Fractional PLL

**Table 2-28: Fractional PLL Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

<sup>(155)</sup> This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.

<sup>(156)</sup> t<sub>pll\_powerdown</sub> is the PLL powerdown minimum pulse width.

<sup>(157)</sup> t<sub>pll\_lock</sub> is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.



## Core Performance Specifications

### Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

Symbol	Performance		Unit
	C3, I3L	C4, I4	
Global and Regional Clock	650	580	MHz
Periphery Clock	500	500	MHz

### PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

Symbol	Parameter	Min	Typ	Max	Unit
$f_{IN}^{(167)}$	Input clock frequency (C3, I3L speed grade)	5	—	800	MHz
	Input clock frequency (C4, I4 speed grade)	5	—	650	MHz
$f_{INPFD}$	Input frequency to the PFD	5	—	325	MHz
$f_{FINPFD}$	Fractional Input clock frequency to the PFD	50	—	160	MHz
$f_{VCO}^{(168)}$	PLL VCO operating range (C3, I3L speed grade)	600	—	1600	MHz
	PLL VCO operating range (C4, I4 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%

<sup>(167)</sup> This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

<sup>(168)</sup> The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.

Description	Min	Typ	Max	Unit
Diode ideality factor	1.006	1.008	1.010	—

## Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

**Note:** The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

## High-Speed I/O Specification

### High-Speed Clock Specifications

**Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
4	120	128	ps

## Memory Output Clock Jitter Specifications

**Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices**

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

Clock Network	Parameter	Symbol	C3, I3L		C4, I4		Unit
			Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	-55	55	-55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-82.5	82.5	-82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	-82.5	82.5	-82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-90	90	-90	90	ps
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-45	45	-56	56	ps

## Duty Cycle Distortion (DCD) Specifications

**Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins**

The DCD numbers do not cover the core clock network.

Symbol	C3, I3L		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

## Configuration Specification

### POR Specifications

**Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices**

Select the POR delay based on the MSEL setting as described in the “Configuration Schemes for Arria V Devices” table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 <sup>(202)</sup>
Standard	100	300

#### Related Information

[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

<sup>(202)</sup> The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Term	Definition
$V_{OCM}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
$V_{OD}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
$V_{SWING}$	Differential input voltage
$V_X$	Input differential cross point voltage
$V_{OX}$	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

## Document Revision History

Date	Version	Changes
February 2017	2017.02.10	<ul style="list-style-type: none"> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table.</li> <li>Changed the minimum value for <math>t_{CD2UMC}</math> in the "PS Timing Parameters for Arria V GZ Devices" table.</li> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.</li> </ul>