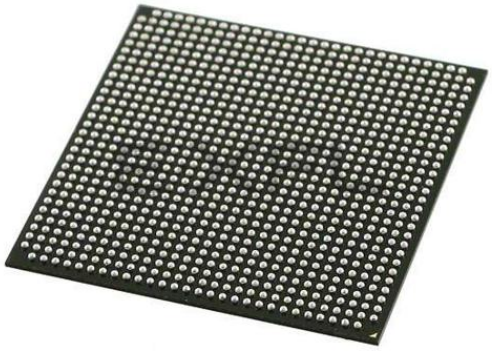

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	7362
Number of Logic Elements/Cells	156000
Total RAM Bits	11746304
Number of I/O	416
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba3d4f31i5n

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Arria V GX, GT, SX, and ST Device Datasheet

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2017.02.10

AV-51002

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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

Related Information

Arria V Device Overview
Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-125	1.19	1.25	1.31	0.18	(15)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.3	$V_{CCIO} + 0.48$
HSUL-12	1.14	1.2	1.3	0.26	0.26	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$	0.44	0.44

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal(41)	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300(42)/2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—	—	1.2	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.
(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Data rate (10-Gbps transceiver)(44)	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin(45)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins(46)	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	750(47)/800	—	mV
V_{ICM} (DC coupled)	≤ 3.2Gbps(48)	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	85			Ω
	100-Ω setting	100			Ω
	120-Ω setting	120			Ω
	150-Ω setting	150			Ω
t_{LTR}(49)	—	—	—	10	µs
t_{LTD}(50)	—	4	—	—	µs

(45) The device cannot tolerate prolonged operation at this absolute maximum.
(46) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
(47) The AC coupled V_{ICM} is 750 mV for PCIe mode only.
(48) For standard protocol compliance, use AC coupling.
(49) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
(50) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V_{OD} Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

Related Information

SPICE Models for Altera Devices
Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Protocol	Sub-protocol	Data Rate (Mbps)
Common Public Radio Interface (CPRI)	CPRI E6LV	614.4
	CPRI E6HV	614.4
	CPRI E6LVII	614.4
	CPRI E12LV	1,228.8
	CPRI E12HV	1,228.8
	CPRI E12LVII	1,228.8
	CPRI E24LV	2,457.6
	CPRI E24LVII	2,457.6
	CPRI E30LV	3,072
	CPRI E30LVII	3,072
	CPRI E48LVII	4,915.2
	CPRI E60LVII	6,144
	CPRI E96LVIII(60)	9,830.4
Gbps Ethernet (GbE)	GbE 1250	1,250
OBSAI	OBSAI 768	768
	OBSAI 1536	1,536
	OBSAI 3072	3,072
	OBSAI 6144	6,144
Serial digital interface (SDI)	SDI 270 SD	270
	SDI 1485 HD	1,485
	SDI 2970 3G	2,970

(60) You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

Symbol	Condition	–I3, –C4			–I5, –C5			–C6			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	SERDES factor J ≥ 8[76][78], LVDS TX with RX DPA	[77]	—	1600	[77]	—	1500	[77]	—	1250	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	[77]	—	[79]	[77]	—	[79]	[77]	—	[79]	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	945	[77]	—	945	[77]	—	945	Mbps
Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate)[80]	SERDES factor J = 4 to 10[81]	[77]	—	200	[77]	—	200	[77]	—	200	Mbps
$t_{x\ Jitter}$ -True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps – 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

(78) The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.
(79) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.
(80) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(81) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

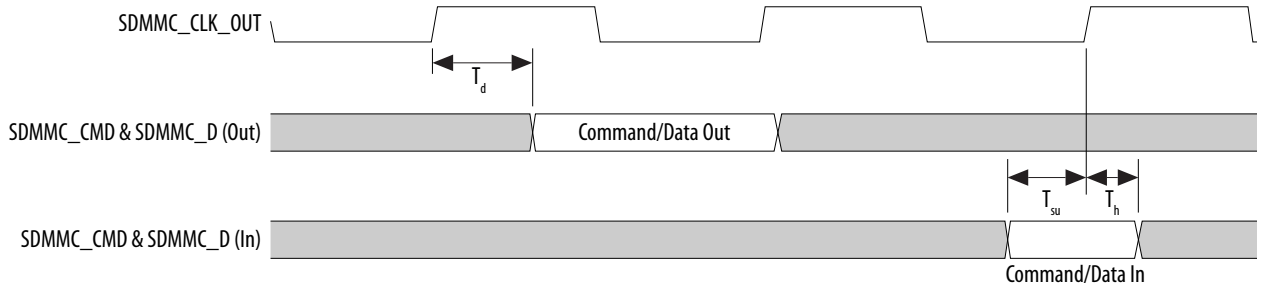
After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
T_{sdmmc_clk} (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{sdmmc\_clk\_out}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{dutycycle}$	SDMMC_CLK_OUT duty cycle	45	55	%
T_d	SDMMC_CMD/SDMMC_D output delay	(T_{sdmmc_clk} × `drvsel`)/2 – 1.23 (87)	(T_{sdmmc_clk} × `drvsel`)/2 + 1.69 (87)	ns
T_{su}	Input setup time	1.05 – (T_{sdmmc_clk} × `smplsel`)/2 (88)	—	ns
T_h	Input hold time	(T_{sdmmc_clk} × `smplsel`)/2 (88)	—	ns

(87) `drvsel` is the drive clock phase shift select value.
(88) `smplsel` is the sample clock phase shift select value.

Figure 1-11: SD/MMC Timing Diagram



Related Information

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

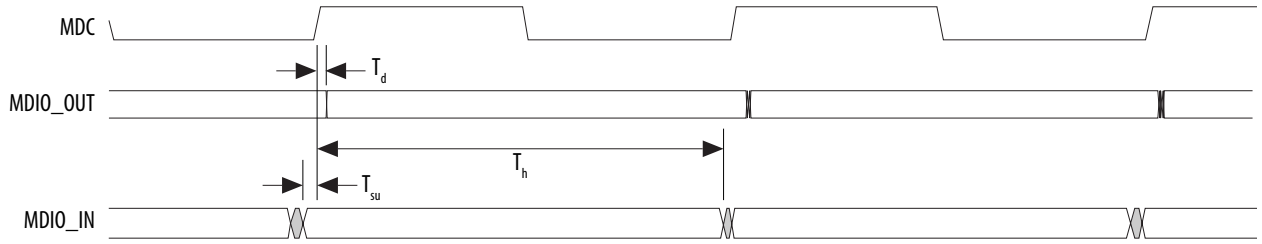
USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

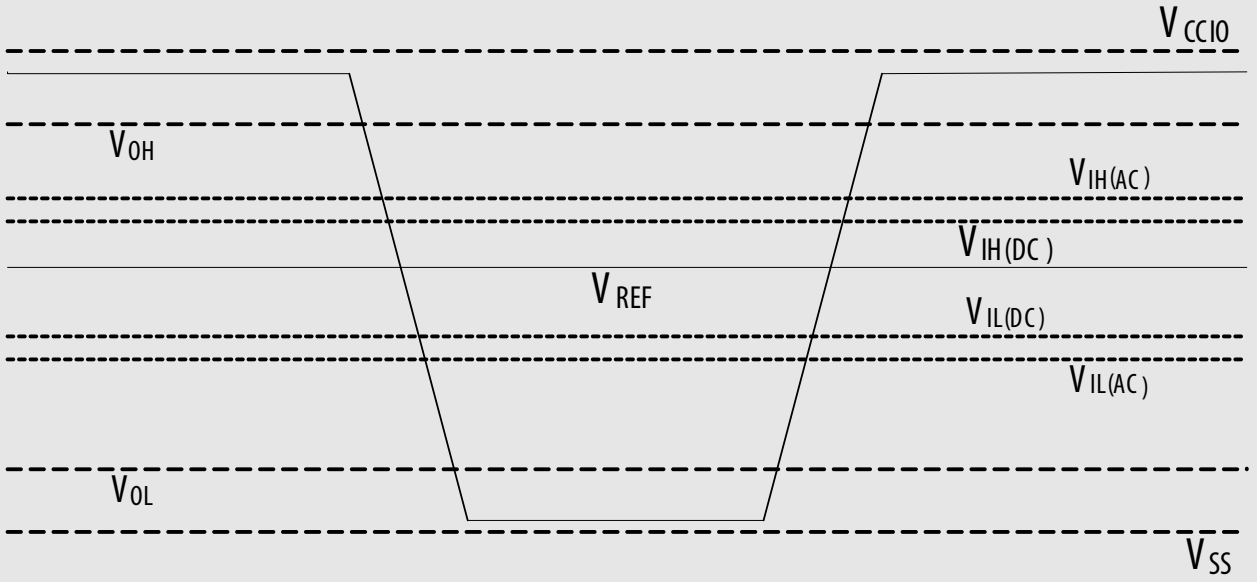
Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
$T_{clkhigh}$	SCL high time	4.7	—	0.6	—	µs
T_{clklow}	SCL low time	4	—	1.3	—	µs
T_s	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
T_h	Hold time for SCL to SDA data	0	3.45	0	0.9	µs
T_d	SCL to SDA output data delay	—	0.2	—	0.2	µs
T_{su_start}	Setup time for a repeated start condition	4.7	—	0.6	—	µs
T_{hd_start}	Hold time for a repeated start condition	4	—	0.6	—	µs
T_{su_stop}	Setup time for a stop condition	4	—	0.6	—	µs

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard 
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{OCT} = R_{SCAL}\left(1 + \left(\frac{dR}{dT} \times \triangle T\right) \pm \left(\frac{dR}{dV} \times \triangle V\right)\right)$$

Notes:
1. The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
2. R_{SCAL} is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
5. dR/dT is the percentage change of R_{SCAL} with temperature.
6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (124)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver pin	50 mA

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

Symbol	Description	V_{CCIO} Conditions (V) (125)	Value (126)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	k Ω
		2.5 ±5%	25	k Ω
		1.8 ±5%	25	k Ω
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	k Ω
		1.25 ±5%	25	k Ω
		1.2 ±5%	25	k Ω

(124) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.
(125) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
(126) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 × V_{CCIO} – 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} + 0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}	0.44	0.44

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V) (128)			V_{ID} (mV) (129)			$V_{ICM(DC)}$ (V)			V_{OD} (V) (130)			V_{OCM} (V) (130)		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section.														
2.5 V LVDS (131)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	D_{MAX} ≤ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D_{MAX} > 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS (132)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—

(128) Differential inputs are powered by VCCPD which requires 2.5 V.
(129) The minimum VID value is applicable over the entire common mode range, VCM.
(130) RL range: 90 ≤ RL ≤ 110 Ω.
(131) For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.
(132) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

Symbol	Parameter	Min	Typ	Max	Unit
f_{OUT} (169)	Output frequency for an internal global or regional clock (C3, I3L speed grade)	—	—	650	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grade)	—	—	580	MHz
f_{OUT_EXT} (169)	Output frequency for an external clock output (C3, I3L speed grade)	—	—	667	MHz
	Output frequency for an external clock output (C4, I4 speed grade)	—	—	533	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (170)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns

(169) This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.
(170) High bandwidth PLL settings are not supported in external feedback mode.

Memory	Mode	Resources Used		Performance				Unit
		ALUTs	Memory	C3	C4	I3L	I4	
M20K Block	Single-port, all supported widths	0	1	650	550	500	450	MHz
	Simple dual-port, all supported widths	0	1	650	550	500	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	455	400	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	400	350	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	500	450	500	450	MHz
	True dual port, all supported widths	0	1	650	550	500	450	MHz
	ROM, all supported widths	0	1	650	550	500	450	MHz

Temperature Sensing Diode Specifications

Table 2-37: Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 kHz	< 100 ms	8 bits	8 bits

Table 2-38: External Temperature Sensing Diode Specifications for Arria V GZ Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	µA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω

Duty Cycle Distortion (DCD) Specifications

Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

Symbol	C3, I3L		C4, I4		Unit
	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	%

Configuration Specification

POR Specifications

Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

POR Delay	Minimum (ms)	Maximum (ms)
Fast	4	12 (202)
Standard	100	300

Related Information

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

(202) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	• Changed the minimum value for t_{CD2UMC} in the “FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1” table. • Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. • Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. • Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. • Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.