





Welcome to <u>E-XFL.COM</u>

Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba5d4f31c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1-5

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V	Core voltage power supply	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V _{CC}	Core voltage power suppry	-I3	1.12	1.15	1.18	V
V	Periphery circuitry, PCIe hard IP block,	-C4, -I5, -C5, -C6	1.07	1.1	1.13	V
V CCP	and transceiver PCS power supply	-I3	1.12	1.15	1.18	V
		3.3 V	3.135	3.3	3.465	V
V	Configuration pins power supply	3.0 V	2.85	3.0	3.15	V
V CCPGM		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V _{CC_AUX}	Auxiliary supply	_	2.375	2.5	2.625	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply	_	1.2	—	3.0	V
	(For design security volatile key register)					
		3.3 V	3.135	3.3	3.465	V
V _{CCPD} ⁽³⁾	I/O pre-driver power supply	3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} is not powered up.



⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Transceiver Power Supply Operating Conditions

Table '	1-4:	Transceiver	Power S	upply	Operating	Conditions	for Arria V Devices	j
---------	------	-------------	---------	-------	-----------	------------	---------------------	---

Symbol	Description	Minimum ⁽⁵⁾	Typical	Maximum ⁽⁵⁾	Unit
V _{CCA_GXBL}	Transceiver high voltage power (left side)	2 275	2 500	2 625	V
V _{CCA_GXBR}	Transceiver high voltage power (right side)	2.575	2.300	2.025	v
V _{CCR_GXBL}	GX and SX speed grades—receiver power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCR_GXBR}	GX and SX speed grades—receiver power (right side)	1.00/1.12	1.1/1.13	1.14/1.10	v
V _{CCR_GXBL}	GT and ST speed grades—receiver power (left side)	1 17	1 20	1 23	V
V _{CCR_GXBR}	GT and ST speed grades—receiver power (right side)	1.17	1.20	1.20	v
V _{CCT_GXBL}	GX and SX speed grades—transmitter power (left side)	1.08/1.12	1 1/1 15(6)	1 14/1 18	V
V _{CCT_GXBR}	GX and SX speed grades—transmitter power (right side)	1.00/1.12	1.1/1.15	1.14/1.10	v
V _{CCT_GXBL}	GT and ST speed grades—transmitter power (left side)	1 17	1 20	1 23	V
V _{CCT_GXBR}	GT and ST speed grades—transmitter power (right side)	1.17	1.20	1.23	v
V _{CCH_GXBL}	Transmitter output buffer power (left side)	1 /25	1 500	1 575	V
V _{CCH_GXBR}	Transmitter output buffer power (right side)	1.423	1.300	1.375	v

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate <=3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.



Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

1/O Standard	VII	_{-(DC)} (V)	V _{IH(D}	_{C)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	I _{OL} ⁽¹⁴⁾	(14)(mA)
	Min	Max	Min	Мах	Max	Min	Мах	Min	(mA)	IOH. (IIIIM)
SSTL-2 Class I	-0.3	V _{REF} - 0.15	V _{REF} + 0.15	$V_{CCIO} + 0.3$	V _{REF} - 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	$V_{CCIO} + 0.3$	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} - 0.125	V _{REF} + 0.125	$V_{CCIO} + 0.3$	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	$V_{CCIO} + 0.3$	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCIO} – 0.28	13.4	-13.4
SSTL-15 Class I	—	V _{REF} – 0.1	$V_{REF} + 0.1$	_	V _{REF} - 0.175	V _{REF} + 0.175	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	V _{REF} – 0.1	$V_{REF} + 0.1$	—	V _{REF} - 0.175	V _{REF} + 0.175	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135	—	V _{REF} - 0.09	$V_{REF} + 0.09$	_	V _{REF} - 0.16	$V_{REF} + 0.16$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$		
SSTL-125	—	V _{REF} - 0.85	$V_{REF} + 0.85$	—	V _{REF} - 0.15	$V_{REF} + 0.15$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$		
HSTL-18 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.2	$V_{REF} + 0.2$	0.4	V _{CCIO} – 0.4	16	-16
HSTL-15 Class I	_	V _{REF} – 0.1	$V_{REF} + 0.1$		V _{REF} – 0.2	V _{REF} + 0.2	0.4	$V_{CCIO} - 0.4$	8	-8



⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Table 1-38: Memory Block Performance Specifications for Arria V Devices

Momory	Mada	Resources Used		Performance			Unit	
Memory	Mode	ALUTs	Memory	-I3, -C4	-I5, -C5	-C6	Ont	
	Single port, all supported widths	0	1	500	450	400	MHz	
	Simple dual-port, all supported widths	0	1	500	450	400	MHz	
MLAB	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz	
	ROM, all supported width	_		500	450	400	MHz	
	Single-port, all supported widths	0	1	400	350	285	MHz	
	Simple dual-port, all supported widths	0	1	400	350	285	MHz	
M10K Block	Simple dual-port with the read-during- write option set to Old Data , all supported widths	0	1	315	275	240	MHz	
	True dual port, all supported widths	0	1	400	350	285	MHz	
	ROM, all supported widths	0	1	400	350	285	MHz	

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

Maximum input jitter = Input clock period × Divide value (N) × 0.02

Table 1-50: Examples of Maximum Input Jitter

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

Quad SPI Flash Timing Characteristics

Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
F _{clk}	SCLK_OUT clock frequency (External clock)	_	_	108	MHz
T _{qspi_clk}	QSPI_CLK clock period (Internal reference clock)	2.32			ns
T _{dutycycle}	SCLK_OUT duty cycle	45		55	%
T _{dssfrst}	Output delay QSPI_SS valid before first clock edge		1/2 cycle of SCLK_OUT		ns
T _{dsslst}	Output delay QSPI_SS valid after last clock edge	-1		1	ns
T _{dio}	I/O data output delay	-1		1	ns
T _{din_start}	Input data valid start			$(2 + R_{delay}) \times T_{qspi_clk} - 7.52^{(85)}$	ns



Figure 1-10: SPI Slave Timing Diagram



Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses drvsel = 3 and smplsel = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.



Symbol	Description	Min	Max	Unit
$T_{dh}^{(89)}$	Data to write enable hold time	5	—	ns
T _{cea}	Chip enable to data access time		25	ns
T _{rea}	Read enable to data access time		16	ns
T _{rhz}	Read enable to data high impedance		100	ns
T _{rr}	Ready to read enable low	20	—	ns

Figure 1-17: NAND Command Latch Timing Diagram





HPS JTAG Timing Specifications

Symbol	Description	Min	Max	Unit
t _{JCP}	TCK clock period	30	_	ns
t _{JCH}	TCK clock high time	14		ns
t _{JCL}	TCK clock low time	14		ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2		ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3		ns
t _{JPH}	JTAG port hold time	5		ns
t _{JPCO}	JTAG port clock to output		12 ⁽⁹⁰⁾	ns
t _{JPZX}	JTAG port high impedance to valid output		14 ⁽⁹⁰⁾	ns
t _{JPXZ}	JTAG port valid output to high impedance		14 ⁽⁹⁰⁾	ns

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 ⁽⁹¹⁾	ms

⁽⁹⁰⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

⁽⁹¹⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.



1-80 AS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$ DCLK period	—	—
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)		
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

FPP Configuration Timing

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

Symbol	Parameter	Minimum	Maximum	Unit
t _{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t _{SU}	Data setup time before the falling edge on DCLK	1.5		ns
t _{DH}	Data hold time after the falling edge on DCLK	0	_	ns
t _{CD2UM}	CONF_DONE high to user mode	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + ($T_{init} \times CLKUSR$ period)	_	—
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles



Sumbol	Description	Conditions	Resistance	Unit	
Symbol	Description	Conditions	C3, I3L	C4, I4	onic
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8 and 1.5 V	±40	±40	%
25-Ω R _S	Internal series termination without calibration (25- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±40	±40	%
50-Ω R _S	Internal series termination without calibration (50- Ω setting)	$V_{CCIO} = 1.2 V$	±50	±50	%
100-Ω R _D	Internal differential termination (100- Ω setting)	$V_{CCIO} = 2.5 V$	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$\mathbf{R}_{\text{OCT}} = \mathbf{R}_{\text{SCAL}} \left(1 + \left(\frac{dR}{dT} \times \bigtriangleup T \right) \pm \left(\frac{dR}{dV} \times \bigtriangleup V \right) \right)$$

Notes:

1. The R_{oct} value shows the range of OCT resistance with the variation of temperature and V_{ccio} . 2. R_{scAL} is the OCT resistance value at power-up. 3. ΔT is the variation of temperature with respect to the temperature at power-up. 4. ΔV is the variation of voltage with respect to the V_{ccio} at power-up. 5. dR/dT is the percentage change of R_{scAL} with temperature. 6. dR/dV is the percentage change of R_{scAL} with voltage

6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V_{CCIO} range of \pm 5% and a temperature range of 0° to 85°C.





	V _{IL(D}	_{C)} (V)	$V_{\rm IH(DC)}(V) \qquad V_{\rm IL(AC)}(V) \qquad V_{\rm IH(AC)}(V) \qquad V_{\rm IH(AC$	V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	Ι (L (mA)		
I/O Standard	Min	Max	Min	Max	Мах	Min	Max	Min	i _{ol} (mA)	i _{oh} (mA)
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	$V_{REF} + 0.25$	0.28	V _{CCIO} – 0.28	13.4	-13.4
SSTL-15 Class I		V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{\rm CCIO}$	$0.8 \times V_{ m CCIO}$	8	-8
SSTL-15 Class II	—	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.175	V _{REF} + 0.175	$0.2 \times V_{\rm CCIO}$	$0.8 \times V_{ m CCIO}$	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	—
SSTL-125 Class I, II	_	V _{REF} – 0.85	V _{REF} + 0.85	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	_	_
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCIO}	0.8 * V _{CCIO}	—	_
HSTL-18 Class I		V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	$V_{\rm CCIO}$ – 0.4	8	-8
HSTL-18 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} - 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	16	-16
HSTL-15 Class I	—	V _{REF} – 0.1	V _{REF} + 0.1	—	V _{REF} – 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	8	-8
HSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.2	V _{REF} + 0.2	0.4	V _{CCIO} – 0.4	16	-16
HSTL-12 Class I	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{ m CCIO}$	$0.75 \times V_{ m CCIO}$	8	-8
HSTL-12 Class II	-0.15	V _{REF} – 0.08	V _{REF} + 0.08	V _{CCIO} + 0.15	V _{REF} – 0.15	V _{REF} + 0.15	$0.25 \times V_{\rm CCIO}$	$0.75 \times V_{\rm CCIO}$	16	-16
HSUL-12		V _{REF} – 0.13	V _{REF} + 0.13	_	V _{REF} – 0.22	V_{REF} + 0.22	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	_	

Arria V GZ Device Datasheet

Altera Corporation



1/O Standard	۷ _C	_{CIO} (V) ⁽	(128)		V _{ID} (mV) ⁽¹²⁹⁾		V _{ICM(DC)} (V)		$V_{ICM(DC)}(V)$ $V_{OD}(V)^{(130)}$		⁽¹³⁰⁾ V _{OCM} (V) ⁽¹³⁰⁾		30)		
	Min	Тур	Мах	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Мах
RSDS (HIO) (133)	2.375	2.5	2.625	100	V _{CM} = 1.25 V		0.3		1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini- LVDS (HIO) (134)	2.375	2.5	2.625	200	_	600	0.4	_	1.325	0.25		0.6	1	1.2	1.4
LVPECL		_	_	300		_	0.6	D _{MAX} ≤ 700 Mbps	1.8	_	_		_		
(135), (136)	_	_	_	300			1	D _{MAX} > 700 Mbps	1.6	_	_		_		

Related Information

Glossary on page 2-73



⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.

⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.

RL range: $90 \le RL \le 110 \Omega$. (130)

⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.

⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Symbol	Parameter	Min	Тур	Max	Unit
t (171) (172)	Input clock cycle-to-cycle jitter (f_{REF} $\geq 100~MHz)$	—	—	0.15	UI (p-p)
'INCCJ',	Input clock cycle-to-cycle jitter ($f_{REF} < 100 \text{ MHz}$)	-750		+750	ps (p-p)
tourny p.c. ⁽¹⁷³⁾	Period Jitter for dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)			175	ps (p-p)
toutpj_dc ⁽¹⁷³⁾	Period Jitter for dedicated clock output in integer PLL (f _{OUT} < 100 Mhz)	_		17.5	mUI (p-p)
t (173)	Period Jitter for dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f _{OUT} < 100 MHz)	_		$25^{(176)},$ 17.5 ⁽¹⁷⁴⁾	mUI (p-p)
t	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT} \ge 100 \text{ MHz}$)	_	_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL (f _{OUT} < 100 MHz)	_		17.5	mUI (p-p)
t (173)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} \ge 100 \text{ MHz}$)	—		250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
^t FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT} < 100 \text{ MHz}$)			$25^{(176)}, \\ 17.5^{(174)}$	mUI (p-p)

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps. ⁽¹⁷²⁾ The f_{REF} is fIN/N specification applies when N = 1.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be \geq 1200 MHz.



⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10⁻¹² (14 sigma, 99.999999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

Symbol	Conditions	C3, I3L			C4, I4			Unit	
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Onit	
f _{HSCLK_in} (input clock frequency) True Differential I/O Standards ⁽¹⁷⁹⁾	Clock boost factor W = 1 to 40 $^{(180)}$	5	_	625	5	_	525	MHz	
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		625	5		525	MHz	
f _{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(180)}$	5		420	5		420	MHz	
f _{HSCLK_OUT} (output clock frequency)	—	5		625 (181)	5		525 (181)	MHz	

Transmitter High-Speed I/O Specifications

Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



 $^{^{(179)}\,}$ This only applies to DPA and soft-CDR modes.

⁽¹⁸⁰⁾ Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

⁽¹⁸¹⁾ This is achieved by using the LVDS clock network.

Symbol	Conditions	C3, I3L				Unit		
Symbol	Conditions	Min	Тур	Мах	Min	Тур	Max	Unit
t _{x Jitter} - True Differential I/O	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		160		—	160	ps
Standards	Total Jitter for Data Rate < 600 Mbps	—		0.1		_	0.1	UI
t _{x Jitter} - Emulated Differential I/O Standards with Three	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—		300		—	325	ps
External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	—		0.2		—	0.25	UI
t _{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	%
	True Differential I/O Standards	_		200		—	200	ps
t _{RISE} & t _{FALL}	Emulated Differential I/O Standards with three external output resistor networks			250		_	300	ps
	True Differential I/O Standards			150		—	150	ps
TCCS	Emulated Differential I/O Standards	_	_	300		_	300	ps

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.



DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Тур	Мах	Min	Тур	Мах	
DPA run length	—	_	_	10000	_		10000	UI

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾	Maximum
SPI-4	0000000001111111111	2	128	640 data transitions



⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification

Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Free	Sinusoidal Jitter (UI)	
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350



DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 - 890	300 - 890	MHz

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$.

Speed Grade	Min	Мах	Unit	
C3, I3L	8	15	ps	
C4, I4	8	16	ps	

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -3 speed grade is ± 84 ps or ± 42 ps.

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

Symbol	Parameter	Minimum	Maximum	Unit
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times maximum$	—	_
		DCLK period		
t _{CD2UM} C	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) (209)		_

Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 2-57 ٠
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Arria V GZ Device Datasheet

Altera Corporation



⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

Term				Definition			
R _L	Receiver differential input discrete resistor (external to the Arria V GZ device).						
SW (sampling window)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:						
	Bit Time						
		0.5 x TCCS	RSKM	Sampling Window (SW)	RSKM	0.5 x TCCS	
Single-ended voltage referenced I/O standard	 The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing: Single-Ended Voltage Referenced I/O Standard 						
		V _{0H}		V REF	Viн(DC Vil(DC)	V <u>ccio</u> VIH(AC) VIL(AC) VIL(AC)	

