Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	8962
Number of Logic Elements/Cells	190000
Total RAM Bits	13284352
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba5d4f35i5n

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Data rate (10-Gbps transceiver)[44]	—	0.611	—	10.3125	Gbps
Absolute V_{MAX} for a receiver pin[45]	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	−0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins[46]	—	100	—	—	mV
V_{ICM} (AC coupled)	—	—	750[47]/800	—	mV
V_{ICM} (DC coupled)	≤ 3.2Gbps[48]	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	85			Ω
	100-Ω setting	100			Ω
	120-Ω setting	120			Ω
	150-Ω setting	150			Ω
t_{LTR}[49]	—	—	—	10	μs
t_{LTD}[50]	—	4	—	—	μs

[45] The device cannot tolerate prolonged operation at this absolute maximum.

[46] The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

[47] The AC coupled V_{ICM} is 750 mV for PCIe mode only.

[48] For standard protocol compliance, use AC coupling.

[49] t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

[50] t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.
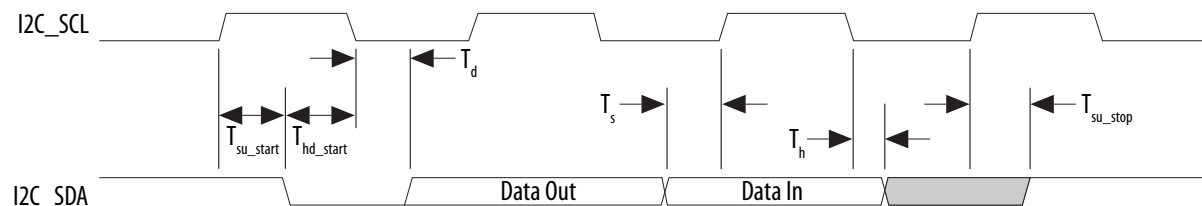
Typical TX V$_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX V$_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω

Symbol	V$_{OD}$ Setting[58]	V$_{OD}$ Value (mV)	V$_{OD}$ Setting[58]	V$_{OD}$ Value (mV)
	6[59]	120	34	680
	7[59]	140	35	700
	8[59]	160	36	720
	9	180	37	740
	10	200	38	760
	11	220	39	780
	12	240	40	800
	13	260	41	820
	14	280	42	840
V$_{OD}$ differential peak-to-peak typical	15	300	43	860
	16	320	44	880
	17	340	45	900
	18	360	46	920
	19	380	47	940
	20	400	48	960
	21	420	49	980
	22	440	50	1000
	23	460	51	1020
	24	480	52	1040

[58] Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.
[59] Only valid for data rates ≤ 5 Gbps.

Symbol	Description	Min	Max	Unit
T_h	SPI MISO hold time	1	—	ns
$T_{dutycycle}$	SPI_CLK duty cycle	45	55	%
$T_{dssfrst}$	Output delay SPI_SS valid before first clock edge	8	—	ns
T_{dsslst}	Output delay SPI_SS valid after last clock edge	8	—	ns
T_{dio}	Master-out slave-in (MOSI) output delay	−1	1	ns

[86] This value is based on `rx_sample_dly` = 1 and `spi_m_clk` = 120 MHz. `spi_m_clk` is the internal clock that is used by SPI Master to derive it's `SCLK_OUT`. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

Figure 1-16: I²C Timing Diagram

NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the c4 output of the main HPS PLL and timing registers provided in the NAND controller.

Symbol	Description	Min	Max	Unit
T_{wp} [89]	Write enable pulse width	10	—	ns
T_{wh} [89]	Write enable hold time	7	—	ns
T_{rp} [89]	Read enable pulse width	10	—	ns
T_{reh} [89]	Read enable hold time	7	—	ns
T_{clesu} [89]	Command latch enable to write enable setup time	10	—	ns
T_{cleh} [89]	Command latch enable to write enable hold time	5	—	ns
T_{cesu} [89]	Chip enable to write enable setup time	15	—	ns
T_{ceh} [89]	Chip enable to write enable hold time	5	—	ns
T_{alesu} [89]	Address latch enable to write enable setup time	10	—	ns
T_{aleh} [89]	Address latch enable to write enable hold time	5	—	ns
T_{dsu} [89]	Data to write enable setup time	10	—	ns

[89] Timing of the NAND interface is controlled through the NAND configuration registers.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CK}[105]	nCONFIG high to first rising edge on DCLK	1506	—	μs
t_{ST2CK}[105]	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode[106]	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times$ CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information

PS Configuration Timing
Provides the PS configuration timing waveform.

---

[105] If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.
[106] The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

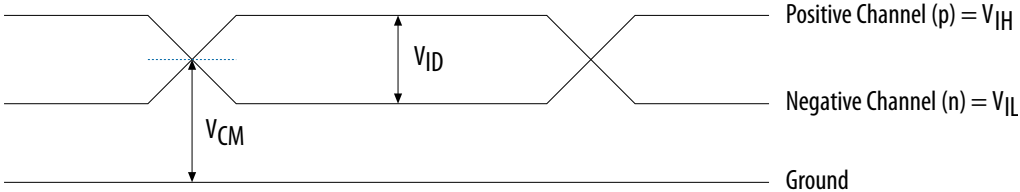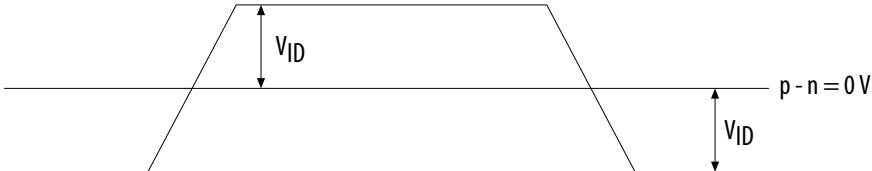## Minimum Configuration Time Estimation

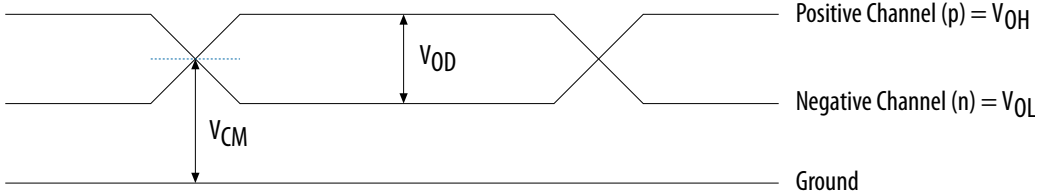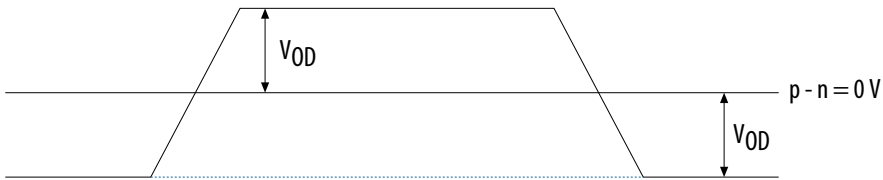**Table 1-73: Minimum Configuration Time Estimation for Arria V Devices**

The estimated values are based on the configuration `.rbf` sizes in Uncompressed .rbf Sizes for Arria V Devices table.
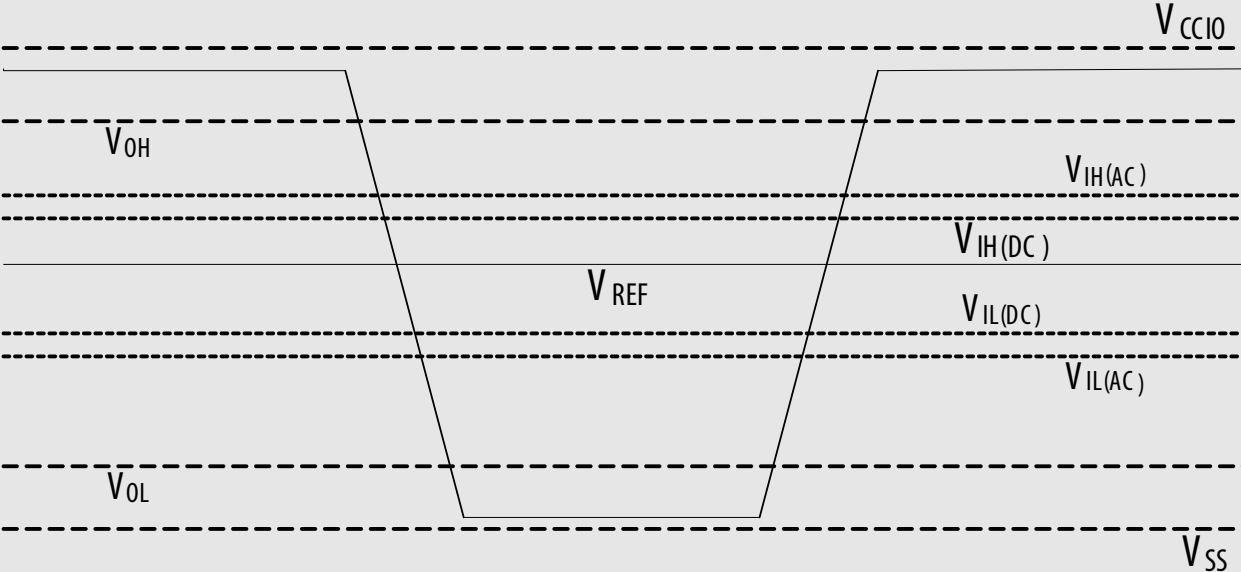
Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Glossary

Table 1-78: Glossary

Term	Definition
Differential I/O standards	Receiver Input Waveforms

Term	Definition
	Transmitter Output Waveforms **Single-Ended Waveform** Positive Channel (p) = V_{OH} V_{OD} Negative Channel (n) = V_{OL} V_{CM} Ground **Differential Waveform** V_{OD} p − n = 0 V V_{OD}
f_{HSCLK}	Left/right PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} =1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ =1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).

Term	Definition
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.
	The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.
	Single-Ended Voltage Referenced I/O Standard
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Date	Version	Changes
July 2014	3.8	• Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Updated V_{CC_HPS} specification in Table 5. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 39. • Updated T_d and T_h specifications in Table 45. • Added T_h specification in Table 47 and Figure 13. • Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 58. • Added DCLK device initialization clock source specification in Table 60. • Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature. • Removed $f_{MAX\_RU\_CLK}$ specification in Table 63.
February 2014	3.7	• Updated $V_{CCRSTCLK\_HPS}$ maximum specification in Table 1. • Added $V_{CC\_AUX\_SHARED}$ specification in Table 1.
December 2013	3.6	• Added "HPS PLL Specifications". • Added Table 24, Table 39, and Table 40. • Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. • Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. • Removed table: GPIO Pulse Width for Arria V Devices.

Symbol	Description	Minimum	Maximum	Unit
V_I	DC input voltage	−0.5	3.8	V
T_J	Operating junction temperature	−55	125	°C
T_{STG}	Storage temperature (No bias)	−65	150	°C
I_{OUT}	DC output current per pin	−25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	−0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	−0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	−0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	−0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	−0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	−0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	−0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	−0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	−0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	−0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	−0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

Symbol	Description	Condition (V)	Overshoot Duration as % @ $T_J = 100°C$	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Recommended Operating Conditions

Table 2-5: Recommended Operating Conditions for Arria V GZ Devices

Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum[114]	Typical	Maximum [114]	Unit
V_{CC}	Core voltage and periphery circuitry power supply [115]	—	0.82	0.85	0.88	V

[114] The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

[115] The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB [122]	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: • Data rate > 10.3 Gbps. • DFE is used.	1.05	3.0	1.5	V
If ANY of the following conditions are true [123] : • ATX PLL is used. • Data rate > 6.5Gbps. • DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	1.0			
If ALL of the following conditions are true: • ATX PLL is not used. • Data rate ≤ 6.5Gbps. • DFE, AEQ, and EyeQ are not used.	0.85	2.5		

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

---

[122] If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

[123] Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	−0.3	V_{REF} − 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} − 0.25	V_{REF} + 0.25	0.28	V_{CCIO} − 0.28	13.4	−13.4
SSTL-15 Class I	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	−8
SSTL-15 Class II	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	−16
SSTL-135 Class I, II	—	V_{REF} − 0.09	V_{REF} + 0.09	—	V_{REF} − 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} − 0.85	V_{REF} + 0.85	—	V_{REF} − 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.2	V_{REF} + 0.2	0.4	V_{CCIO} − 0.4	8	−8
HSTL-18 Class II	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.2	V_{REF} + 0.2	0.4	V_{CCIO} − 0.4	16	−16
HSTL-15 Class I	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.2	V_{REF} + 0.2	0.4	V_{CCIO} − 0.4	8	−8
HSTL-15 Class II	—	V_{REF} − 0.1	V_{REF} + 0.1	—	V_{REF} − 0.2	V_{REF} + 0.2	0.4	V_{CCIO} − 0.4	16	−16
HSTL-12 Class I	−0.15	V_{REF} − 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} − 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	−8
HSTL-12 Class II	−0.15	V_{REF} − 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} − 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	−16
HSUL-12	—	V_{REF} − 0.13	V_{REF} + 0.13	—	V_{REF} − 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—

Symbol	Parameter	Min	Typ	Max	Unit
t_{OUTPJ_IO}, [173], [175]	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{FOUTPJ_IO} [173], [175], [176]	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} [173], [175]	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{FOUTCCJ\_IO}$ [173], [175], [176]	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$ [173], [177]	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLS ($f_{OUT} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

[175] The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

[176] This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

[177] The cascaded PLL specification is only applicable with the following condition:
    a. Upstream PLL: 0.59Mhz $\leq$ Upstream PLL BW < 1 MHz
    b. Downstream PLL: Downstream PLL BW > 2 MHz

Symbol	Parameter	Min	Typ	Max	Unit
k_{VALUE}	Numerator of Fraction	128	8388608	2147483648	—
f_{RES}	Resolution of VCO frequency (f_{INPFD} = 100 MHz)	390625	5.96	0.023	Hz

Related Information

- **Duty Cycle Distortion (DCD) Specifications** on page 2-56
- **DLL Range Specifications** on page 2-53

DSP Block Specifications

Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices

Mode	Performance			Unit
	C3, I3L	C4	I4	
Modes using One DSP Block				
Three 9 × 9	480	420		MHz
One 18 × 18	480	420	400	MHz
Two partial 18 × 18 (or 16 × 16)	480	420	400	MHz
One 27 × 27	400	350		MHz
One 36 × 18	400	350		MHz
One sum of two 18 × 18 (One sum of two 16 × 16)	400	350		MHz
One sum of square	400	350		MHz
One 18 × 18 plus 36 (a × b) + c	400	350		MHz
Modes using Two DSP Blocks				
Three 18 × 18	400	350		MHz
One sum of four 18 × 18	380	300		MHz

Symbol	Conditions	C3, I3L			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 [182], [183]	[184]	—	1250	[184]	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA [185], [186], [187], [188]	[184]	—	1600	[184]	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	[184]	—	[189]	[184]	—	[189]	Mbps
	SERDES factor J = 1, uses SDR Register	[184]	—	[189]	[184]	—	[189]	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) [190]	SERDES factor J = 4 to 10 [191]	[184]	—	840	[184]	—	840	Mbps

[182] If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

[183] The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

[184] The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

[185] Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

[186] Requires package skew compensation with PCB trace length.

[187] Do not mix single-ended I/O buffer within LVDS I/O bank.

[188] Chip-to-chip communication only with a maximum load of 5 pF.

[189] The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
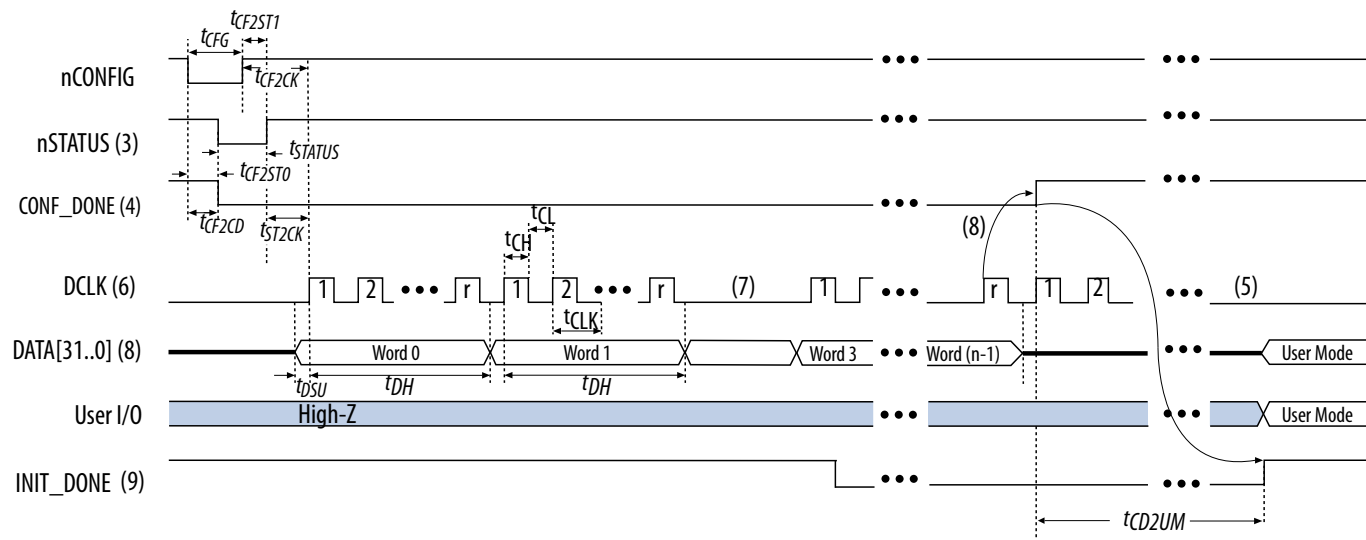
[190] You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

[191] When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.

Notes:
1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	μs
t_{STATUS}	nSTATUS low pulse width	268	1,506 [210]	μs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 [211]	μs
t_{CF2CK} [212]	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t_{ST2CK} [212]	nSTATUS high to first rising edge of DCLK	2	—	μs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	$N-1/f_{DCLK}$ [213]	—	s
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency (FPP ×8/×16)	—	125	MHz
	DCLK frequency (FPP ×32)	—	100	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode [214]	175	437	μs

[210] You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

[211] You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

[212] If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

[213] N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

[214] The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

Term	Definition
V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V_{SWING}	Differential input voltage
V_X	Input differential cross point voltage
V_{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	• Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table. • Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table. • Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. • Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. • Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.