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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba7d4f31i5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1-4 Recommended Operating Conditions

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
		3.8	100	%
		3.85	68	%
		3.9	45	%
		3.95	28	%
		4	15	%
		4.05	13	%
		4.1	11	%
		4.15	9	%
Vi (AC)	AC input voltage	4.2	8	%
		4.25	7	%
		4.3	5.4	%
		4.35	3.2	%
		4.4	1.9	%
		4.45	1.1	%
		4.5	0.6	%
		4.55	0.4	%
		4.6	0.2	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.



I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Тур	Max	Unit
II	Input pin	$V_{I} = 0 V$ to $V_{CCIOMAX}$	-30	—	30	μΑ
I _{OZ}	Tri-stated I/O pin	$V_{O} = 0 V$ to $V_{CCIOMAX}$	-30		30	μΑ

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

				V _{CCIO} (V)				o (V)							
Parameter	Symbol	Condition	1.	.2	1	.5	1	.8	2	.5	3.	.0	3	.3	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	_	12		30	_	50		70		70		μΑ
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	-8	_	-12		-30	_	-50		-70	_	-70		μΑ
Bus-hold, low, overdrive current	I _{ODL}	$\begin{array}{c} 0 \ \mathrm{V} < \mathrm{V_{IN}} \\ < \mathrm{V_{CCIO}} \end{array}$		125	_	175	_	200		300		500	_	500	μΑ
Bus-hold, high, overdrive current	I _{ODH}	0 V <v<sub>IN <v<sub>CCIO</v<sub></v<sub>	_	-125	_	-175	_	-200		-300	_	-500	_	-500	μΑ

Arria V GX, GT, SX, and ST Device Datasheet

Altera Corporation



I/O Standard		$V_{CCIO}(V)$)		V _{ID} (mV) ⁽¹⁶⁾			$V_{ICM(DC)}(V)$		١	V _{OD} (V) ⁽¹⁷	7)	١	V _{OCM} (V) ⁽	17)(18)								
	Min	Тур	Мах	Min	Condition	Max	Min	Condition	Max	Min	Тур	Max	Min	Тур	Max								
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.						receiver, and ecifications																
2.5 V	2 375	2.5	2 625	100	V _{CM} =		0.05	D _{MAX} ≤ 1.25 Gbps	1.80	0.247		0.6	1 125	1 25	1 375								
LVDS ⁽¹⁹⁾	2.375	2.5	2.023	100 1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	1.25 V	_	1.05	D _{MAX} > 1.25 Gbps	1.55	0.247		0.0	1.125	1.25	1.375
RSDS (HIO) ⁽²⁰⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	_	0.25		1.45	0.1	0.2	0.6	0.5	1.2	1.4								
Mini-LVDS (HIO) ⁽²¹⁾	2.375	2.5	2.625	200		600	0.300	_	1.425	0.25	_	0.6	1	1.2	1.4								
	300					D _{MAX} ≤ 700 Mbps	$X \leq 1.80$ [bps																
				1.00	D _{MAX} > 700 Mbps	1.60																	

- Transceiver Specifications for Arria V GX and SX Devices on page 1-23 Provides the specifications for transmitter, receiver, and reference clock I/O pin.
- $^{(16)}$ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.
- ⁽¹⁷⁾ $R_{\rm L}$ range: $90 \le R_{\rm L} \le 110 \ \Omega$.
- ⁽¹⁸⁾ This applies to default pre-emphasis setting only.
- ⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.
- ⁽²⁰⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.
- ⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.
- ⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.



Symbol/Description	Condition	Tran	sceiver Speed Gra	de 3	Unit
Symbol/Description	Condition	Min	Тур	Max	Ont
	85- Ω setting	—	85	—	Ω
Differential on-chip termination	100- Ω setting	—	100	—	Ω
resistors	120-Ω setting	—	120	—	Ω
	150-Ω setting		150	_	Ω
Intra-differential pair skew	TX V_{CM} = 0.65 V (AC coupled) and slew rate of 15 ps			15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode			180	ps
Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾	× <i>N</i> PMA bonded mode			500	ps

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver S	peed Grade 3	Unit	
Symbol Description	Min	Max	onit	
Supported data range	0.611	10.3125	Gbps	
fPLL supported data range	611	3125	Mbps	

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.



Symbol	Parameter	Condition	Min	Тур	Мах	Unit
		-3 speed grade	5	—	800 ⁽⁶¹⁾	MHz
f	Input clock fraguency	-4 speed grade	5		800 ⁽⁶¹⁾	MHz
IIN	input clock nequency	–5 speed grade	5	_	750 ⁽⁶¹⁾	MHz
		-6 speed grade	5		625(61)	MHz
f _{INPFD}	Integer input clock frequency to the phase frequency detector (PFD)	_	5	_	325	MHz
f _{fINPFD}	Fractional input clock frequency to the PFD		50	_	160	MHz
		-3 speed grade	600	—	1600	MHz
f (62)	PLL voltage-controlled oscillator (VCO) operating range	-4 speed grade	600	_	1600	MHz
IVCO		–5 speed grade	600		1600	MHz
		-6 speed grade	600		1300	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	_	40		60	%
		-3 speed grade	_	_	500 ⁽⁶³⁾	MHz
£	Output frequency for internal global or	-4 speed grade	—	—	500 ⁽⁶³⁾	MHz
LOUT	regional clock	-5 speed grade	_	_	500 ⁽⁶³⁾	MHz
		-6 speed grade	_	_	400 ⁽⁶³⁾	MHz



⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled



Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Darallel Papid I/O	00001111	2	128	640
rataliei Kapiti 1/0	10010000	4	64	640
Miscellaneous	10101010	8	32	640
witscenaricous	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.





DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

Parameter	-I3, -C4	-I5, -C5	-C6	Unit
DLL operating frequency range	200 - 667	200 - 667	200 - 667	MHz

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DOS PSERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

Number of DQS Delay Buffer	–I3, –C4	–I5, –C5	-C6	Unit
2	40	80	80	ps



Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard. The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma. Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

Parameter C	Clock Notwork	Symbol	-I3, -C4		–I5, –C5		-C6		Unit
	CIOCK NELWOIK	Symbol	Min	Max	Min	Max	Min	Max	
Clock period jitter	PHYCLK	t _{JIT(per)}	-41	41	-50	50	-55	55	ps
Cycle-to-cycle period jitter	PHYCLK	t _{JIT(cc)}	6	3	9	0	9	94	ps

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	_		20	MHz
T _{OCTCAL}	Number of octus RCLK clock cycles required for $R_{\rm S}$ OCT/R_T OCT calibration		1000		Cycles
T _{OCTSHIFT}	Number of OCTUSRCLK clock cycles required for OCT code to shift out		32	_	Cycles
T _{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	_	2.5		ns



1-82 PS Configuration Timing

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CK}^{(105)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
t _{ST2CK} ⁽¹⁰⁵⁾	nSTATUS high to first rising edge of DCLK	2		μs
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA[] hold time after rising edge on DCLK	0	_	ns
t _{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f_{MAX}	DCLK frequency	_	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽¹⁰⁶⁾	175	437	μs
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} × CLKUSR period)	_	_
T _{init}	Number of clock cycles required for device initialization	8,576		Cycles

Related Information

PS Configuration Timing

Provides the PS configuration timing waveform.



 $^{^{(105)}}$ If <code>nstatus</code> is monitored, follow the t_{ST2CK} specification. If <code>nstatus</code> is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰⁶⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

Conditions	VCCR_GXB and VCCT_GXB ⁽¹²²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	1.05			
• Data rate > 10.3 Gbps.				
• DFE is used.				
If ANY of the following conditions are true ⁽¹²³⁾ :	1.0	3.0		
 ATX PLL is used. Data rate > 6.5Gbps. DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. 			1.5	V
If ALL of the following conditions are true:	0.85	2.5		
 ATX PLL is not used. Data rate ≤ 6.5Gbps. DFE, AEQ, and EyeQ are not used. 				

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



⁽¹²²⁾ If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

⁽¹²³⁾ Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

I/O Standard		V _{CCIO} (V)		V _{REF} (V)			V _{TT} (V)		
	Min	Тур	Max	Min	Тур	Max	Min	Тур	Мах
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 imes V_{ m CCIO}$	0.49 × V _{CCIO}	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	$0.49 \times V_{ m CCIO}$	0.5 × VCCIO	$0.51 \times V_{CCIO}$
SSTL-12 Class I, II	1.14	1.20	1.26	$0.49 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$	0.49 × V _{CCIO}	0.5 × VCCIO	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCIO} /2	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCIO} /2	_
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 imes V_{ m CCIO}$	$0.53 \times V_{ m CCIO}$	_	V _{CCIO} /2	_
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{ m CCIO}$	$0.51 \times V_{ m CCIO}$			_

Table 2-18: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices

I/O Standard	V _{IL(D}	$V_{IL(DC)}(V) \qquad V_{IH(DC)}(V) \qquad V_{IL(AC)}(V) \qquad V_{IH(AC)}(V)$		V _{IH(AC)} (V)	V _{OL} (V)	V _{OH} (V)	L.(mA)	I. (mA)		
	Min	Max	Min	Max	Мах	Min	Max	Min	י _{סן} (וויא)	
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCIO} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCIO} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7



Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transo	Unit		
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max	
fixedclk clock frequency	PCIe Receiver Detect	_	100 or 125	_	_	100 or 125	_	MHz
Reconfiguration clock (mgmt_clk_ clk) frequency	—	100		125	100	_	125	MHz

Arria V Device Overview

For more information about device ordering codes.

Receiver

Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Trans	Transceiver Speed Grade 2			Transceiver Speed Grade 3		
	Conditions	Min	Тур	Max	Min	Тур	Max	Onic
Supported I/O Standards	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS							
Data rate (Standard PCS) (143), (144)	—	600		9900	600	_	8800	Mbps
Data rate (10G PCS) (143), (144)	_	600		12500	600	_	10312.5	Mbps
Absolute $\mathrm{V}_{\mathrm{MAX}}$ for a receiver pin $^{(145)}$	—			1.2			1.2	V
Absolute V_{MIN} for a receiver pin	_	-0.4	_		-0.4	_	_	V

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

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Symbol/Description	Conditions	Trans	ceiver Spee	d Grade 2	Transceiver Speed Grade 3			Unit	
Symbol/Description	Conditions	Min	Тур	Max	Min	Тур	Max		
Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration	—			1.6	—	_	1.6	V	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration ⁽¹⁴⁶⁾	$V_{CCR_GXB} = 1.0 V$ $(V_{ICM} = 0.75 V)$			1.8	—		1.8	V	
	$V_{CCR_GXB} = 0.85 V$ $(V_{ICM} = 0.6 V)$			2.4	—		2.4	V	
Minimum differential eye opening at receiver serial input pins ⁽¹⁴⁷⁾⁽¹⁴⁸⁾	_	85		_	85	_	—	mV	
	85– Ω setting		85 ± 30%	—	—	85 ± 30%	_	Ω	
Differential on-chip termination	100– Ω setting		100 ± 30%	—	—	100 ± 30%	_	Ω	
resistors	120– Ω setting		120 ± 30%	—	_	120 ± 30%	—	Ω	
	150– Ω setting		150 ± 30%	_	_	150 ± 30%	_	Ω	



⁽¹⁴⁶⁾ The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

⁽¹⁴⁷⁾ The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽¹⁴⁸⁾ Minimum eye opening of 85 mV is only for the unstressed input eye condition.

2-44 Periphery Performance

Description	Min	Тур	Мах	Unit
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps



FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1,

t_{CF2ST1} tcfg ;↔ nCONFIG ŤĊF2CK nSTATUS (3) 🕳 tstatus tCF2ST0 CONF_DONE (4) TCL tCH tsT2CK ŤĊF2CD (8) DCLK (6) (7) 1 2 ••• r 2 ••• r 1 \mathbf{D} (5) tCLK DATA[31..0] (8) Word 0 Word User Mode Word 3 • • • Word (n-1) tDH tDH tpsy High-Z User I/O User Mode INIT DONE (9) tCD2UM

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.

Notes:

- 1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- 3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
- 4. After power-up, before and during configuration, CONF_DONE is low.
- 5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- 6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
- 7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31.0] pins prior to sending the first DCLK rising edge.
- 8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- 9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.





Configuration, Design Security, and Remote System Upgrades in Arria V Devices

Initialization

Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices

Initialization Clock Source	Configuration Schemes Maximum Frequency (MHz)		Minimum Number of Clock Cycles
Internal Oscillator	nternal Oscillator AS, PS, FPP 12.5		
CLKUSR ⁽²²²⁾	PS, FPP	125	9576
	AS	100	8576
DCLK	PS, FPP	125	

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (.hex) or tabular text file (.ttf) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

Arria V GZ Device Datasheet

Altera Corporation



⁽²²¹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section of the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²²⁾ To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the "User Watchdog Timer" section.
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices For more information about the reset_timer input for the ALTREMOTE_UPDATE IP core, refer to the "Remote System Upgrade State Machine" section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete placeand-route.

Related Information

Arria V Devices Documentation page

For the Excel-based I/O Timing spreadsheet

Arria V GZ Device Datasheet

Altera Corporation



⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.

⁽²²⁷⁾ This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.





Term	Definition
V _{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
V _{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
V _{SWING}	Differential input voltage
V _X	Input differential cross point voltage
V _{OX}	Output differential cross point voltage
W	High-speed I/O block—clock boost factor

Document Revision History

Date	Version	Changes
February 2017	2017.02.10	 Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table. Changed the minimum value for t_{CD2UMC} in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK to DATA[] Ratio is 1" table.
		 Changed the minimum value for t_{CD2UMC} in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table. Changed the minimum value for t_{CD2UMC} in the "PS Timing Parameters for Arria V GZ Devices" table. Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table.



Date	Version	Changes
July 2014	3.8	 Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	 Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications".
August 2013	3.5	Updated Table 28.
August 2013	3.4	 Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	 Added Table 23. Updated Table 5, Table 22, Table 26, and Table 57. Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	 Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. Updated "Maximum Allowed Overshoot and Undershoot Voltage".
December 2012	3.0	Initial release.

