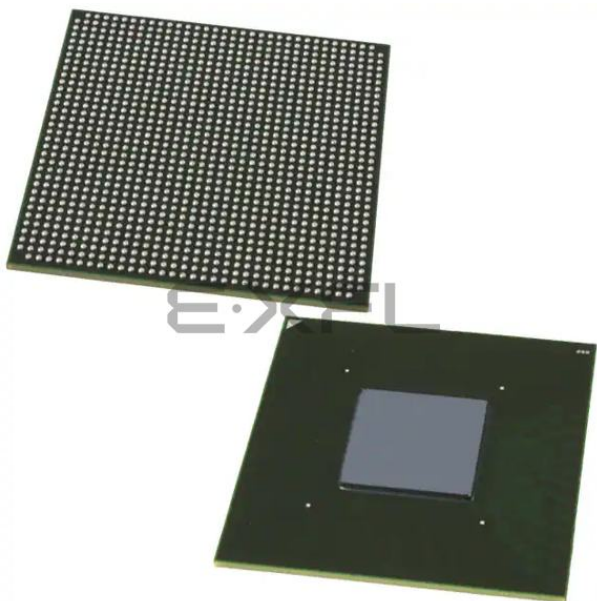




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxba7d4f35c5n

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V_{CC}	Core voltage power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCP}	Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply	–C4, –I5, –C5, –C6	1.07	1.1	1.13	V
		–I3	1.12	1.15	1.18	V
V_{CCPGM}	Configuration pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
V_{CC_AUX}	Auxiliary supply	—	2.375	2.5	2.625	V
$V_{CCBAT}^{(2)}$	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
$V_{CCPD}^{(3)}$	I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽²⁾ If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT} . Arria V devices do not exit POR if V_{CCBAT} is not powered up.

⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CCIO}	I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	1.283	1.35	1.418	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	1.14	1.2	1.26	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C
t _{RAMP} ⁽⁴⁾	Power supply ramp time	Standard POR	200 μs	—	100 ms	—
		Fast POR	200 μs	—	4 ms	—

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

Symbol	Description	Condition	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIOMAX}$	-30	—	30	μA

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Parameter	Symbol	Condition	V _{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I _{SUSL}	V _{IN} > V _{IL} (max)	8	—	12	—	30	—	50	—	70	—	70	—	μA
Bus-hold, high, sustaining current	I _{SUSH}	V _{IN} < V _{IH} (min)	−8	—	−12	—	−30	—	−50	—	−70	—	−70	—	μA
Bus-hold, low, overdrive current	I _{ODL}	0 V < V _{IN} < V _{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	μA
Bus-hold, high, overdrive current	I _{ODH}	0 V < V _{IN} < V _{CCIO}	—	−125	—	−175	—	−200	—	−300	—	−500	—	−500	μA

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTD_manual}^{(51)}$	—	4	—	—	μs
$t_{LTR_LTD_manual}^{(52)}$	—	15	—	—	μs
Programmable ppm detector ⁽⁵³⁾	—	$\pm 62.5, 100, 125, 200, 250, 300, 500, \text{ and } 1000$			ppm
Run length	—	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 ⁽⁵⁴⁾ DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams.			

Table 1-29: Transmitter Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.5 V PCML				
Data rate (6-Gbps transceiver)	—	611	—	6553.6	Mbps
Data rate (10-Gbps transceiver)	—	0.611	—	10.3125	Gbps
V _{OCM} (AC coupled)	—	—	650	—	mV
V _{OCM} (DC coupled)	≤ 3.2 Gbps ⁽⁴⁸⁾	670	700	730	mV

⁽⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedto data signal goes high when the CDR is functioning in the manual mode.

⁽⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedto ref signal goes high when the CDR is functioning in the manual mode.

⁽⁵³⁾ The rate match FIFO supports only up to ± 300 ppm.

⁽⁵⁴⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

Table 1-38: Memory Block Performance Specifications for Arria V Devices

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	–I3, –C4	–I5, –C5	–C6	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 100°C	±8°C	No	1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When $J = 3$ to 10, use the serializer/deserializer (SERDES) block. When $J = 1$ or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	800	5	—	750	5	—	625	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷³⁾		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	625	5	—	625	5	—	500	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷⁴⁾		Clock boost factor $W = 1$ to $40^{(72)}$	5	—	420	5	—	420	5	—	420	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)		—	5	—	$625^{(75)}$	5	—	$625^{(75)}$	5	—	$500^{(75)}$	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor $J = 3$ to $10^{(76)}$	⁽⁷⁷⁾	—	1250	⁽⁷⁷⁾	—	1250	⁽⁷⁷⁾	—	1050	Mbps

⁽⁷²⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁷³⁾ This applies to DPA and soft-CDR modes only.

⁽⁷⁴⁾ This applies to non-DPA mode only.

⁽⁷⁵⁾ This is achieved by using the LVDS clock network.

⁽⁷⁶⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁷⁷⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

Symbol		Condition	-I3, -C4			-I5, -C5			-C6			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
		Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver	True Differential I/O Standards - f_{HSDRDPA} (data rate)	SERDES factor J = 3 to 10 ⁽⁷⁶⁾	150	—	1250	150	—	1250	150	—	1050	Mbps
		SERDES factor J ≥ 8 with DPA ⁽⁷⁶⁾⁽⁷⁸⁾	150	—	1600	150	—	1500	150	—	1250	Mbps
	f_{HSDR} (data rate)	SERDES factor J = 3 to 10	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	⁽⁷⁷⁾	—	⁽⁸³⁾	Mbps
		SERDES factor J = 1 to 2, uses DDR registers	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	⁽⁷⁷⁾	—	⁽⁷⁹⁾	Mbps
DPA Mode	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft-CDR Mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	±ppm
Non-DPA Mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

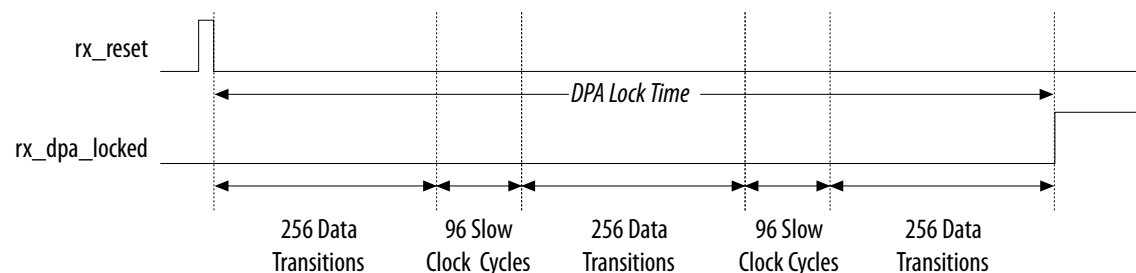


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

POR Delay	Minimum	Maximum	Unit
Standard	100	300	ms

Related Information**MSEL Pin Settings**

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing

Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 ⁽⁹²⁾	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	2	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	12 ⁽⁹³⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽⁹³⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽⁹³⁾	ns

⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

Variant	Member Code	Active Serial ⁽¹⁰⁸⁾			Fast Passive Parallel ⁽¹⁰⁹⁾		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Arria V GX	A1	4	100	178	16	125	36
	A3	4	100	178	16	125	36
	A5	4	100	255	16	125	51
	A7	4	100	255	16	125	51
	B1	4	100	344	16	125	69
	B3	4	100	344	16	125	69
	B5	4	100	465	16	125	93
	B7	4	100	465	16	125	93
Arria V GT	C3	4	100	178	16	125	36
	C7	4	100	255	16	125	51
	D3	4	100	344	16	125	69
	D7	4	100	465	16	125	93
Arria V SX	B3	4	100	465	16	125	93
	B5	4	100	465	16	125	93
Arria V ST	D3	4	100	465	16	125	93
	D5	4	100	465	16	125	93

Related Information**Configuration Files** on page 1-83⁽¹⁰⁸⁾ DCLK frequency of 100 MHz using external CLKUSR.⁽¹⁰⁹⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Date	Version	Changes
November 2012	3.0	- Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. - Removed table: Transceiver Block Jitter Specifications for Arria V Devices. - Added HPS information: - Added “HPS Specifications” section. - Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. - Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. - Updated Table 3 and Table 5.
October 2012	2.4	- Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. - Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21.
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	- Updated the maximum voltage for V_I (DC input voltage) in Table 1. - Updated Table 20 to include the Arria V GX -I3 speed grade. - Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. - Updated the SERDES factor condition in Table 30. - Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.
June 2012	2.1	Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4.

Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade			
	C3	C4	I3L	I4
2	Yes	—	Yes	—
3	—	Yes	—	Yes

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	−0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	−0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	−0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	−0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	−0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	−0.5	3.9	V
V _{CCIO}	I/O power supply	−0.5	3.9	V
V _{CCD_FPLL}	PLL digital power supply	−0.5	1.8	V
V _{CCA_FPLL}	PLL analog power supply	−0.5	3.4	V

Symbol	Description	Minimum ⁽¹¹⁸⁾	Typical	Maximum ⁽¹¹⁸⁾	Unit
$V_{CCR_GXBL}^{(121)}$	Receiver analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCR_GXBR}^{(121)}$	Receiver analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBL}^{(121)}$	Transmitter analog power supply (left side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
$V_{CCT_GXBR}^{(121)}$	Transmitter analog power supply (right side)	0.82	0.85	0.88	V
		0.97	1.0	1.03	
		1.03	1.05	1.07	
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	1.425	1.5	1.575	V

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.4	2.4	2	-2
LVC MOS	2.85	3	3.15	-0.3	0.8	1.7	3.6	0.2	$V_{CCIO} - 0.2$	0.1	-0.1
2.5 V	2.375	2.5	2.625	-0.3	0.7	1.7	3.6	0.4	2	1	-1
1.8 V	1.71	1.8	1.89	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	0.45	$V_{CCIO} - 0.45$	2	-2
1.5 V	1.425	1.5	1.575	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2
1.2 V	1.14	1.2	1.26	-0.3	$0.35 \times V_{CCIO}$	$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	2	-2

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$

I/O Standard	$V_{IL(DC)} (V)$		$V_{IH(DC)} (V)$		$V_{IL(AC)} (V)$	$V_{IH(AC)} (V)$	$V_{OL} (V)$	$V_{OH} (V)$	$I_{ol} (mA)$	$I_{oh} (mA)$
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class II	-0.3	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCIO} + 0.3$	$V_{REF} - 0.25$	$V_{REF} + 0.25$	0.28	$V_{CCIO} - 0.28$	13.4	-13.4
SSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	8	-8
SSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.175$	$V_{REF} + 0.175$	$0.2 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	16	-16
SSTL-135 Class I, II	—	$V_{REF} - 0.09$	$V_{REF} + 0.09$	—	$V_{REF} - 0.16$	$V_{REF} + 0.16$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-125 Class I, II	—	$V_{REF} - 0.85$	$V_{REF} + 0.85$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
SSTL-12 Class I, II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.2 * V_{CCIO}$	$0.8 * V_{CCIO}$	—	—
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	⁽¹²⁷⁾	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

⁽¹²⁷⁾ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾	—	100	—	710	100	—	710	MHz

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
R _{REF}	—	—	1800 ±1%	—	—	1800 ±1%	—	Ω

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Transceiver Clocks**Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁴¹⁾ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵³⁾	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁵⁴⁾	—		—	10	—	—	10	μs

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁵³⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁴⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Date	Version	Changes
July 2014	3.8	- Updated Table 21. - Updated Table 22 V_{OCM} (DC Coupled) condition. - Updated the DCLK note to Figure 6, Figure 7, and Figure 9. - Added note to Table 5 and Table 6. - Added the DCLK specification to Table 50. - Added note to Table 51. - Updated the list of parameters in Table 53.
February 2014	3.7	Updated Table 28.
December 2013	3.6	- Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. - Updated “PLL Specifications”.
August 2013	3.5	Updated Table 28.
August 2013	3.4	- Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. - Updated Table 2 and Table 28.
June 2013	3.3	Updated Table 23, Table 28, Table 51, and Table 55.
May 2013	3.2	- Added Table 23. - Updated Table 5, Table 22, Table 26, and Table 57. - Updated Figure 6, Figure 7, Figure 8, and Figure 9.
March 2013	3.1	- Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52. - Updated “Maximum Allowed Overshoot and Undershoot Voltage”.
December 2012	3.0	Initial release.