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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	336
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	672-BBGA, FCBGA
Supplier Device Package	672-FBGA (27x27)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxba7d6f27c6n">https://www.e-xfl.com/product-detail/intel/5agxba7d6f27c6n</a>

## Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

I/O Standard	$V_{CCIO}$ (V)			$V_{REF}$ (V)			$V_{TT}$ (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	$V_{REF} - 0.04$	$V_{REF}$	$V_{REF} + 0.04$
SSTL-15 Class I, II	1.425	1.5	1.575	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-135 Class I, II	1.283	1.35	1.418	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
SSTL-125 Class I, II	1.19	1.25	1.26	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	$0.47 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.53 \times V_{CCIO}$	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	$0.49 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.51 \times V_{CCIO}$	—	—	—

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{OL}^{(14)}$ (mA)	$I_{OH}^{(14)}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25 \times V_{CCIO}$	$0.75 \times V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1 \times V_{CCIO}$	$0.9 \times V_{CCIO}$	—	—

### Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

I/O Standard	$V_{CCIO}$ (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-135	1.283	1.35	1.45	0.18	<sup>(15)</sup>	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$

<sup>(14)</sup> To meet the  $I_{OL}$  and  $I_{OH}$  specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the  $I_{OL}$  and  $I_{OH}$  specifications in the datasheet.

<sup>(15)</sup> The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter $\text{REFCLK}$ phase noise <sup>(43)</sup>	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	$\geq 1$ MHz	—	—	–130	dBc/Hz
$R_{\text{REF}}$	—	—	$2000 \pm 1\%$	—	$\Omega$

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$\text{fixedclk}$ clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP ( $\text{mgmt\_clk\_clk}$ ) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver) <sup>(44)</sup>	—	611	—	6553.6	Mbps

<sup>(43)</sup> The transmitter  $\text{REFCLK}$  phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.<sup>(44)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Symbol	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)	V <sub>OD</sub> Setting <sup>(58)</sup>	V <sub>OD</sub> Value (mV)
	25	500	53	1060
	26	520	54	1080
	27	540	55	1100
	28	560	56	1120
	29	580	57	1140
	30	600	58	1160
	31	620	59	1180
	32	640	60	1200
	33	660		

## Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy  $|B| + |C| \leq 60$  where  $|B| = V_{OD}$  setting with termination value,  $R_{TERM} = 100 \Omega$  and  $|C| = 1st$  post tap pre-emphasis setting.
- $|B| - |C| > 5$  for data rates  $< 5$  Gbps and  $|B| - |C| > 8.25$  for data rates  $> 5$  Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$ , where  $V_{MAX} = |B| + |C|$  and  $V_{MIN} = |B| - |C|$ .

Exception for PCIe Gen2 design: V<sub>OD</sub> setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis – 6dB setting (pipe\_txdeemp = 1'b0) using Altera PCIe Hard IP and PIPE IP cores.

<sup>(58)</sup> Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

For example, when  $V_{OD} = 800$  mV, the corresponding  $V_{OD}$  value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices**

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime $V_{OD}$ Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
0	0	0	0	0	0	0	0	dB
1	1.97	0.88	0.43	0.32	0.24	0.19	0.13	dB
2	3.58	1.67	0.95	0.76	0.61	0.5	0.41	dB
3	5.35	2.48	1.49	1.2	1	0.83	0.69	dB
4	7.27	3.31	2	1.63	1.36	1.14	0.96	dB
5	—	4.19	2.55	2.1	1.76	1.49	1.26	dB
6	—	5.08	3.11	2.56	2.17	1.83	1.56	dB
7	—	5.99	3.71	3.06	2.58	2.18	1.87	dB
8	—	6.92	4.22	3.47	2.93	2.48	2.11	dB
9	—	7.92	4.86	4	3.38	2.87	2.46	dB
10	—	9.04	5.46	4.51	3.79	3.23	2.77	dB
11	—	10.2	6.09	5.01	4.23	3.61	—	dB
12	—	11.56	6.74	5.51	4.68	3.97	—	dB
13	—	12.9	7.44	6.1	5.12	4.36	—	dB
14	—	14.44	8.12	6.64	5.57	4.76	—	dB
15	—	—	8.87	7.21	6.06	5.14	—	dB

Quartus Prime 1st Post Tap Pre-Emphasis Setting	Quartus Prime V <sub>OD</sub> Setting							Unit
	10 (200 mV)	20 (400 mV)	30 (600 mV)	35 (700 mV)	40 (800 mV)	45 (900 mV)	50 (1000 mV)	
16	—	—	9.56	7.73	6.49	—	—	dB
17	—	—	10.43	8.39	7.02	—	—	dB
18	—	—	11.23	9.03	7.52	—	—	dB
19	—	—	12.18	9.7	8.02	—	—	dB
20	—	—	13.17	10.34	8.59	—	—	dB
21	—	—	14.2	11.1	—	—	—	dB
22	—	—	15.38	11.87	—	—	—	dB
23	—	—	—	12.67	—	—	—	dB
24	—	—	—	13.48	—	—	—	dB
25	—	—	—	14.37	—	—	—	dB
26	—	—	—	—	—	—	—	dB
27	—	—	—	—	—	—	—	dB
28	—	—	—	—	—	—	—	dB
29	—	—	—	—	—	—	—	dB
30	—	—	—	—	—	—	—	dB
31	—	—	—	—	—	—	—	dB

**Related Information****[SPICE Models for Altera Devices](#)**

Provides the Arria V HSSI HSPICE models.

**Transceiver Compliance Specification**

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

## HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

**Table 1-50: Examples of Maximum Input Jitter**

Input Reference Clock Period	Divide Value (N)	Maximum Jitter	Unit
40 ns	1	0.8	ns
40 ns	2	1.6	ns
40 ns	4	3.2	ns

## Quad SPI Flash Timing Characteristics

**Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices**

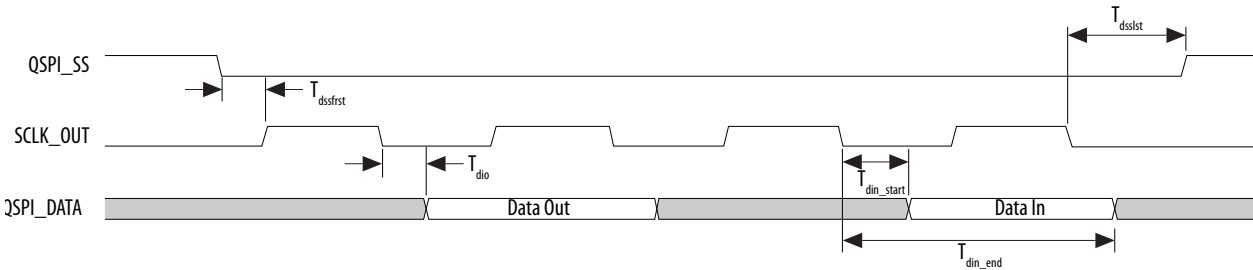
Symbol	Description	Min	Typ	Max	Unit
F <sub>clk</sub>	SCLK_OUT clock frequency (External clock)	—	—	108	MHz
T <sub>qspi_clk</sub>	QSPI_CLK clock period (Internal reference clock)	2.32	—	—	ns
T <sub>dutycycle</sub>	SCLK_OUT duty cycle	45	—	55	%
T <sub>dssfrst</sub>	Output delay QSPI_SS valid before first clock edge	—	1/2 cycle of SCLK_OUT	—	ns
T <sub>dsslst</sub>	Output delay QSPI_SS valid after last clock edge	–1	—	1	ns
T <sub>dio</sub>	I/O data output delay	–1	—	1	ns
T <sub>din_start</sub>	Input data valid start	—	—	$(2 + R_{\text{delay}}) \times T_{\text{qspi\_clk}} - 7.52^{(85)}$	ns



Symbol	Description	Min	Typ	Max	Unit
$T_{din\_end}$	Input data valid end	$(2 + R_{delay}) \times T_{qspi\_clk} - 1.21^{(85)}$	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics

Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
$T_{clk}$	CLK clock period	16.67	—	ns
$T_{su}$	SPI Master-in slave-out (MISO) setup time	8.35 <sup>(86)</sup>	—	ns

<sup>(85)</sup>  $R_{delay}$  is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about  $R_{delay}$ , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

Symbol	Description	Min	Max	Unit
$T_h$	SPI MISO hold time	1	—	ns
$T_{\text{duty cycle}}$	SPI_CLK duty cycle	45	55	%
$T_{\text{dssfrst}}$	Output delay SPI_SS valid before first clock edge	8	—	ns
$T_{\text{dsslst}}$	Output delay SPI_SS valid after last clock edge	8	—	ns
$T_{\text{dio}}$	Master-out slave-in (MOSI) output delay	–1	1	ns

<sup>(86)</sup> This value is based on  $\text{rx\_sample\_dly} = 1$  and  $\text{spi\_m\_clk} = 120$  MHz.  $\text{spi\_m\_clk}$  is the internal clock that is used by SPI Master to derive its  $\text{SCLK\_OUT}$ . These timings are based on  $\text{rx\_sample\_dly}$  of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct  $\text{rx\_sample\_dly}$  value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about  $\text{rx\_sample\_delay}$ , refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

## HPS JTAG Timing Specifications

**Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices**

Symbol	Description	Min	Max	Unit
$t_{JCP}$	TCK clock period	30	—	ns
$t_{JCH}$	TCK clock high time	14	—	ns
$t_{JCL}$	TCK clock low time	14	—	ns
$t_{JPSU}$ (TDI)	TDI JTAG port setup time	2	—	ns
$t_{JPSU}$ (TMS)	TMS JTAG port setup time	3	—	ns
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	12 <sup>(90)</sup>	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14 <sup>(90)</sup>	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14 <sup>(90)</sup>	ns

## Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

### POR Specifications

**Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices**

POR Delay	Minimum	Maximum	Unit
Fast	4	12 <sup>(91)</sup>	ms

<sup>(90)</sup> A 1-ns adder is required for each  $V_{CCIO\_HPS}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 13 ns if  $V_{CCIO\_HPS}$  of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

<sup>(91)</sup> The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
$T_{init}$	Number of clock cycles required for device initialization	8,576	—	Cycles

**Related Information****FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

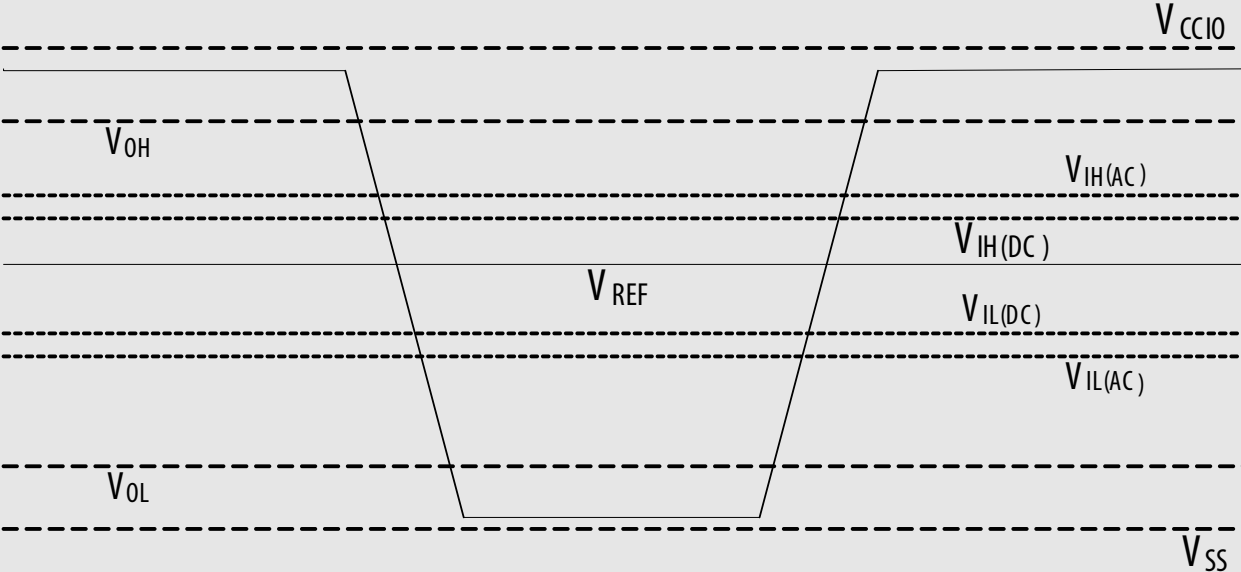
## AS Configuration Timing

**Table 1-68: AS Timing Parameters for AS  $\times 1$  and  $\times 4$  Configurations in Arria V Devices**

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The  $t_{CF2CD}$ ,  $t_{CF2ST0}$ ,  $t_{CFG}$ ,  $t_{STATUS}$ , and  $t_{CF2ST1}$  timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the  $t_{CF2ST1}$  value if you do not delay configuration by externally holding  $nSTATUS$  low.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CO}$	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
$t_{SU}$	Data setup time before the falling edge on DCLK	1.5	—	ns
$t_{DH}$	Data hold time after the falling edge on DCLK	0	—	ns
$t_{CD2UM}$	CONF_DONE high to user mode	175	437	$\mu s$
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
$T_{init}$	Number of clock cycles required for device initialization	8,576	—	Cycles

Term	Definition
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p> 
$t_C$	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
$t_{DUTY}$	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Term	Definition
$t_{\text{FALL}}$	Signal high-to-low transition time (80–20%)
$t_{\text{INCCJ}}$	Cycle-to-cycle jitter tolerance on the PLL clock input
$t_{\text{OUTPJ\_IO}}$	Period jitter on the GPIO driven by a PLL
$t_{\text{OUTPJ\_DC}}$	Period jitter on the dedicated clock output driven by a PLL
$t_{\text{RISE}}$	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1 / (\text{Receiver Input Clock Frequency Multiplication Factor}) = t_{\text{C}}/w$ )
$V_{\text{CM(DC)}}$	DC common mode input voltage.
$V_{\text{ICM}}$	Input common mode voltage—The common mode of the differential signal at the receiver.
$V_{\text{ID}}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{\text{DIF(AC)}}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{\text{DIF(DC)}}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
$V_{\text{IH}}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{\text{IH(AC)}}$	High-level AC input voltage
$V_{\text{IH(DC)}}$	High-level DC input voltage
$V_{\text{IL}}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{\text{IL(AC)}}$	Low-level AC input voltage
$V_{\text{IL(DC)}}$	Low-level DC input voltage
$V_{\text{OCM}}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
$V_{\text{OD}}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
$V_{\text{SWING}}$	Differential input voltage
$V_{\text{X}}$	Input differential cross point voltage

Date	Version	Changes
December 2015	2015.12.16	<ul style="list-style-type: none"><li>Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.<ul style="list-style-type: none"><li>Updated <math>F_{clk}</math>, <math>T_{duty\ cycle}</math>, and <math>T_{dss\ first}</math> specifications.</li><li>Added <math>T_{qspi\_clk}</math>, <math>T_{din\_start}</math>, and <math>T_{din\_end}</math> specifications.</li><li>Removed <math>T_{din\ max}</math> specifications.</li></ul></li><li>Updated the minimum specification for <math>T_{clk}</math> to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.</li><li>Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.<ul style="list-style-type: none"><li>Updated <math>T_{clk}</math> to <math>T_{sdmmc\_clk\_out}</math> symbol.</li><li>Updated <math>T_{sdmmc\_clk\_out}</math> and <math>T_d</math> specifications.</li><li>Added <math>T_{sdmmc\_clk}</math>, <math>T_{su}</math>, and <math>T_h</math> specifications.</li><li>Removed <math>T_{din\ max}</math> specifications.</li></ul></li><li>Updated the following diagrams:<ul style="list-style-type: none"><li>Quad SPI Flash Timing Diagram</li><li>SD/MMC Timing Diagram</li></ul></li><li>Updated configuration .rbf sizes for Arria V devices.</li><li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li></ul>

Date	Version	Changes
June 2015	2015.06.16	<ul style="list-style-type: none"> <li>Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table: <ul style="list-style-type: none"> <li>True RSDS output standard: data rates of up to 360 Mbps</li> <li>True mini-LVDS output standard: data rates of up to 400 Mbps</li> </ul> </li> <li>Added note in the condition for Transmitter—Emulated Differential I/O Standards <math>f_{HSDR}</math> data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.</li> <li>Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.</li> <li>Updated <math>T_h</math> location in I<sup>2</sup>C Timing Diagram.</li> <li>Updated <math>T_{wp}</math> location in NAND Address Latch Timing Diagram.</li> <li>Corrected the unit for <math>t_{DH}</math> from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is &gt;1 for Arria V Devices table.</li> <li>Updated the maximum value for <math>t_{CO}</math> from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.</li> <li>Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter. <ul style="list-style-type: none"> <li>FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1</li> <li>FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is &gt;1</li> <li>AS Configuration Timing Waveform</li> <li>PS Configuration Timing Waveform</li> </ul> </li> </ul>



Lower number refers to faster speed grade.

L = Low power devices.

Transceiver Speed Grade	Core Speed Grade			
	C3	C4	I3L	I4
2	Yes	—	Yes	—
3	—	Yes	—	Yes

## Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

**Caution:** Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices**

Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	−0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	−0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	−0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	−0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	−0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	−0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	−0.5	3.9	V
V <sub>CCD_FPLL</sub>	PLL digital power supply	−0.5	1.8	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	−0.5	3.4	V

Symbol	Description	Condition	Minimum <sup>(114)</sup>	Typical	Maximum <sup>(114)</sup>	Unit
V <sub>CCPT</sub>	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V <sub>CCPD</sub> <sup>(116)</sup>	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V <sub>CCIO</sub>	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V <sub>CCPGM</sub>	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V <sub>CCA_FPLL</sub>	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V <sub>CCD_FPLL</sub>	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V <sub>CCBAT</sub> <sup>(117)</sup>	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V

<sup>(114)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(116)</sup> V<sub>CCPD</sub> must be 2.5 V when V<sub>CCIO</sub> is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V<sub>CCPD</sub> must be 3.0 V when V<sub>CCIO</sub> is 3.0 V.

<sup>(117)</sup> If you do not use the design security feature in Arria V GZ devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Arria V GZ devices do not exit POR if V<sub>CCBAT</sub> is not powered up.

## Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

Parameter	Symbol	Conditions	V <sub>CCIO</sub>										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I <sub>SUSL</sub>	V <sub>IN</sub> > V <sub>IL</sub> (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	μA
High sustaining current	I <sub>SUSH</sub>	V <sub>IN</sub> < V <sub>IH</sub> (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	μA
Low overdrive current	I <sub>ODL</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	120	—	160	—	200	—	300	—	500	μA
High overdrive current	I <sub>ODH</sub>	0V < V <sub>IN</sub> < V <sub>CCIO</sub>	—	−120	—	−160	—	−200	—	−300	—	−500	μA
Bus-hold trip point	V <sub>TRIP</sub>	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

## On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.

## DLL Range Specifications

**Table 2-47: DLL Range Specifications for Arria V GZ Devices**

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Parameter	C3, I3L	C4, I4	Unit
DLL operating frequency range	300 – 890	300 – 890	MHz

## DQS Logic Block Specifications

**Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices**

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$ .

Speed Grade	Min	Max	Unit
C3, I3L	8	15	ps
C4, I4	8	16	ps

**Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Arria V GZ Devices**

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is  $\pm 84 \text{ ps}$  or  $\pm 42 \text{ ps}$ .

Number of DQS Delay Buffers	C3, I3L	C4, I4	Unit
1	30	32	ps
2	60	64	ps
3	90	96	ps

**Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices**

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8