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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### Details

Product Status	Obsolete
Number of LABs/CLBs	11460
Number of Logic Elements/Cells	242000
Total RAM Bits	15470592
Number of I/O	384
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	896-BBGA, FCBGA
Supplier Device Package	896-FBGA (31x31)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5agxba7d6f31c6n">https://www.e-xfl.com/product-detail/intel/5agxba7d6f31c6n</a>

**Caution:** Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 1-1: Absolute Maximum Ratings for Arria V Devices**

Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Core voltage power supply	−0.50	1.43	V
V <sub>CCP</sub>	Periphery circuitry, PCIe® hardIP block, and transceiver physical coding sublayer (PCS) power supply	−0.50	1.43	V
V <sub>CCPGM</sub>	Configuration pins power supply	−0.50	3.90	V
V <sub>CC_AUX</sub>	Auxiliary supply	−0.50	3.25	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	−0.50	3.90	V
V <sub>CCPD</sub>	I/O pre-driver power supply	−0.50	3.90	V
V <sub>CCIO</sub>	I/O power supply	−0.50	3.90	V
V <sub>CCD_FPLL</sub>	Phase-locked loop (PLL) digital power supply	−0.50	1.80	V
V <sub>CCA_FPLL</sub>	PLL analog power supply	−0.50	3.25	V
V <sub>CCA_GXB</sub>	Transceiver high voltage power	−0.50	3.25	V
V <sub>CCH_GXB</sub>	Transmitter output buffer power	−0.50	1.80	V
V <sub>CCR_GXB</sub>	Receiver power	−0.50	1.50	V
V <sub>CCT_GXB</sub>	Transmitter power	−0.50	1.50	V
V <sub>CCL_GXB</sub>	Transceiver clock network power	−0.50	1.50	V
V <sub>I</sub>	DC input voltage	−0.50	3.80	V
V <sub>CC_HPS</sub>	HPS core voltage and periphery circuitry power supply	−0.50	1.43	V
V <sub>CCPD_HPS</sub>	HPS I/O pre-driver power supply	−0.50	3.90	V
V <sub>CCIO_HPS</sub>	HPS I/O power supply	−0.50	3.90	V
V <sub>CCRSTCLK_HPS</sub>	HPS reset and clock input pins power supply	−0.50	3.90	V

Symbol	Description	Condition	Minimum <sup>(7)</sup>	Typical	Maximum <sup>(7)</sup>	Unit
$V_{CCPD\_HPS}^{(8)}$	HPS I/O pre-driver power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
$V_{CCIO\_HPS}$	HPS I/O buffers power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V <sup>(9)</sup>	1.283	1.35	1.418	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins power supply	3.3 V	3.135	3.3	3.465	V
		3.0 V	2.85	3.0	3.15	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
$V_{CCPLL\_HPS}$	HPS PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V

<sup>(7)</sup> The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

<sup>(8)</sup>  $V_{CCPD\_HPS}$  must be 2.5 V when  $V_{CCIO\_HPS}$  is 2.5, 1.8, 1.5, or 1.2 V.  $V_{CCPD\_HPS}$  must be 3.0 V when  $V_{CCIO\_HPS}$  is 3.0 V.  $V_{CCPD\_HPS}$  must be 3.3 V when  $V_{CCIO\_HPS}$  is 3.3 V.

<sup>(9)</sup>  $V_{CCIO\_HPS}$  1.35 V is supported for HPS row I/O bank only.

Parameter	Symbol	Condition	V <sub>CCIO</sub> (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold trip point	V <sub>TRIP</sub>	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

### OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

**Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices**

Calibration accuracy for the calibrated on-chip series termination ( $R_S$  OCT) and on-chip parallel termination ( $R_T$  OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-I3, -C4	-I5, -C5	-C6	
25- $\Omega$ $R_S$	Internal series termination with calibration (25- $\Omega$ setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
50- $\Omega$ $R_S$	Internal series termination with calibration (50- $\Omega$ setting)	$V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
34- $\Omega$ and 40- $\Omega$ $R_S$	Internal series termination with calibration (34- $\Omega$ and 40- $\Omega$ setting)	$V_{CCIO} = 1.5, 1.35, 1.25, 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
48- $\Omega$ , 60- $\Omega$ , and 80- $\Omega$ $R_S$	Internal series termination with calibration (48- $\Omega$ , 60- $\Omega$ , and 80- $\Omega$ setting)	$V_{CCIO} = 1.2$	$\pm 15$	$\pm 15$	$\pm 15$	%
50- $\Omega$ $R_T$	Internal parallel termination with calibration (50- $\Omega$ setting)	$V_{CCIO} = 2.5, 1.8, 1.5, 1.2$	-10 to +40	-10 to +40	-10 to +40	%
20- $\Omega$ , 30- $\Omega$ , 40- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ $R_T$	Internal parallel termination with calibration (20- $\Omega$ , 30- $\Omega$ , 40- $\Omega$ , 60- $\Omega$ , and 120- $\Omega$ setting)	$V_{CCIO} = 1.5, 1.35, 1.25$	-10 to +40	-10 to +40	-10 to +40	%

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to -0.5%	—	—	0 to -0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	$\Omega$
V <sub>ICM</sub> (AC coupled)	—	—	1.1/1.15 <sup>(26)</sup>	—	—	1.1/1.15 <sup>(26)</sup>	—	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	250	—	550	mV
Transmitter REFCLK phase noise <sup>(27)</sup>	10 Hz	—	—	-50	—	—	-50	dBc/Hz
	100 Hz	—	—	-80	—	—	-80	dBc/Hz
	1 KHz	—	—	-110	—	—	-110	dBc/Hz
	10 KHz	—	—	-120	—	—	-120	dBc/Hz
	100 KHz	—	—	-120	—	—	-120	dBc/Hz
	≥1 MHz	—	—	-130	—	—	-130	dBc/Hz
R <sub>REF</sub>	—	—	2000 ±1%	—	—	2000 ±1%	—	$\Omega$

<sup>(26)</sup> For data rate ≤3.2 Gbps, connect V<sub>CCR\_GXBL/R</sub> to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V<sub>CCR\_GXBL/R</sub> to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

<sup>(27)</sup> The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10<sup>-12</sup>.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew <sup>(39)</sup>	×N PMA bonded mode	—	—	500	—	—	500	ps

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4		Transceiver Speed Grade 6		Unit
	Min	Max	Min	Max	
Supported data range	611	6553.6	611	3125	Mbps
fPLL supported data range	611	3125	611	3125	Mbps

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

Symbol/Description	Transceiver Speed Grade 4 and 6		Unit
	Min	Max	
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

**Related Information**

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36
- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)  
Provides more information about the power supply connection for different data rates.

<sup>(39)</sup> This specification is only applicable to channels on one side of the device across two transceiver banks.

## Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL <sup>(40)</sup> , HCSL, and LVDS				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(41)</sup>	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal <sup>(41)</sup>	—	—	400	ps
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 <sup>(42)</sup> /2000	mV
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V <sub>ICM</sub> (AC coupled)	—	—	1.2	—	V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for the PCIe reference clock	250	—	550	mV

<sup>(40)</sup> Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.<sup>(41)</sup> REFCLK performance requires to meet transmitter REFCLK phase noise specification.<sup>(42)</sup> The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Transmitter $\text{REFCLK}$ phase noise <sup>(43)</sup>	10 Hz	—	—	–50	dBc/Hz
	100 Hz	—	—	–80	dBc/Hz
	1 KHz	—	—	–110	dBc/Hz
	10 KHz	—	—	–120	dBc/Hz
	100 KHz	—	—	–120	dBc/Hz
	$\geq 1$ MHz	—	—	–130	dBc/Hz
$R_{\text{REF}}$	—	—	$2000 \pm 1\%$	—	$\Omega$

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$\text{fixedclk}$ clock frequency	PCIe Receiver Detect	—	125	—	MHz
Transceiver Reconfiguration Controller IP ( $\text{mgmt\_clk\_clk}$ ) clock frequency	—	75	—	125	MHz

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS				
Data rate (6-Gbps transceiver) <sup>(44)</sup>	—	611	—	6553.6	Mbps

<sup>(43)</sup> The transmitter  $\text{REFCLK}$  phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER)  $10^{-12}$ , equivalent to 14 sigma.<sup>(44)</sup> To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.



Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

Symbol/Description	Transceiver Speed Grade 3		Unit
	Min	Max	
Interface speed (PMA direct mode)	50	153.6 <sup>(56)</sup> , 161 <sup>(57)</sup>	MHz
Interface speed (single-width mode)	25	187.5	MHz
Interface speed (double-width mode)	25	163.84	MHz

**Related Information**

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36

<sup>(56)</sup> The maximum frequency when core transceiver local routing is selected.

<sup>(57)</sup> The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{\text{OUTPJ\_DC}}^{(67)}$	Period jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTPJ\_DC}}^{(67)}$	Period jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 <sup>(68)</sup> , 175 <sup>(69)</sup>	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 <sup>(68)</sup> , 17.5 <sup>(69)</sup>	mUI (p-p)
$t_{\text{OUTCCJ\_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	175	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ\_DC}}^{(67)}$	Cycle-to-cycle jitter for dedicated clock output in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	250 <sup>(68)</sup> , 175 <sup>(69)</sup>	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	25 <sup>(68)</sup> , 17.5 <sup>(69)</sup>	mUI (p-p)
$t_{\text{OUTPJ\_IO}}^{(67)(70)}$	Period jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ\_IO}}^{(67)(68)(70)}$	Period jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ\_IO}}^{(67)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ\_IO}}^{(67)(68)(70)}$	Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL	$F_{\text{OUT}} \geq 100 \text{ MHz}$	—	—	600	ps (p-p)
		$F_{\text{OUT}} < 100 \text{ MHz}$	—	—	60	mUI (p-p)

<sup>(67)</sup> Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

<sup>(68)</sup> This specification only covered fractional PLL for low bandwidth. The  $f_{\text{VCO}}$  for fractional value range 0.05–0.95 must be  $\geq 1000 \text{ MHz}$ .

<sup>(69)</sup> This specification only covered fractional PLL for low bandwidth. The  $f_{\text{VCO}}$  for fractional value range 0.20–0.80 must be  $\geq 1200 \text{ MHz}$ .

<sup>(70)</sup> External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smp1sel` via the system manager. `drvsel` can be set from 1 to 7 and `smp1sel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

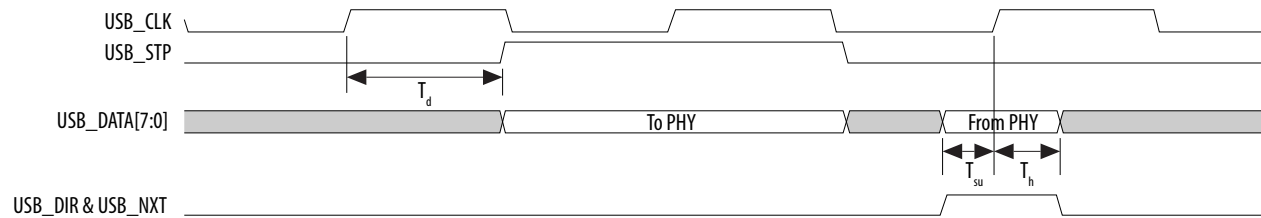
The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

Symbol	Description	Min	Max	Unit
$T_{\text{sdmmc\_clk}}$ (internal reference clock)	SDMMC_CLK clock period (Identification mode)	20	—	ns
	SDMMC_CLK clock period (Default speed mode)	5	—	ns
	SDMMC_CLK clock period (High speed mode)	5	—	ns
$T_{\text{sdmmc\_clk\_out}}$ (interface output clock)	SDMMC_CLK_OUT clock period (Identification mode)	2500	—	ns
	SDMMC_CLK_OUT clock period (Default speed mode)	40	—	ns
	SDMMC_CLK_OUT clock period (High speed mode)	20	—	ns
$T_{\text{duty cycle}}$	SDMMC_CLK_OUT duty cycle	45	55	%
$T_d$	SDMMC_CMD/SDMMC_D output delay	$(T_{\text{sdmmc\_clk}} \times \text{drvsel})/2 - 1.23^{(87)}$	$(T_{\text{sdmmc\_clk}} \times \text{drvsel})/2 + 1.69^{(87)}$	ns
$T_{\text{su}}$	Input setup time	$1.05 - (T_{\text{sdmmc\_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns
$T_h$	Input hold time	$(T_{\text{sdmmc\_clk}} \times \text{smp1sel})/2^{(88)}$	—	ns

<sup>(87)</sup> `drvsel` is the drive clock phase shift select value.

<sup>(88)</sup> `smp1sel` is the sample clock phase shift select value.

Figure 1-12: USB Timing Diagram

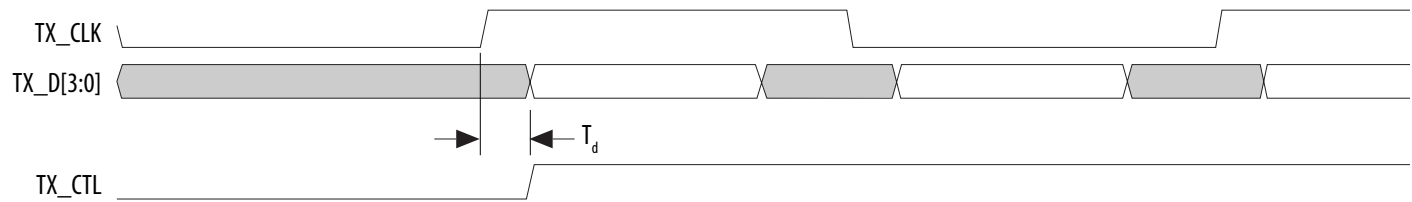


Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
$T_{clk}$ (1000Base-T)	TX_CLK clock period	—	8	—	ns
$T_{clk}$ (100Base-T)	TX_CLK clock period	—	40	—	ns
$T_{clk}$ (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{duty cycle}$	TX_CLK duty cycle	45	—	55	%
$T_d$	TX_CLK to TXD/TX_CTL output data delay	-0.85	—	0.15	ns

Figure 1-13: RGMII TX Timing Diagram



Symbol	Parameter	Minimum	Maximum	Unit
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1506 <sup>(94)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1506 <sup>(95)</sup>	μs
t <sub>CF2CK</sub> <sup>(96)</sup>	nCONFIG high to first rising edge on DCLK	1506	—	μs
t <sub>ST2CK</sub> <sup>(96)</sup>	nSTATUS high to first rising edge of DCLK	2	—	μs
t <sub>DSU</sub>	DATA[ ] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA[ ] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CL</sub>	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CLK</sub>	DCLK period	$1/f_{\text{MAX}}$	—	s
f <sub>MAX</sub>	DCLK frequency (FPP × 8/ × 16)	—	125	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(97)</sup>	175	437	μs
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4× maximum DCLK period	—	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (T <sub>init</sub> × CLKUSR period)	—	—
T <sub>init</sub>	Number of clock cycles required for device initialization	8,576	—	Cycles

**Related Information****FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

<sup>(94)</sup> You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

<sup>(95)</sup> You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

<sup>(96)</sup> If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

<sup>(97)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

## FPP Configuration Timing when DCLK-to-DATA[] &gt;1

Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is &gt;1 for Arria V Devices

Use these timing parameters when you use the decompression and design security features.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	μs
$t_{STATUS}$	nSTATUS low pulse width	268	1506 <sup>(98)</sup>	μs
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1506 <sup>(99)</sup>	μs
$t_{CF2CK}^{(100)}$	nCONFIG high to first rising edge on DCLK	1506	—	μs
$t_{ST2CK}^{(100)}$	nSTATUS high to first rising edge of DCLK	2	—	μs
$t_{DSU}$	DATA[] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA[] hold time after rising edge on DCLK	$N - 1/f_{DCLK}^{(101)}$	—	s
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency (FPP ×8/ ×16)	—	125	MHz
$t_R$	Input rise time	—	40	ns
$t_F$	Input fall time	—	40	ns
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(102)</sup>	175	437	μs

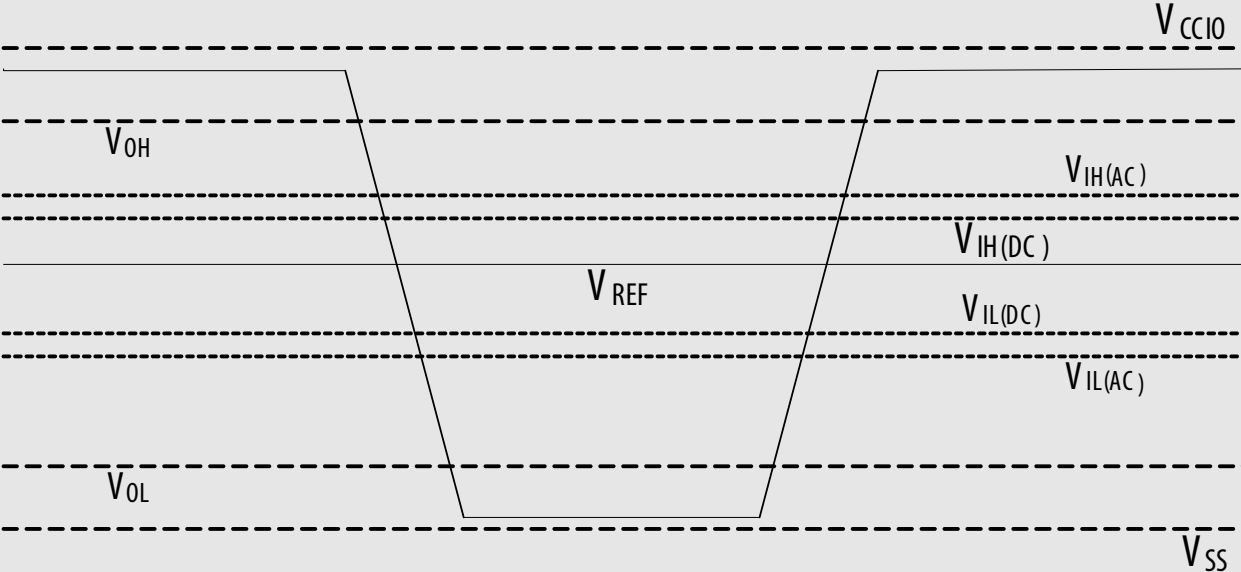
<sup>(98)</sup> This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

<sup>(99)</sup> This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

<sup>(100)</sup> If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

<sup>(101)</sup>  $N$  is the DCLK-to-DATA[] ratio and  $f_{DCLK}$  is the DCLK frequency of the system.

<sup>(102)</sup> The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Term	Definition
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p> 
$t_C$	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
$t_{DUTY}$	High-speed I/O block—Duty cycle on high-speed transmitter output clock.

Date	Version	Changes
November 2012	3.0	<ul style="list-style-type: none"> <li>Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.</li> <li>Removed table: Transceiver Block Jitter Specifications for Arria V Devices.</li> <li>Added HPS information: <ul style="list-style-type: none"> <li>Added “HPS Specifications” section.</li> <li>Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.</li> <li>Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.</li> <li>Updated Table 3 and Table 5.</li> </ul> </li> </ul>
October 2012	2.4	<ul style="list-style-type: none"> <li>Updated Arria V GX <math>V_{CCR\_GXBL/R}</math>, <math>V_{CCT\_GXBL/R}</math>, and <math>V_{CCL\_GXBL/R}</math> minimum and maximum values, and data rate in Table 4.</li> <li>Added receiver <math>V_{ICM}</math> (AC coupled) and <math>V_{ICM}</math> (DC coupled) values, and transmitter <math>V_{OCM}</math> (AC coupled) and <math>V_{OCM}</math> (DC coupled) values in Table 20 and Table 21.</li> </ul>
August 2012	2.3	Updated the SERDES factor condition in Table 30.
July 2012	2.2	<ul style="list-style-type: none"> <li>Updated the maximum voltage for <math>V_I</math> (DC input voltage) in Table 1.</li> <li>Updated Table 20 to include the Arria V GX -I3 speed grade.</li> <li>Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.</li> <li>Updated the SERDES factor condition in Table 30.</li> <li>Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade.</li> </ul>
June 2012	2.1	Updated $V_{CCR\_GXBL/R}$ , $V_{CCT\_GXBL/R}$ , and $V_{CCL\_GXBL/R}$ values in Table 4.



Date	Version	Changes
June 2012	2.0	<ul style="list-style-type: none"><li>• Updated for the Quartus II software v12.0 release:</li><li>• Restructured document.</li><li>• Updated “Supply Current and Power Consumption” section.</li><li>• Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52.</li><li>• Added Table 22, Table 23, and Table 33.</li><li>• Added Figure 1–1 and Figure 1–2.</li><li>• Added “Initialization” and “Configuration Files” sections.</li></ul>
February 2012	1.3	<ul style="list-style-type: none"><li>• Updated Table 2–1.</li><li>• Updated Transceiver-FPGA Fabric Interface rows in Table 2–20.</li><li>• Updated <math>V_{CCP}</math> description.</li></ul>
December 2011	1.2	Updated Table 2–1 and Table 2–3.
November 2011	1.1	<ul style="list-style-type: none"><li>• Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36.</li><li>• Added Table 2–5.</li><li>• Added Figure 2–4.</li></ul>
August 2011	1.0	Initial release.

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
25-Ω R <sub>S</sub>	Internal series termination without calibration (25-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.8 and 1.5 V	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50-Ω setting)	V <sub>CCIO</sub> = 1.2 V	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100-Ω setting)	V <sub>CCIO</sub> = 2.5 V	±25	±25	%

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{OCT} = R_{SCAL} \left( 1 + \left( \frac{dR}{dT} \times \Delta T \right) \pm \left( \frac{dR}{dV} \times \Delta V \right) \right)$$

Notes:

1. The R<sub>OCT</sub> value shows the range of OCT resistance with the variation of temperature and V<sub>CCIO</sub>.
2. R<sub>SCAL</sub> is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
5. dR/dT is the percentage change of R<sub>SCAL</sub> with temperature.
6. dR/dV is the percentage change of R<sub>SCAL</sub> with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices

Valid for a V<sub>CCIO</sub> range of ±5% and a temperature range of 0° to 85°C.

## CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{\text{pll\_powerdown}}$ <sup>(153)</sup>	—	1	—	—	1	—	—	μs
$t_{\text{pll\_lock}}$ <sup>(154)</sup>	—		—	10	—	—	10	μs

## Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

## ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

<sup>(153)</sup>  $t_{\text{pll\_powerdown}}$  is the PLL powerdown minimum pulse width.

<sup>(154)</sup>  $t_{\text{pll\_lock}}$  is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Clock Network	ATX PLL			CMU PLL <sup>(161)</sup>			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
xN (PCIe)	—	8.0	8	—	5.0	8	—	—	—
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
	—	8.01 to 9.8304	Up to 7 channels above and below PLL						

## Standard PCS Data Rate

**Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices**

The maximum data rate is also constrained by the transceiver speed grade. Refer to the “Commercial and Industrial Speed Grade Offering for Arria V GZ Devices” table for the transceiver speed grade.

Mode <sup>(164)</sup>	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	2	C3, I3L core speed grade	9.9	9	7.84	7.2	5.3	4.7	4.24	3.76
	3	C4, I4 core speed grade	8.8	8.2	7.2	6.56	4.8	4.3	3.84	3.44

<sup>(161)</sup> ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

<sup>(164)</sup> The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

## JTAG Configuration Specifications

**Table 2-54: JTAG Timing Parameters and Values for Arria V GZ Devices**

Symbol	Description	Min	Max	Unit
$t_{JCP}$	TCK clock period	30	—	ns
$t_{JCP}$	TCK clock period	167 <sup>(203)</sup>	—	ns
$t_{JCH}$	TCK clock high time	14	—	ns
$t_{JCL}$	TCK clock low time	14	—	ns
$t_{JPSU}$ (TDI)	TDI JTAG port setup time	2	—	ns
$t_{JPSU}$ (TMS)	TMS JTAG port setup time	3	—	ns
$t_{JPH}$	JTAG port hold time	5	—	ns
$t_{JPCO}$	JTAG port clock to output	—	11 <sup>(204)</sup>	ns
$t_{JPZX}$	JTAG port high impedance to valid output	—	14 <sup>(204)</sup>	ns
$t_{JPXZ}$	JTAG port valid output to high impedance	—	14 <sup>(204)</sup>	ns

## Fast Passive Parallel (FPP) Configuration Timing

### DCLK-to-DATA[ ] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[ ] ratio when you turn on encryption or the compression feature.

<sup>(203)</sup> The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

<sup>(204)</sup> A 1-ns adder is required for each V<sub>CCIO</sub> voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if V<sub>CCIO</sub> of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.