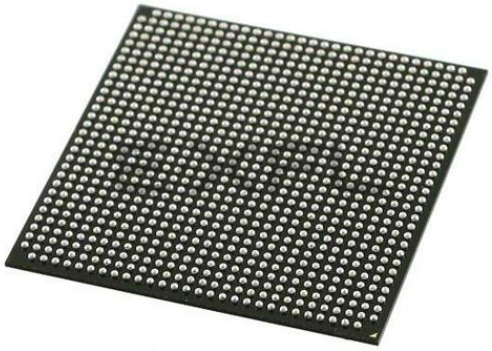

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 14151 |
| Number of Logic Elements/Cells | 300000 |
| Total RAM Bits | 17358848 |
| Number of I/O | 384 |
| Number of Gates | - |
| Voltage - Supply | 1.07V ~ 1.13V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 896-BBGA, FCBGA |
| Supplier Device Package | 896-FBGA (31x31) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5agxbb1d4f31c5n |

## I/O Pin Leakage Current

### Table 1-6: I/O Pin Leakage Current for Arria V Devices

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

## Bus Hold Specifications

### Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |

## I/O Standard Specifications

Tables in this section list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Arria V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

### Single-Ended I/O Standards

**Table 1-14: Single-Ended I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[13] (mA) | $I_{OH}$[13] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

(13) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew[39] | ×*N* PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices**

| Symbol/Description | Transceiver Speed Grade 4 | | Transceiver Speed Grade 6 | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Supported data range | 611 | 6553.6 | 611 | 3125 | Mbps |
| fPLL supported data range | 611 | 3125 | 611 | 3125 | Mbps |

**Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices**

| Symbol/Description | Transceiver Speed Grade 4 and 6 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

**Related Information**

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36
- **Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines**
  Provides more information about the power supply connection for different data rates.

[39] This specification is only applicable to channels on one side of the device across two transceiver banks.

**Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices**

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Interface speed (PMA direct mode) | 50 | 153.6[56], 161[57] | MHz |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

**Related Information**

- **CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-35
- **CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain** on page 1-36

[56] The maximum frequency when core transceiver local routing is selected.
[57] The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

For example, when $V_{OD}$ = 800 mV, the corresponding $V_{OD}$ value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

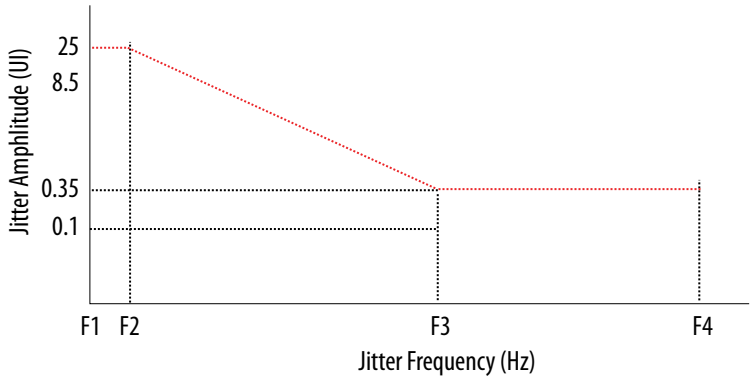
To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices**

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | dB |
| 1 | 1.97 | 0.88 | 0.43 | 0.32 | 0.24 | 0.19 | 0.13 | dB |
| 2 | 3.58 | 1.67 | 0.95 | 0.76 | 0.61 | 0.5 | 0.41 | dB |
| 3 | 5.35 | 2.48 | 1.49 | 1.2 | 1 | 0.83 | 0.69 | dB |
| 4 | 7.27 | 3.31 | 2 | 1.63 | 1.36 | 1.14 | 0.96 | dB |
| 5 | — | 4.19 | 2.55 | 2.1 | 1.76 | 1.49 | 1.26 | dB |
| 6 | — | 5.08 | 3.11 | 2.56 | 2.17 | 1.83 | 1.56 | dB |
| 7 | — | 5.99 | 3.71 | 3.06 | 2.58 | 2.18 | 1.87 | dB |
| 8 | — | 6.92 | 4.22 | 3.47 | 2.93 | 2.48 | 2.11 | dB |
| 9 | — | 7.92 | 4.86 | 4 | 3.38 | 2.87 | 2.46 | dB |
| 10 | — | 9.04 | 5.46 | 4.51 | 3.79 | 3.23 | 2.77 | dB |
| 11 | — | 10.2 | 6.09 | 5.01 | 4.23 | 3.61 | — | dB |
| 12 | — | 11.56 | 6.74 | 5.51 | 4.68 | 3.97 | — | dB |
| 13 | — | 12.9 | 7.44 | 6.1 | 5.12 | 4.36 | — | dB |
| 14 | — | 14.44 | 8.12 | 6.64 | 5.57 | 4.76 | — | dB |
| 15 | — | — | 8.87 | 7.21 | 6.06 | 5.14 | — | dB |

## LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

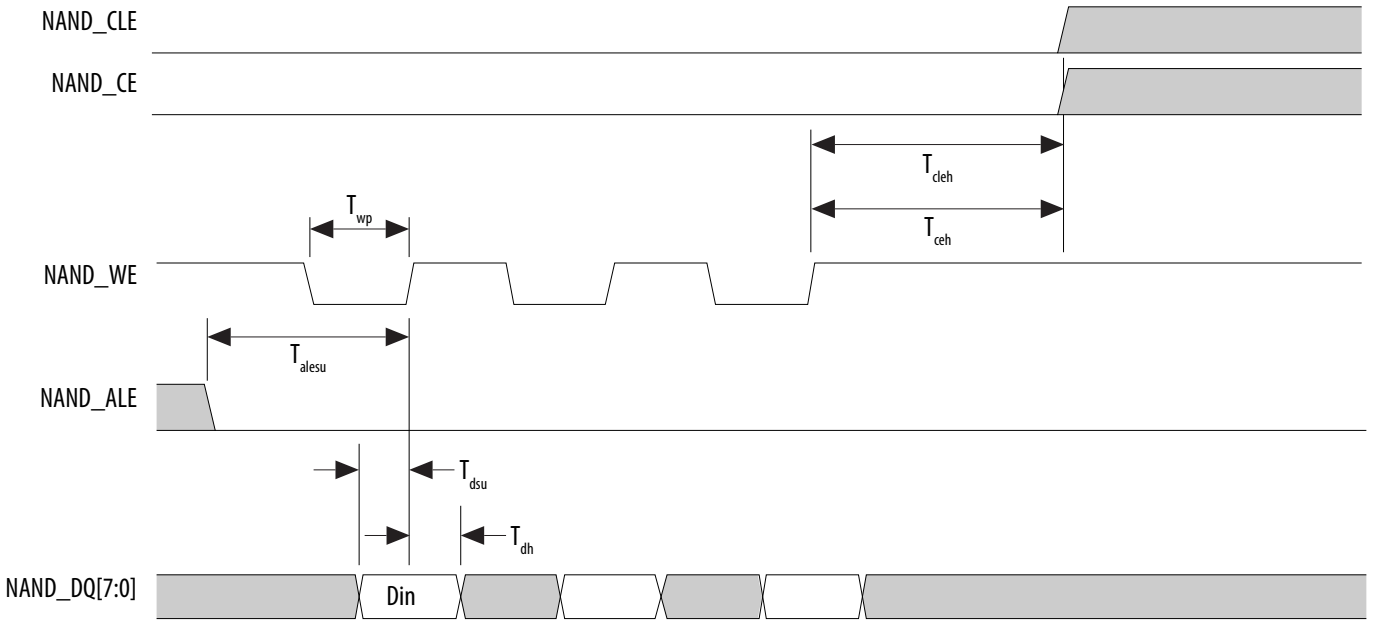
### Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps




### Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

**Figure 1-19: NAND Data Write Timing Diagram**



The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

**Arria V I/O Timing Spreadsheet**
Provides the Arria V Excel-based I/O timing spreadsheet.

## Programmable IOE Delay

**Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices**

| Parameter[112] | Available Settings | Minimum Offset[113] | Fast Model | | Slow Model | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | –C4 | –C5 | –C6 | –I3 | –I5 | |
| D1 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |
| D3 | 8 | 0 | 1.763 | 1.795 | 2.999 | 3.496 | 3.571 | 3.031 | 3.643 | ns |
| D4 | 32 | 0 | 0.508 | 0.518 | 0.869 | 1.063 | 1.063 | 1.063 | 1.057 | ns |
| D5 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |

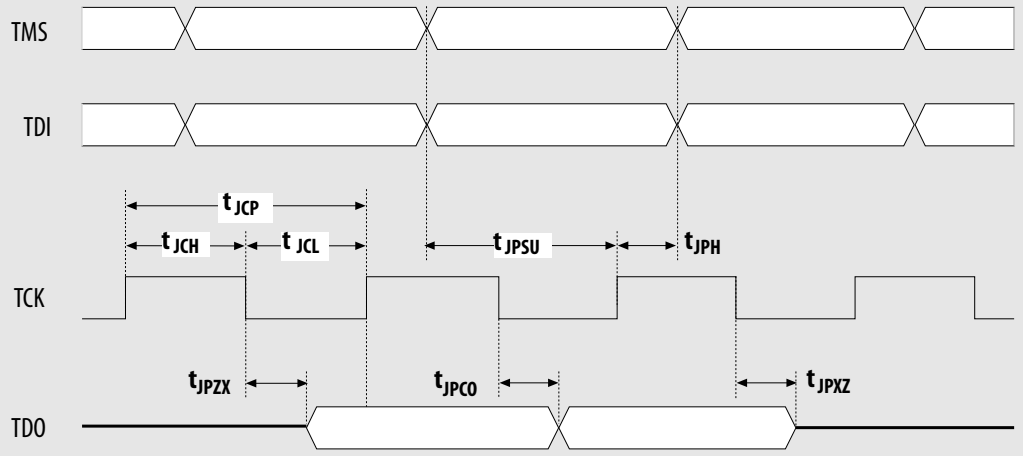
## Programmable Output Buffer Delay

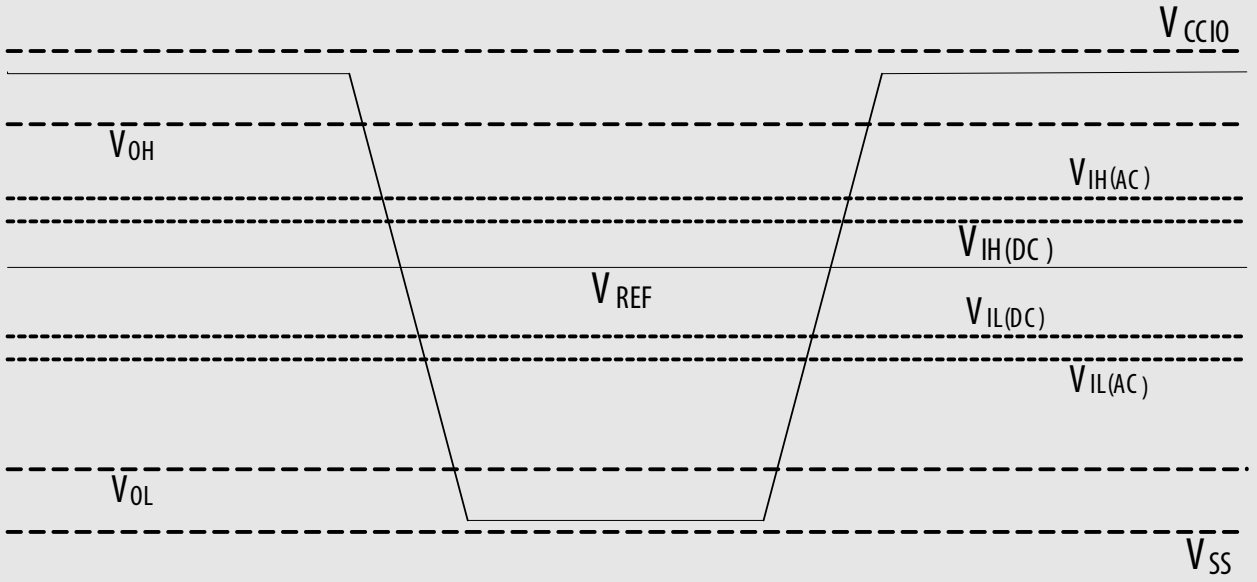
**Table 1-77: Programmable Output Buffer Delay for Arria V Devices**

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

(112) You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.
(113) Minimum offset does not include the intrinsic delay.

| Term | Definition |
|---|---|
| JTAG timing specifications | JTAG Timing Specifications  |

| Term | Definition |
|---|---|
| Single-ended voltage referenced I/O standard | The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.<br>Single-Ended Voltage Referenced I/O Standard<br>  |
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on high-speed transmitter output clock. |

| Date | Version | Changes |
|---|---|---|
| August 2013 | 3.5 | • Removed "Pending silicon characterization" note in Table 29.<br>• Updated Table 25. |
| August 2013 | 3.4 | • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64.<br>• Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29. |
| June 2013 | 3.3 | Updated Table 20, Table 21, Table 25, and Table 38. |
| May 2013 | 3.2 | • Added Table 37.<br>• Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23.<br>• Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64.<br>• Updated industrial junction temperature range for –I3 speed grade in "PLL Specifications" section. |
| March 2013 | 3.1 | • Added HPS reset information in the "HPS Specifications" section.<br>• Added Table 60.<br>• Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59.<br>• Updated Figure 21. |

| Symbol | Description | Condition | Minimum[114] | Typical | Maximum [114] | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

## Recommended Transceiver Power Supply Operating Conditions

**Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices**

| Symbol | Description | Minimum [118] | Typical | Maximum[118] | Unit |
|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ [119], [120] | Transceiver channel PLL power supply (left side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA\_GXBR}$ [119], [120] | Transceiver channel PLL power supply (right side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side) | 0.82 | 0.85 | 0.88 | V |

(114) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(118) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(119) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(120) When using ATX PLLs, the supply must be 3.0 V.

| Symbol | Description | Conditions | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 2.5 V | ±25 | ±25 | % |

**Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices**

$$R_{OCT} = R_{SCAL}\left(1 + \left(\frac{dR}{dT} \times \triangle T\right) \pm \left(\frac{dR}{dV} \times \triangle V\right)\right)$$

Notes:
1. The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
2. $R_{SCAL}$ is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
5. dR/dT is the percentage change of $R_{SCAL}$ with temperature.
6. dR/dV is the percentage change of $R_{SCAL}$ with voltage.

**Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ Devices**

Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

| I/O Standard | $V_{CCIO}$ (V) [128] | | | $V_{ID}$ (mV) [129] | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) [130] | | | $V_{OCM}$ (V) [130] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| RSDS (HIO) [133] | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) [134] | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL [135], [136] | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Related Information**

**Glossary** on page 2-73

[128] Differential inputs are powered by VCCPD which requires 2.5 V.
[129] The minimum VID value is applicable over the entire common mode range, VCM.
[130] RL range: 90 ≤ RL ≤ 110 Ω.
[133] For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.
[134] For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.
[135] LVPECL is only supported on dedicated clock input pins.
[136] For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{INCCJ}$ (171), (172) | Input clock cycle-to-cycle jitter ($f_{REF}$ ≥ 100 MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{REF}$ < 100 MHz) | -750 | — | +750 | ps (p-p) |
| $t_{OUTPJ\_DC}$ (173) | Period Jitter for dedicated clock output in integer PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output in integer PLL ($f_{OUT}$ < 100 Mhz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTPJ\_DC}$ (173) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 250(176), 175(174) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT}$ < 100 MHz) | — | — | 25(176), 17.5 (174) | mUI (p-p) |
| $t_{OUTCCJ\_DC}$ (173) | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT}$ < 100 MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ\_DC}$ (173) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 250(176), 175 (174) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT}$ < 100 MHz) | — | — | 25(176), 17.5 (174) | mUI (p-p) |

(171) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.
(172) The $f_{REF}$ is fIN/N specification applies when N = 1.
(173) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.
(174) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197) | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS RX with DPA (193), (195), (196), (197) | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (198) | — | (200) | (198) | — | (200) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |

(192) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
(193) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.
(194) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.
(195) Requires package skew compensation with PCB trace length.
(196) Do not mix single-ended I/O buffer within LVDS I/O bank.
(197) Chip-to-chip communication only with a maximum load of 5 pF.
(198) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(199) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.
(200) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

**Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

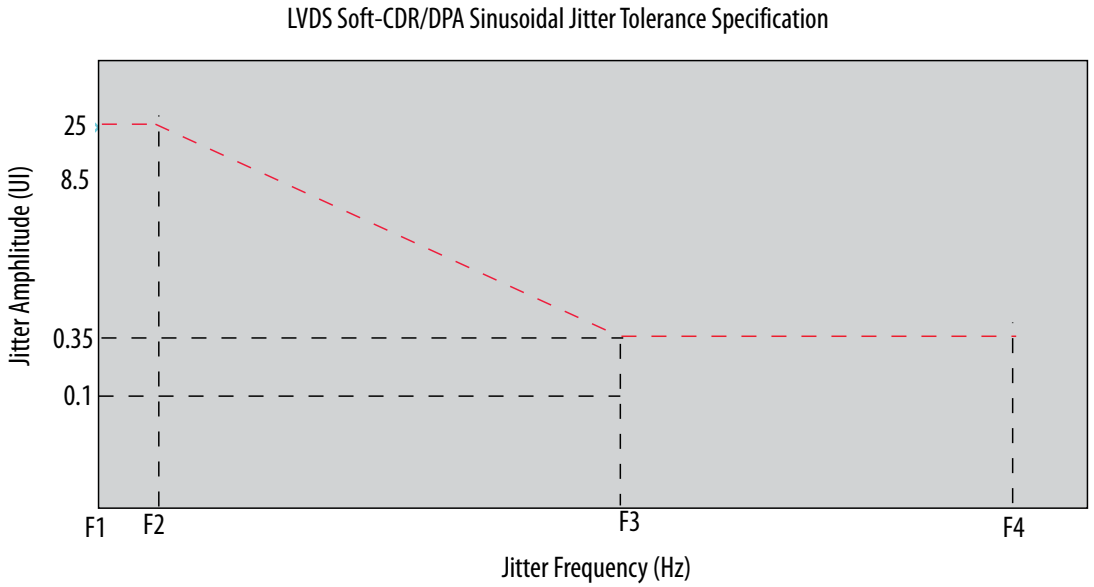



**Table 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps**

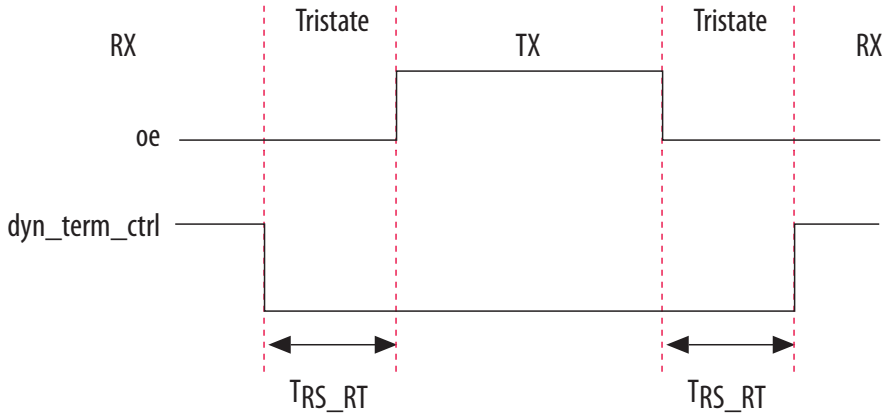
| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

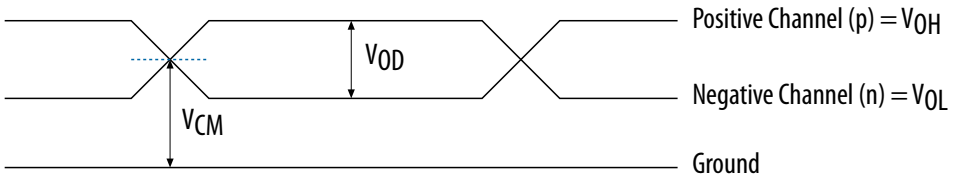
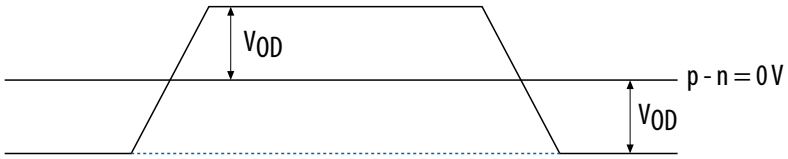
## OCT Calibration Block Specifications

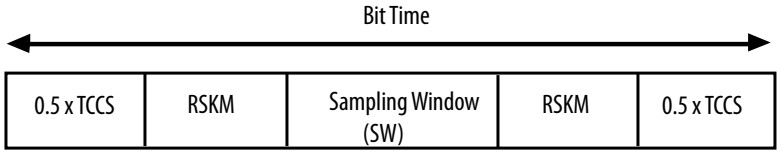
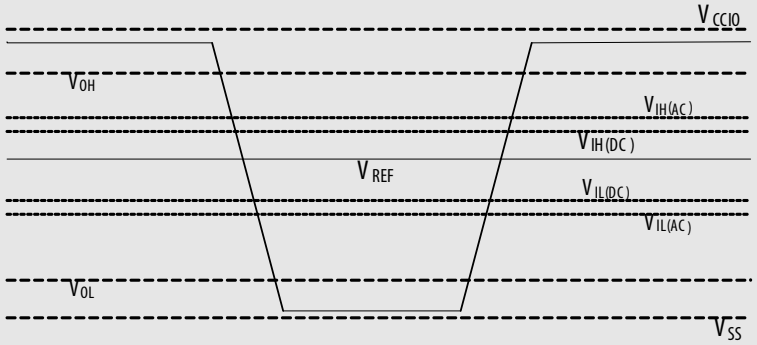
**Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS\_RT}$ | Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (See the figure below.) | — | 2.5 | — | ns |

**Figure 2-6: Timing Diagram for `oe` and `dyn_term_ctrl` Signals**



| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br> |
| $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |

| Term | Definition |
|---|---|
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V GZ device). |
| SW (sampling window) | Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:<br>  |
| Single-ended voltage referenced I/O standard | The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>Single-Ended Voltage Referenced I/O Standard<br>  |