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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	14151
Number of Logic Elements/Cells	300000
Total RAM Bits	17358848
Number of I/O	544
Number of Gates	-
Voltage - Supply	1.07V ~ 1.13V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA Exposed Pad
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5agxbb1d4f35c5n

Symbol	Description	Minimum	Maximum	Unit
V _{CCPLL_HPS}	HPS PLL analog power supply	–0.50	3.25	V
V _{CC_AUX_SHARED}	HPS auxiliary power supply	–0.50	3.25	V
I _{OUT}	DC output current per pin	–25	40	mA
T _J	Operating junction temperature	–55	125	°C
T _{STG}	Storage temperature (no bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			-I3, -C4	-I5, -C5	-C6	
60- Ω and 120- Ω R _T	Internal parallel termination with calibration (60- Ω and 120- Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	-10 to +40	%
25- Ω R _{S_left_shift}	Internal left shift series termination with calibration (25- Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

OCT Without Calibration Resistance Tolerance Specifications

Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	ResistanceTolerance			Unit
			-I3, -C4	-I5, -C5	-C6	
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
25- Ω R _S	Internal series termination without calibration (25- Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 3.0, 2.5	±30	±40	±40	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.8, 1.5	±30	±40	±40	%
50- Ω R _S	Internal series termination without calibration (50- Ω setting)	V _{CCIO} = 1.2	±35	±50	±50	%
100- Ω R _D	Internal differential termination (100- Ω setting)	V _{CCIO} = 2.5	±25	±40	±40	%

I/O Standard	V _{CCIO} (V)			V _{ID} (mV) ⁽¹⁶⁾			V _{ICM(DC)} (V)			V _{OD} (V) ⁽¹⁷⁾			V _{OCM} (V) ⁽¹⁷⁾⁽¹⁸⁾		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables.														
2.5 V LVDS ⁽¹⁹⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.05	D _{MAX} ≤ 1.25 Gbps	1.80	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	D _{MAX} > 1.25 Gbps	1.55						
RSDS (HIO) ⁽²⁰⁾	2.375	2.5	2.625	100	V _{CM} = 1.25 V	—	0.25	—	1.45	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) ⁽²¹⁾	2.375	2.5	2.625	200	—	600	0.300	—	1.425	0.25	—	0.6	1	1.2	1.4
LVPECL ⁽²²⁾	—	—	—	300	—	—	0.60	D _{MAX} ≤ 700 Mbps	1.80	—	—	—	—	—	—
							1.00	D _{MAX} > 700 Mbps	1.60						

Related Information

- [Transceiver Specifications for Arria V GX and SX Devices](#) on page 1-23
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

⁽¹⁶⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

⁽¹⁷⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽¹⁸⁾ This applies to default pre-emphasis setting only.

⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.

⁽²⁰⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

- [Transceiver Specifications for Arria V GT and ST Devices](#) on page 1-29
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²³⁾ , HCSL, and LVDS							
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽²⁴⁾	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽²⁴⁾	—	—	400	—	—	400	ps
Duty cycle	—	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	300 ⁽²⁵⁾ / 2000	200	—	300 ⁽²⁵⁾ / 2000	mV

⁽²³⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

⁽²⁴⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.

⁽²⁵⁾ The maximum peak-to-peak differential input voltage of 300 mV is allowed for DC coupled link.

Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Run length	—	—	—	200	—	—	200	UI
Programmable equalization AC and DC gain	AC gain setting = 0 to 3 ⁽³⁸⁾ DC gain setting = 0 to 1	Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams.						dB

Table 1-23: Transmitter Specifications for Arria V GX and SX Devices

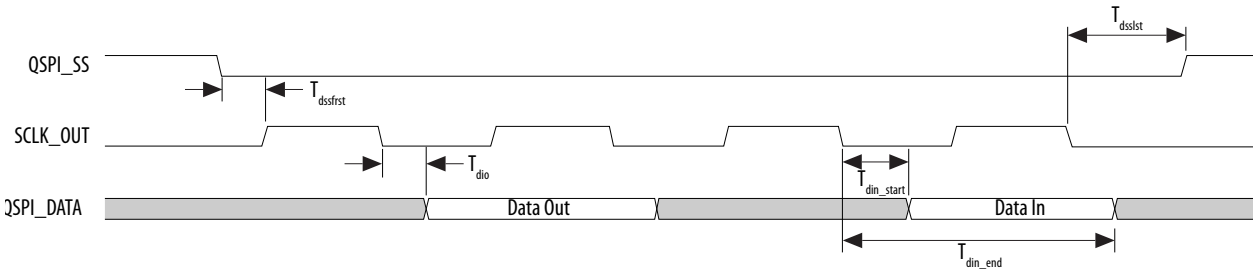
Symbol/Description	Condition	Transceiver Speed Grade 4			Transceiver Speed Grade 6			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported I/O standards	1.5 V PCML							
Data rate	—	611	—	6553.6	611	—	3125	Mbps
V _{OCM} (AC coupled)	—	—	650	—	—	650	—	mV
V _{OCM} (DC coupled)	≤ 3.2Gbps ⁽³²⁾	670	700	730	670	700	730	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	Ω
Intra-differential pair skew	TX V _{CM} = 0.65 V (AC coupled) and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	×6 PMA bonded mode	—	—	180	—	—	180	ps

⁽³⁷⁾ The rate match FIFO supports only up to ±300 parts per million (ppm).⁽³⁸⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

Symbol	Description	Min	Typ	Max	Unit
T_{din_end}	Input data valid end	$(2 + R_{delay}) \times T_{qspi_clk} - 1.21^{(85)}$	—	—	ns

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.



Related Information

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics

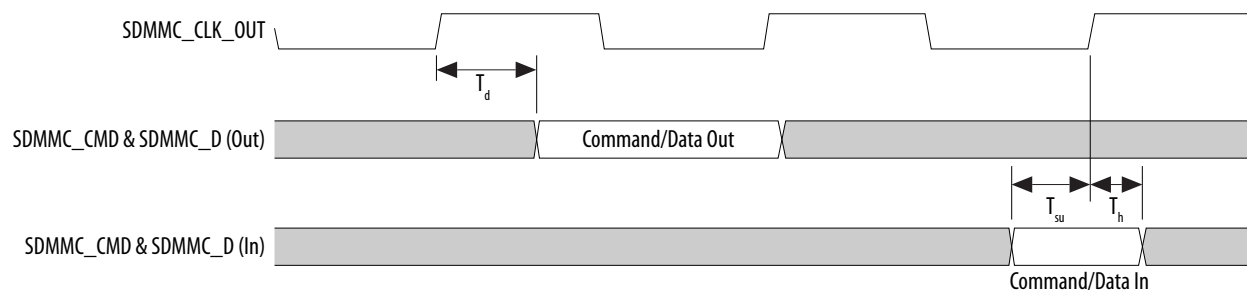
Table 1-52: SPI Master Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

Symbol	Description	Min	Max	Unit
T_{clk}	CLK clock period	16.67	—	ns
T_{su}	SPI Master-in slave-out (MISO) setup time	8.35 ⁽⁸⁶⁾	—	ns

⁽⁸⁵⁾ R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay} , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

Figure 1-11: SD/MMC Timing Diagram

**Related Information**

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual

Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

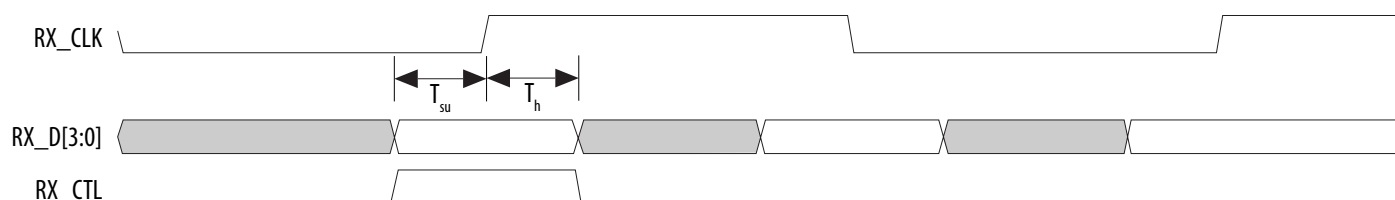
PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	USB CLK clock period	—	16.67	—	ns
T_d	CLK to USB_STP/USB_DATA[7:0] output delay	4.4	—	11	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	2	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Table 1-57: RGMII RX Timing Requirements for Arria V Devices

Symbol	Description	Min	Typ	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	ns
T_{clk} (10Base-T)	RX_CLK clock period	—	400	ns
T_{su}	RX_D/RX_CTL setup time	1	—	ns
T_h	RX_D/RX_CTL hold time	1	—	ns

Figure 1-14: RGMII RX Timing Diagram**Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices**

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	—	400	—	ns
T_d	MDC to MDIO output data delay	10	—	20	ns
T_s	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Symbol	Parameter	Minimum	Maximum	Unit
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS $\times 1$ and $\times 4$ Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding $nSTATUS$ low.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before the falling edge on DCLK	1.5	—	ns
t_{DH}	Data hold time after the falling edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	μs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times \text{maximum DCLK period}$	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$	—	—
T_{init}	Number of clock cycles required for device initialization	8,576	—	Cycles

Variant	Member Code	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits)
Arria V GX	A1	71,015,712	439,960
	A3	71,015,712	439,960
	A5	101,740,800	446,360
	A7	101,740,800	446,360
	B1	137,785,088	457,368
	B3	137,785,088	457,368
	B5	185,915,808	463,128
	B7	185,915,808	463,128
Arria V GT	C3	71,015,712	439,960
	C7	101,740,800	446,360
	D3	137,785,088	457,368
	D7	185,915,808	463,128
Arria V SX	B3	185,903,680	450,968
	B5	185,903,680	450,968
Arria V ST	D3	185,903,680	450,968
	D5	185,903,680	450,968

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Arria V I/O Timing Spreadsheet](#)

Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

Parameter ⁽¹¹²⁾	Available Settings	Minimum Offset ⁽¹¹³⁾	Fast Model		Slow Model					Unit
			Industrial	Commercial	–C4	–C5	–C6	–I3	–I5	
D1	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns
D3	8	0	1.763	1.795	2.999	3.496	3.571	3.031	3.643	ns
D4	32	0	0.508	0.518	0.869	1.063	1.063	1.063	1.057	ns
D5	32	0	0.508	0.517	0.870	1.063	1.063	0.872	1.057	ns

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

⁽¹¹²⁾ You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹¹³⁾ Minimum offset does not include the intrinsic delay.

Term	Definition
JTAG timing specifications	<p>JTAG Timing Specifications</p> <p>The diagram illustrates the timing relationships between JTAG signals TMS, TDI, TCK, and TDO. TMS and TDI are high-impedance signals that transition between high and low states. TCK is a clock signal with specific timing parameters: t_{JCH} (setup time before TCK rising edge), t_{JCL} (hold time after TCK falling edge), t_{JPSU} (setup time before TCK rising edge), and t_{JPH} (hold time after TCK falling edge). TDO is a data output signal that transitions between high and low states. Timing parameters for TDO include t_{JPZX} (setup time before TCK rising edge), t_{JPCO} (hold time after TCK falling edge), and t_{JPXZ} (hold time after TCK falling edge).</p>

Symbol	Description	Minimum	Maximum	Unit
V_I	DC input voltage	-0.5	3.8	V
T_J	Operating junction temperature	-55	125	°C
T_{STG}	Storage temperature (No bias)	-65	150	°C
I_{OUT}	DC output current per pin	-25	40	mA

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

Symbol	Description	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	-0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	-0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	-0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	-0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	-0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	-0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	-0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	-0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	-0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	-0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	-0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Symbol	Description	Conditions	Calibration Accuracy		Unit
			C3, I3L	C4, I4	
25-Ω R _S	Internal series termination with calibration (25-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
50-Ω R _S	Internal series termination with calibration (50-Ω setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%
34-Ω and 40-Ω R _S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V	±15	±15	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V _{CCIO} = 1.2 V	±15	±15	%
50-Ω R _T	Internal parallel termination with calibration (50-Ω setting)	V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V	-10 to +40	-10 to +40	%
20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V _{CCIO} = 1.5, 1.35, 1.25 V	-10 to +40	-10 to +40	%
60-Ω and 120-Ω R _T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V _{CCIO} = 1.2	-10 to +40	-10 to +40	%
25-Ω R _{S_left_shift}	Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting)	V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	%

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

Symbol	Description	Conditions	Resistance Tolerance		Unit
			C3, I3L	C4, I4	
25-Ω R, 50-Ω R _S	Internal series termination without calibration (25-Ω setting)	V _{CCIO} = 3.0 and 2.5 V	±40	±40	%

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
R _{REF}	—	—	1800 ±1%	—	—	1800 ±1%	—	Ω

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Transceiver Clocks**Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁴¹⁾ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors	85- Ω setting	—	85 \pm 20%	—	—	85 \pm 20%	—	Ω
	100- Ω setting	—	100 \pm 20%	—	—	100 \pm 20%	—	Ω
	120- Ω setting	—	120 \pm 20%	—	—	120 \pm 20%	—	Ω
	150- Ω setting	—	150 \pm 20%	—	—	150 \pm 20%	—	Ω
V _{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	mV
V _{OCM} (DC coupled)	—	—	650	—	—	650	—	mV
Intra-differential pair skew	Tx V _{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	ps
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	ps

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

Symbol/Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Supported data range	—	600	—	12500	600	—	10312.5	Mbps
$t_{\text{pll_powerdown}}$ ⁽¹⁵³⁾	—	1	—	—	1	—	—	μs
$t_{\text{pll_lock}}$ ⁽¹⁵⁴⁾	—		—	10	—	—	10	μs

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

⁽¹⁵³⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁴⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Symbol	Parameter	Min	Typ	Max	Unit
$f_{OUT}^{(169)}$	Output frequency for an internal global or regional clock (C3, I3L speed grade)	—	—	650	MHz
	Output frequency for an internal global or regional clock (C4, I4 speed grade)	—	—	580	MHz
$f_{OUT_EXT}^{(169)}$	Output frequency for an external clock output (C3, I3L speed grade)	—	—	667	MHz
	Output frequency for an external clock output (C4, I4 speed grade)	—	—	533	MHz
$t_{OUTDUTY}$	Duty cycle for a dedicated external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code>	—	—	100	MHz
t_{LOCK}	Time required to lock from the end-of-device configuration or deassertion of <code>areset</code>	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/ delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth ⁽¹⁷⁰⁾	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the <code>areset</code> signal	10	—	—	ns

⁽¹⁶⁹⁾ This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

⁽¹⁷⁰⁾ High bandwidth PLL settings are not supported in external feedback mode.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{INCCJ}}^{(171), (172)}$	Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz)	-750	—	+750	ps (p-p)
$t_{\text{OUTPJ_DC}}^{(173)}$	Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTPJ_DC}}^{(173)}$	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
	Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾	mUI (p-p)
$t_{\text{OUTCCJ_DC}}^{(173)}$	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
$t_{\text{FOUTCCJ_DC}}^{(173)}$	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾	ps (p-p)
	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾	mUI (p-p)

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽¹⁷²⁾ The f_{REF} is f_{IN}/N specification applies when $N = 1$.

⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{\text{OUTPJ_IO}}^{(173), (175)}$	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTPJ_IO}}^{(173), (175), (176)}$	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{OUTCCJ_IO}}^{(173), (175)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{FOUTCCJ_IO}}^{(173), (175), (176)}$	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz)	—	—	600	ps (p-p)
	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz)	—	—	60	mUI (p-p)
$t_{\text{CASC_OUTPJ_DC}}^{(173), (177)}$	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz)	—	—	175	ps (p-p)
	Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz)	—	—	17.5	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits

⁽¹⁷⁵⁾ The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

⁽¹⁷⁶⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

⁽¹⁷⁷⁾ The cascaded PLL specification is only applicable with the following condition:

- Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
- Downstream PLL: $\text{Downstream PLL BW} > 2$ MHz